

PHILIPS

Data handbook



Electronic
components
and materials

Components and materials

Part 1 October 1981

PLC modules

PC20 modules

HNIL FZ/30-series

NORbits 60-series, 61-series, 90-series

Input devices

Hybrid integrated circuits

Peripheral devices

COMPONENTS AND MATERIALS

PART 1 - OCTOBER 1981

ASSEMBLIES

PLC MODULES



PC20 MODULES



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NORBITS 60-SERIES, 61-SERIES, 90-SERIES



INPUT DEVICES



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PERIPHERAL DEVICES



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DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, sub-assemblies and materials; it is made up of four series of handbooks each comprising several parts.

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SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
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The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

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May 1980

ELECTRON TUBES (BLUE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	February 1980	T1 02-80 (ET1a 12-75)	Tubes for r.f. heating
Part 2	April 1980	T2 04-80 (ET1b 08-77)	Transmitting tubes for communications
Part 2b	May 1978	ET2b 05-78	Microwave semiconductors and components Gunn, Impatt and noise diodes, mixer and detector diodes, backward diodes, varactor diodes, Gunn oscillators, sub-assemblies, circulators and isolators.
Part 3	June 1980	T3 06-80 (ET2a 11-77)	Klystrons, travelling-wave tubes, microwave diodes
Part 3	January 1975	ET3 01-75	Special Quality tubes, miscellaneous devices
Part 4	September 1980	T4 09-80 (ET2a 11-77)	Magnetrons
Part 5	August 1981	T5 08-81	Cathode-ray tubes Instrument tubes, monitor and display tubes, C.R. tubes for special applications.
Part 6	July 1980	T6 07-80 (ET6 01-77)	Geiger-Müller tubes
Part 7a	March 1977	ET7a 03-77	Gas-filled tubes Thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes.
Part 7b	May 1979	ET7b 05-79	Gas-filled tubes Segment indicator tubes, indicator tubes, switching diodes, dry reed contact units.
Part 8	July 1979	ET8 07-79	Picture tubes and components Colour TV picture tubes, black and white TV picture tubes, monitor tubes, components for colour television, components for black and white television.
Part 9	June 1980	T9 06-80 (ET9 03-78)	Photo and electron multipliers Photomultiplier tubes, phototubes, single channel electron multipliers, channel electron multiplier plates.
Part 10	May 1981	T10 05-81 (ET5b 12-78)	Camera tubes and accessories, image intensifiers

SEMICONDUCTORS (RED SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	March 1980	S1 03-80 (SC1b 05-77)	Diodes Small-signal germanium diodes, small-signal silicon diodes, special diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
Part 2	May 1980	S2 05-80 (SC1a 08-78)	Power diodes, thyristors, triacs Rectifier diodes, voltage regulator diodes (> 1,5 W), rectifier stacks, thyristors, triacs
Part 3	April 1980	S3 04-80 (SC2 11-77, partly) (SC3 01-78, partly)	Small-signal transistors
Part 4	September 1981	S4 09-81 (SC2 06-79)	Low-frequency power transistors
Part 4a	December 1978	SC4a12-78	Transmitting transistors and modules
Part 5	October 1980	S5 10-80 (SC3 01-78, partly)	Field-effect transistors
Part 7	December 1980	S7 12-80 (SC4c 07-78)	Microminiature semiconductors for hybrid circuits
Part 8	April 1980	S8 06-81 (SC4b 09-78)	Devices for optoelectronics Photosensitive diodes and transistors, light-emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices
Part 10	September 1981	S10 09-81 (SC3 01-78, partly)	Wideband transistors and wideband hybrid IC modules

INTEGRATED CIRCUITS (PURPLE SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code. Books with the purple cover will replace existing red covered editions as each is revised.

Part 1	May 1980	IC1 05-80 (SC5b 03-77)	Bipolar ICs for radio and audio equipment
Part 2	May 1980	IC2 05-80 (SC5b 03-77)	Bipolar ICs for video equipment
Part 5a	November 1976	SC5a 11-76	Professional analogue integrated circuits
Part 4	October 1980	IC4 10-80 (SC6 10-77)	Digital integrated circuits LOCMOS HE4000B family
Part 6b	August 1979	SC6b 08-79	ICs for digital systems in radio and television receivers
Part 7	May 1981	IC7 05-81	Signetics Bipolar memories
Part 8	May 1981	IC8 05-81	Signetics Analogue circuits
Part 9	November 1981	IC9 11-81	Signetics TTL Logic

COMPONENTS AND MATERIALS (GREEN SERIES)

Starting in 1980, new part numbers and corresponding codes are being introduced. The former code of the preceding issue is given in brackets under the new code.

Part 1	October 1981	C1 10-81	Assemblies for industrial use PLC modules, PC20 modules, HN1L FZ/30 series, NORbits 60-, 61-, 90-series, input devices, hybrid ICs, peripheral devices
Part 2	June 1981	C2 06-81 (CM3a 09-78)	FM tuners, television tuners, video modulators, surface acoustic wave filters
Part 3	January 1981	C3 01-81 (CM3b 10-78)	Loudspeakers
Part 4a	November 1978	CM4a 11-78	Soft Ferrites Ferrites for radio, audio and television, beads and chokes, Ferroxcube potcores and square cores, Ferroxcube trans- former cores
Part 4b	February 1979	CM4b 02-79	Piezoelectric ceramics, permanent magnet materials
Part 6	May 1981	C6 05-81 (CM6 04-77)	Electric motors and accessories Permanent magnet synchronous motors, stepping motors, direct current motors
Part 7a	January 1979	CM7a 01-79	Assemblies Circuit blocks 40-series and CSA70 (L), counter modules 50-series, input/output devices
Part 8	September 1981	C8 09-81 (CM8 06-79)	Variable mains transformers
Part 9	August 1979	CM9 08-79	Piezoelectric quartz devices Quartz crystal units, temperature compensated crystal oscillators
Part 10	October 1980	C10 10-80	Connectors
Part 11	December 1979	CM11 12-79	Non-linear resistors Voltage dependent resistors (VDR), light dependent resist- ors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC)
Part 12	November 1979	CM12 11-79	Variable resistors and test switches
Part 13	December 1979	CM13 12-79	Fixed resistors
Part 14	April 1980	C14 04-80 (CM2b 02-78)	Electrolytic and solid capacitors
Part 15	May 1980	C15 05-80 (CM2b 02-78)	Film capacitors, ceramic capacitors, variable capacitors

PLC MODULES



MODULES FOR PROGRAMMABLE LOGIC CONTROLLERS

INTRODUCTION

The programmable logic controller (PLC) is used for the controlling of machines or processes. It can be easily programmed and re-programmed as required.

The modular design of the PLC enables a user to build a PLC which is 'tailor-made' for his control task. By specifying the number and the types of PLC modules that he requires, he avoids purchasing more of the expensive electronic capability than he needs.

The PLC modules are formed on standard double Eurocards. Optically coupled interface circuits, specifically designed for an industrial environment, provide excellent noise immunity and a high degree of isolation. The internationally accepted machine signal level of 24 V is used and generous tolerances on operational margins and thresholds ease compatibility headaches.

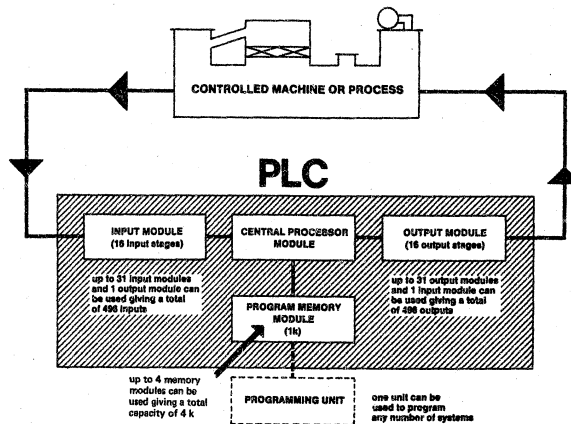
Besides the PLC modules, the PLC comprises back panels, a frame (19 in rack) and a standard power supply. The frame must conform to IEC297 or DIN41494 (for racks) and IEC130-14 or DIN41612 (for connectors). The adoption of these standards means that the frame and the power supply should be easily obtainable.

The following PLC modules are available.

type	description	catalogue no.
CP10	central processor, 32 registers	4322 027 90420
CP11	central processor, without registers	4322 027 90390
IM10	input module, 16 inputs, 24 V d.c.	4322 027 90434
IM11	input module, 16 inputs, 24 V a.c.	4322 027 90403
LX10	load external interface module	4322 027 91600
MM10	program memory module, 1 k, non-volatile core RAM	4322 027 91400
MM11	program memory module, non-volatile, UV-erasable PROMs, 1 k 13 or 2 k 13 capacity; for program copying or read-out	4322 027 91630
MM12	program memory module, non-volatile, UV-erasable PROMs, 1 k 13 or 2 k 13 capacity; for read-out only	4322 027 91640
OM10	output module, 16 outputs, max. 0,1 A each, 24 V d.c.	4322 027 90440
OM12	output module, 8 outputs max. 2 A each, 24 V d.c.	9360 011 50112
PI10*	punch and teletype interface module	8222 412 41572
PU10	programming unit	4322 027 90410
BP11 to BP16	back panels	9390 269 .0112

* Development type.

The diagram shows, in a simplified form, the function of each of the PLC modules. In operation the PLC cycles continuously through a data input/output cycle and a data processing cycle.



The input module converts the signals from the plant into a binary form acceptable to the central processor.

The central processor reads the data from the input module, performs logic equations on it in accordance with the program instructions and transfers the results to the output module.

The output module converts the binary data from the central processor to electrical signals suitable for the control of the plant.

The program memory is the store in which the set of instructions that comprise the program are stored. These instructions dictate the actions which must be taken in response to the condition of each input.

The programming unit is the means by which an operator can write a program, or changes to a program, into the program memory. The unit is portable and thus one may be used to serve any number of PLCs. It is also sufficiently inexpensive to make the permanent location of one in each PLC for monitoring or test purposes, a realistic and useful proposition.

GENERAL CHARACTERISTICS

Operating temperature range	0 to +60 °C
Storage temperature range	-40 to +70 °C
Dimensions	160 mm x 233 mm (double Eurocard) according to IEC297 or DIN41494
Supply voltage (d. c.)	$V_P = 5 \text{ V} \pm 5\%$; $\frac{dV_P}{dt} \leq 5 \text{ V/ms}$
Maximum number of input + output signals	512
Maximum program length	4 x 1024 words
Cycle time	$0,029 (n_{IM} + n_{OM}) + 1,85 n_{MM} \text{ ms}$ n_{IM} = number of input modules n_{OM} = number of output modules n_{MM} = number of memory modules

TESTS AND REQUIREMENTS

All modules are designed to meet the tests below.

Vibration test

IEC68-2, test method Fc: 5 to 55 Hz, amplitude 1,5 mm or 5 g (whichever is less).

Shock test

IEC68-2, test method Ea: 3 shocks in 6 directions, pulse duration 11 ms, peak acceleration 50 g.

Rapid change of temperature test

IEC68-2, test method Na: 5 cycles of 2 h at -40 °C and 2 h at +70 °C.

Damp heat test

IEC68-2, test method Ca: 21 days at 40 °C, R.H. 90 to 95%.

CENTRAL PROCESSORS

DESCRIPTION

These central processors are modules intended for use in combination with the input module IM10 (or IM11), memory module MM10 (or MM11 or MM12), output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC). The central processor is the heart of the logic controller; it asks the input modules for data and the program memory for instructions, processes the data according to these instructions, and applies the result to the output modules. It also generates the internal timing of the controller.

The processor actions take place in two distinct cycles: an input/output cycle and a data processing cycle.

During the input/output cycle the processor addresses each input stage in turn (counter/buffer register) and transfers the present data to the corresponding scratch-pad memory location, see Fig. 1. In the same cycle the processed data of the previous data processing cycle are clocked out from the scratch-pad memory into the latch flip-flops of the output modules. As the scratch-pad memory can hold up 512 bits of data the central processor can handle a maximum combination of 512 inputs, outputs, and intermediate results. Provision is made to prevent loss of information of the scratch-pad memory in the case of power failure.

During the data processing cycle the processor applies an address and a cycle initiate signal to the program memory, which in turn then apply a program word to the processor. The program word contains an instruction and an address, which comprise 13 data bits. An instruction consists of 4 bits of data; these are applied to the logic processing unit and the register processing unit. ¹⁾ The other 9 bits of data form the scratch-pad memory address and are used to select the data bit at this memory location, and also one of the 32 8-bit registers. ¹⁾ The logic processing unit only processes data from the scratch-pad memory. The register processing unit processes the data stored in one of the 8-bit registers, in conjunction with a working register (A-register). Due to the fact that a register is always selected when a scratch-pad memory address is selected, the results of register processing will be stored in the corresponding scratch-pad memory location (condition register). Data for the registers can be supplied by the program memory or by an external source. These data are stored in the registers during the data processing cycle.

¹⁾ Only present in the CP10.

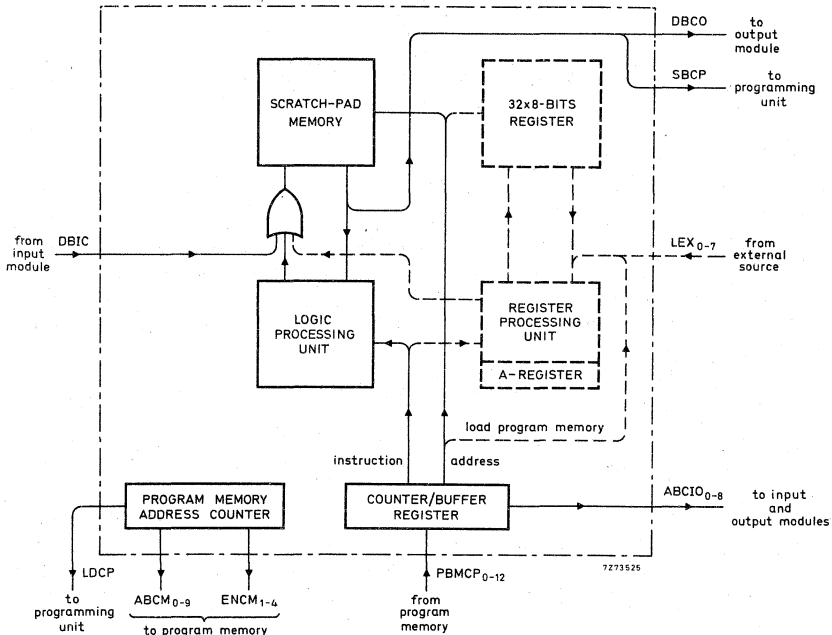


Fig. 1. Simplified block diagram of the central processor. Blocks drawn with broken lines are only extant in the CP10.

The central processor is built on an epoxy-glass printed-wiring board of 233, 4 mm x 160 mm (Euro-card system). The board is provided with two F068-I connectors (board parts); the corresponding panel parts are available under catalogue number 2422 025 89288 (pins for wire wrap), 2422 025 89298 (pins for dip soldering) or 2422 025 89326 (solder tags) ¹⁾. The board has a metal screen at the components side, which is connected to the 0 V line.

¹⁾ For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)
current

V_P 5 V \pm 5%
 I_P max. 2,1 A
typ. 1,9 A

Battery back-up requirements to save contents of the scratch-pad memory in case of power failure.

Battery voltage

V_B 4,5 to 7,5 V

Battery current ($V_P = 0$ V)

I_B typ. 3,5 mA at $V_B = 5$ V

Trickle charge current ($V_P = 5$ V)

typ. 2 mA at $V_B = 5$ V

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminations (Fig. 4)	
			connector 1	connector 2
PBMCP ₀	Program word bits from program memory.	1 TTL		a2, c2
PBMCP ₁		1 TTL		a3, c3
PBMCP ₂		1 TTL		a4, c4
PBMCP ₃		1 TTL		a5, c5
PBMCP ₄		1 TTL		a6, c6
PBMCP ₅		1 TTL		a7, c7
PBMCP ₆		1 TTL		a8, c8
PBMCP ₇		1 TTL		a9, c9
PBMCP ₈		1 TTL		a10, c10
PBMCP ₉		1 TTL		a11, c11
PBMCP ₁₀		1 TTL		a12, c12
PBMCP ₁₁		1 TTL		a13, c13
PBMCP ₁₂		1 TTL		a14, c14
MICC		Memory identification signal; this signal is connected to one of the four ENCM-outputs of the central processor.	2 TTL	a5
SCPC	Store command from programming unit; initiates SCCM (see output data) when the central processor is in a data processing cycle.	2 TTL		a15, c15
DBIC	Data bit from input stage; data is stored in scratch-pad memory during input/output cycle.	3 TTL	c20	
CLCP	Clear signal from external source. When CLCP is LOW the central processor is kept in the start position of an input/output cycle; when CLCP is HIGH the central processor is running (see also SPCE).	2 TTL	a20	

input	function	load	terminations (Fig. 4)	
			connector 1	connector 2
SPCE	Scratch-pad clear enable line from external source. When SPCE is HIGH and CLCP goes from LOW to HIGH all scratch-pad places (except those which are addressed as an input) are set to zero in the first input/output cycle; when SPCE is LOW and CLCP goes from LOW to HIGH the central processor starts with a normal input/output cycle.	2 TTL	a22	
IDIC	Identification signal from input module; prepares central processor for data on DBIC to be written in the scratch-pad memory.	3 TTL	c24	
IDLC	Identification signal from last input or output module; indicates that the last input or output module has been selected.	2 TTL	c26	
LEX ₀ LEX ₁ LEX ₂ LEX ₃ LEX ₄ LEX ₅ LEX ₆ LEX ₇	Data inputs from an external source; eight data bits from an external source can be loaded into the A-register.	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL	a6 a7 a8 a9 a10 a11 a12 a13	

Output data

All outputs meet the standard TTL specifications.

output	function	loadability	terminations (Fig. 4)	
			connector 1	connector 2
ABCIO ₀	Address bits to input and output modules. ABCIO ₀₋₃ select the input or output stage, ABCIO ₄₋₈ select the input or output modules.	32 TTL	c2	
ABCIO ₁		32 TTL	c4	
ABCIO ₂		32 TTL	c6	
ABCIO ₃		32 TTL	c8	
ABCIO ₄		32 TTL	c10	
ABCIO ₅		32 TTL	c12	
ABCIO ₆		32 TTL	c14	
ABCIO ₇		32 TTL	c16	
ABCIO ₈		32 TTL	c18	

output	function	loadability	terminations (Fig. 4)	
			connector 1	connector 2
ABCM ₀	Address bits to program memory, initiated by program address counter.	10 TTL		a20, c20
ABCM ₁		10 TTL		a21, c21
ABCM ₂		10 TTL		a22, c22
ABCM ₃		10 TTL		a23, c23
ABCM ₄		10 TTL		a24, c24
ABCM ₅		10 TTL		a25, c25
ABCM ₆		10 TTL		a26, c26
ABCM ₇		10 TTL		a27, c27
ABCM ₈		10 TTL		a28, c28
ABCM ₉		10 TTL		a29, c29
ENCM ₁	Enable signal to program memory; four lines are necessary when program memory capacity is extended to 4 k	8 TTL	a1, c1	
ENCM ₂		8 TTL	a2	
ENCM ₃		8 TTL	a3	
ENCM ₄		8 TTL	a4	
SCCM	Store command to program memory; level determines whether a program word is read out from program memory to central processor (LOW) or a new program word is written into the program memory (HIGH). SCCM = $\overline{\text{SCPC}}$.	10 TTL		a17, c17
CICM	Cycle initiate signal to program memory; depending on the level of SCCM, CICM starts read/restore or clear/write cycle (bipolar to reduce noise sensitivity).	9 TTL		a19, c19
$\overline{\text{CICM}}$				a18, c18
$\overline{\text{CL}}_{23}$	Inverted clock signal to programming unit.	10 TTL	a15	
CLCO	Clock signal to output module, stores data on DBCO into output stage during input/output cycle.	32 x OM10	a28	
DBCO	Data bit to output module; data is stored in output stage by CLCO.	31 TTL	c22	
SBCP	Status bit to programming unit; clocked by ϕ_{57} it indicates "1" or "0" at selected scratch-pad memory address.	1 TTL	a16	
LDCP	Synchronization signal to programming unit, synchronizes auxiliary address counter in programming unit with address counter in central processor.	10 TTL	a14	
ϕ_{57}	Clock signal for state indication on programming unit; occurs only during data processing cycle.	10 TTL		a16, c16

Alarm output (a26 of connector 1): open collector output, which indicates a LOW level when $V_p < 4,75 \text{ V}$. V_{alarm} , LOW level $< 0,4 \text{ V}$ at $I_c = 3 \text{ mA}$.

Time data

Scan time per input or output module	0,029 ms
Read time per 1 k memory module	1,85 ms
Total cycle time	$0,029 (n_{IM} + n_{OM}) + 1,85 n_{MM}$ ms
	n_{IM} = number of input modules
	n_{OM} = number of output modules
	n_{MM} = number of memory modules

Note - By removing a wire jump, marked "A", on the central processor board the scan time per input or output module is set to 7,4 ms.

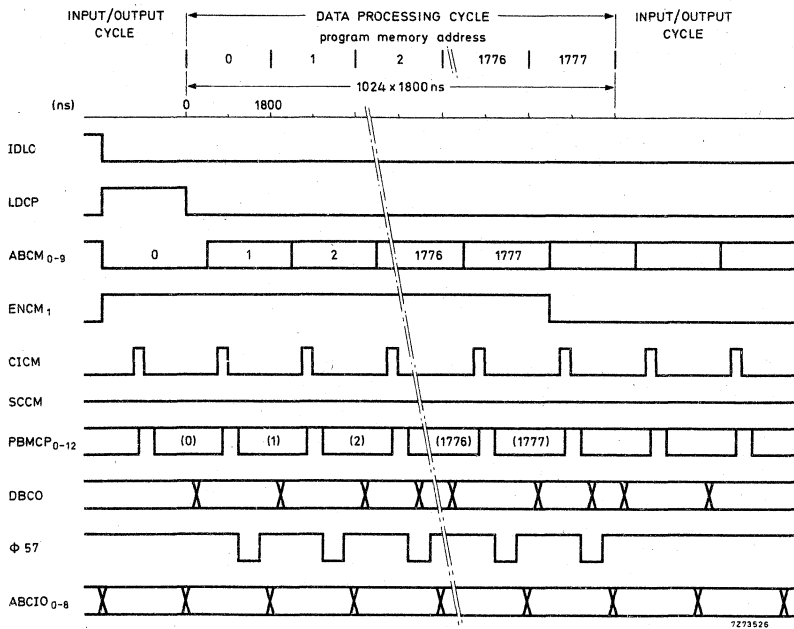


Fig.2. Timing diagram of data processing cycle.

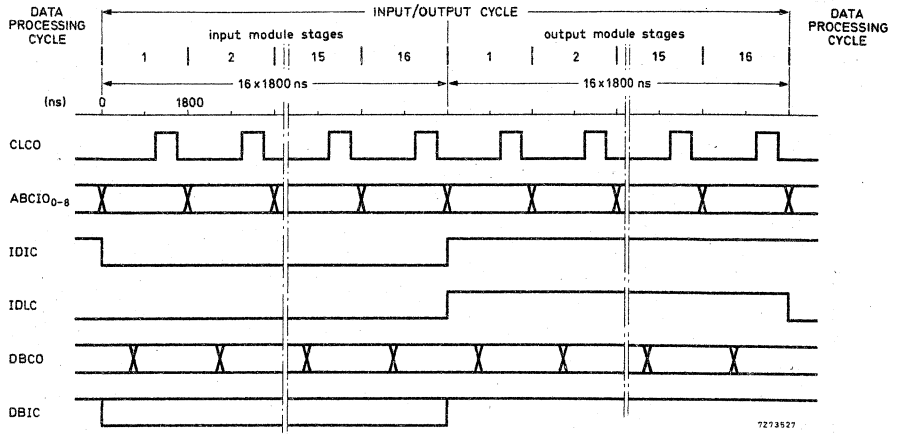


Fig. 3. Timing diagram of input/output cycle.

MECHANICAL DATA

Dimensions in mm

Outlines

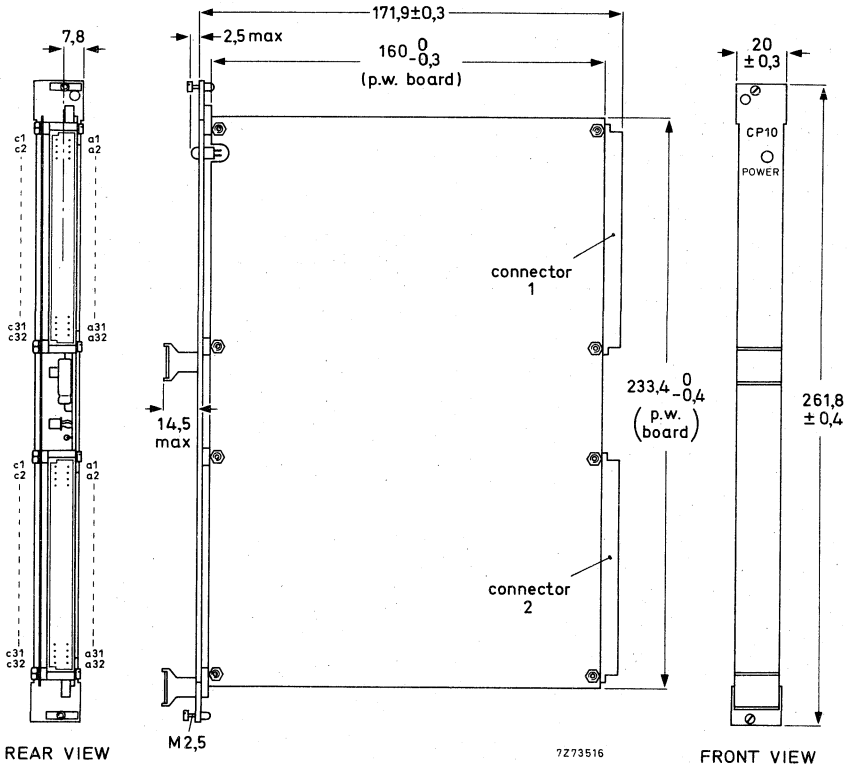


Fig. 4

Mass

400 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
ENCM ₁	1	ENCM ₁	i. c.	1	i. c.
ABCIO ₀	2	ENCM ₂	PBMCP ₀	2	PBMCP ₀
n. c.	3	ENCM ₃	PBMCP ₁	3	PBMCP ₁
ABCIO ₁	4	ENCM ₄	PBMCP ₂	4	PBMCP ₂
n. c.	5	MICC	PBMCP ₃	5	PBMCP ₃
ABCIO ₂	6	LEX ₀	PBMCP ₄	6	PBMCP ₄
n. c.	7	LEX ₁	PBMCP ₅	7	PBMCP ₅
ABCIO ₃	8	LEX ₂	PBMCP ₆	8	PBMCP ₆
n. c.	9	LEX ₃	PBMCP ₇	9	PBMCP ₇
ABCIO ₄	10	LEX ₄	PBMCP ₈	10	PBMCP ₈
n. c.	11	LEX ₅	PBMCP ₉	11	PBMCP ₉
ABCIO ₅	12	LEX ₆	PBMCP ₁₀	12	PBMCP ₁₀
n. c.	13	LEX ₇	PBMCP ₁₁	13	PBMCP ₁₁
ABCIO ₆	14	LDCP	PBMCP ₁₂	14	PBMCP ₁₂
n. c.	15	CL ₂₃	SCPC	15	SCPC
ABCIO ₇	16	SBCP	φ57	16	φ57
n. c.	17	n. c.	SCCM	17	SCCM
ABCIO ₈	18	n. c.	CICM	18	CICM
n. c.	19	n. c.	CICM	19	CICM
DBIC	20	CLCP	ABCM ₀	20	ABCM ₀
n. c.	21	n. c.	ABCM ₁	21	ABCM ₁
DBC0	22	SPCE	ABCM ₂	22	ABCM ₂
n. c.	23	n. c.	ABCM ₃	23	ABCM ₃
IDIC	24	n. c.	ABCM ₄	24	ABCM ₄
n. c.	25	n. c.	ABCM ₅	25	ABCM ₅
IDLC	26	alarm	ABCM ₆	26	ABCM ₆
n. c.	27	n. c.	ABCM ₇	27	ABCM ₇
0 V ¹⁾	28	CLCO	ABCM ₈	28	ABCM ₈
n. c.	29	n. c.	ABCM ₉	29	ABCM ₉
n. c.	30	n. c.	V _B	30	V _B
V _P	31	V _P	V _P	31	V _P
0 V	32	0 V	0 V	32	0 V

n. c. = not connected.
i. c. = internal connection.

¹⁾ No supply line; only to be used as a ground connection for CLCO.

INPUT MODULES

DESCRIPTION

These input modules are intended for use in combination with the central processor CP10 (or CP11), memory module MM10 (or MM11 or MM12), output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC).

The IM10 and IM11 are identical in many respects, but the IM10 is designed for d.c. inputs, whereas the IM11 is designed for a.c. and unsmoothed rectified inputs. Each input module contains 16 addressable input stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All inputs are floating with respect to each other. Each input stage has a LED for status indication: it is lit when the input is active. A delay circuit (symmetrical delay time typ. 1 ms) is incorporated in each input stage of the IM10, to increase the noise immunity. The delay time can be increased by adding extra capacitance (approx. 0,068 $\mu\text{F}/\text{ms}$). A rectifying and smoothing circuit is incorporated in each input stage of the IM11.

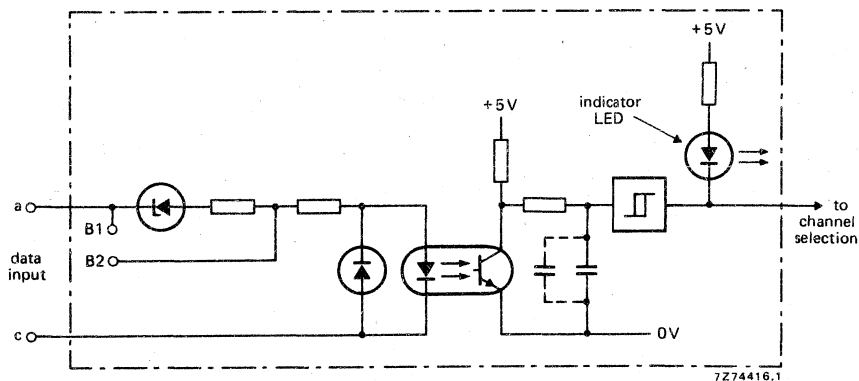


Fig. 1a Circuit diagram of an input stage (IM10).

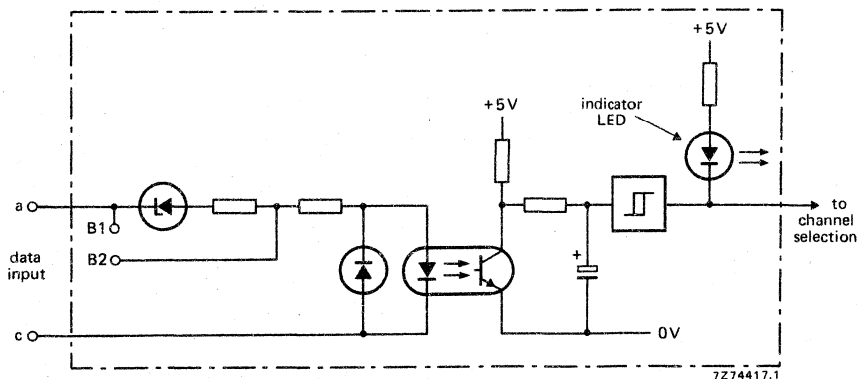


Fig. 1b Circuit diagram of an input stage (IM11).

Each input module has nine address inputs ($ABCIO_{0-8}$) and five module identification inputs (\overline{MID}_{0-4}), which are accessible on the connectors at the rear (Fig. 2).

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (Euro-card system). The board is provided with two F068-1 connectors (board parts); the corresponding rack parts are available on the back panels BP11 to BP16 or separately under catalogue number 2422 025 89291 (pins for wire wrapping), 2422 025 89299 (pins for dip soldering) or 2422 025 89327 (solder tags).*

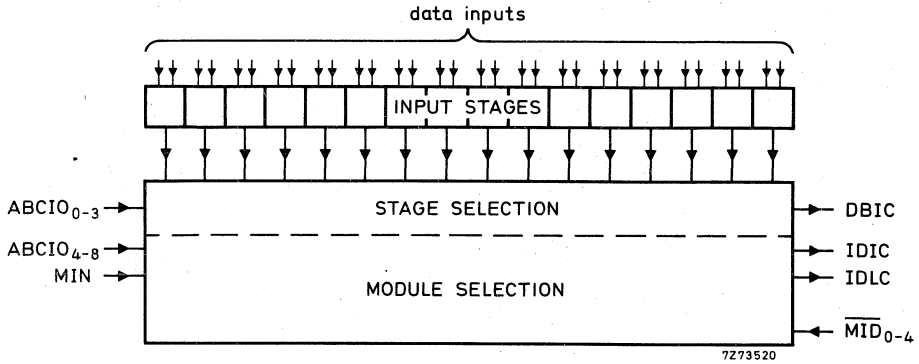


Fig. 2 Block diagram of the input modules.

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)
current

V_p	5 V \pm 5%
I_p	max. 0,5 A typ. 0,45 A

Input data

The data inputs are DI_{XY0} to DI_{XY7} and DI_{XZ0} to DI_{XZ7} . They are accessible on connector 2, see "Terminal location".

	5 V level**	24 V level
Active voltage (V_{a-c})*	3,5 to 6 V \blacktriangle	17 to 30 V \blacktriangle
Non-active voltage (V_{a-c})*	0 to 0,8 V or floating \blacktriangle	0 to 7 V or floating \blacktriangle
Input current, active at V_{a-c} = 5 V or 24 V resp.	typ. 10 mA	typ. 10 mA

The inputs mentioned below meet the standard TTL specifications.

input	function	load	terminations of connector 1 (Fig. 3)
ABCIO ₀ ABCIO ₁ ABCIO ₂ ABCIO ₃ ABCIO ₄ ABCIO ₅ ABCIO ₆ ABCIO ₇ ABCIO ₈	Address bits from central processor; ABCIO ₀₋₃ select the input stage, ABCIO ₄₋₈ selection the input module.	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL	a2, c2 a4, c4 a6, c6 a8, c8 a10 a12 a14 a16 a18
MIN	Module inhibit signal from external source; a low level applied to this input inhibits data on DBIC to be stored in the scratch-pad memory of the central processor.	2 TTL	c26
MID ₀ MID ₁ MID ₂ MID ₃ MID ₄	Module identification inputs; provide module with individual identity.	2 TTL 2 TTL 2 TTL 2 TTL 2 TTL	c10 c12 c14 c16 c18

* Voltage between terminal of row a and terminal of row c of connector 2.

** By short-circuiting terminals B1 and B2 (see Figs 1a and 1b).

\blacktriangle D.C. (for IM10) or a.c. values (for IM11).

Output data

All outputs (open collector) meet the standard TTL specifications.

output	function	loadability	terminations of connector 1 (Fig. 3)
DBIC	Data bit to central processor; data is stored in scratch-pad memory of central processor.	10 TTL	a20
IDIC	Identification signal to central processor (active LOW); prepares central processor for data on DBIC to be written in the scratch-pad memory.	10 TTL	c24
IDLC	Identification signal from last input module to central processor (active HIGH); only the IDLC output of the last input module has to be connected with the IDLC input of the central processor.	2 TTL	a26



MECHANICAL DATA

Dimensions in mm

Outlines

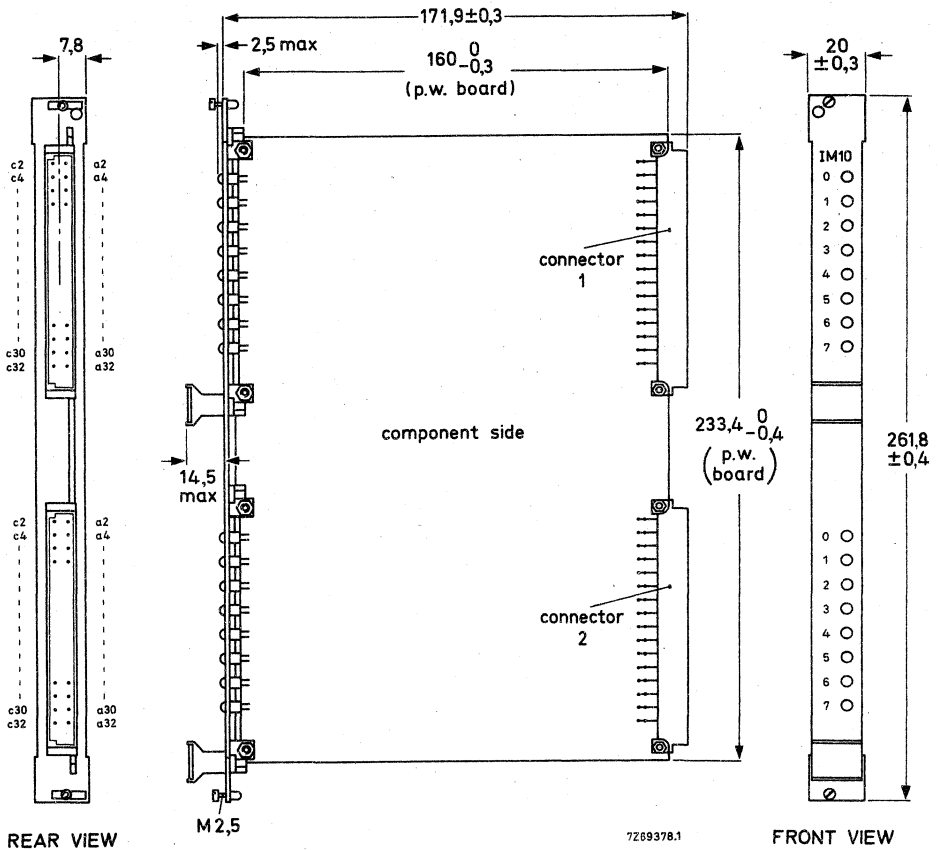


Fig. 3.

Mass 250 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
ABCIO ₀	2	ABCIO ₀	DI _X Y ₀	2	DI _X Y ₀
ABCIO ₁	4	ABCIO ₁	DI _X Y ₁	4	DI _X Y ₁
ABCIO ₂	6	ABCIO ₂	DI _X Y ₂	6	DI _X Y ₂
ABCIO ₃	8	ABCIO ₃	DI _X Y ₃	8	DI _X Y ₃
MID ₀	10	ABCIO ₄	DI _X Y ₄	10	DI _X Y ₄
MID ₁	12	ABCIO ₅	DI _X Y ₅	12	DI _X Y ₅
MID ₂	14	ABCIO ₆	DI _X Y ₆	14	DI _X Y ₆
MID ₃	16	ABCIO ₇	DI _X Y ₇	16	DI _X Y ₇
MID ₄	18	ABCIO ₈	DI _X Z ₀	18	DI _X Z ₀
0 V*	20	DBIC	DI _X Z ₁	20	DI _X Z ₁
0 V*	22	n.c.	DI _X Z ₂	22	DI _X Z ₂
IDIC	24	n.c.	DI _X Z ₃	24	DI _X Z ₃
MIN	26	IDLC	DI _X Z ₄	26	DI _X Z ₄
n.c.	28	n.c.	DI _X Z ₅	28	DI _X Z ₅
V _p	30	V _p	DI _X Z ₆	30	DI _X Z ₆
0 V	32	0 V	DI _X Z ₇	32	DI _X Z ₇

n.c. = not connected.

* No supply line; only to be used for coding of the MID₀₋₄ lines.

LOAD EXTERNAL INTERFACE

DESCRIPTION

This load external interface is intended for use in combination with the central processor CP10, input module IM10 or IM11, output module OM10 or OM12, memory module MM10, MM11 or MM12 and programming unit PU10 to assemble a programmable logic controller (PLC). The module can be used as an interface between the load external inputs LEX₀ to LEX₇ on the CP10 and a number of 8-bit data sources. The data outputs of the different data sources have to be connected to one 8-bit data bus. The LX10 has 16 enable outputs \overline{EN}_0 to \overline{EN}_{17} , which are to enable the different data sources. The 8-bit data bus has to be connected to the data inputs DB₀ to DB₇. The data applied to the data inputs can be inverted on the LX10 by activating the data bit invert input DBI (see the truth table on the next page). The applied data can have a 5 V or a 24 V level. A block diagram is given in Fig. 1. The data inputs and enable outputs are electrically isolated from the 5 V logic circuitry by means of photocouplers. All data inputs are floating with respect to each other. Reading data from the data sources will only occur during the input/output cycle. The data are then stored in a 16 x 8 random-access memory (RAM) on the LX10. The data can be read out of the RAM during the data processing cycle. Storing data into the RAM can be inhibited by applying a 0 V level to the module inhibit input (MIN). Reading data out of the RAM cannot be inhibited. The module has 6 address inputs ABCIO₃ to ABCIO₈. This means that a total number of 64 data sources of 8-bits can be connected to the PLC system via 4 LX10 modules. Therefore the module is provided with 2 module identification inputs (\overline{MID}_3 , \overline{MID}_4) which are accessible on the connector. Irrespective of the number of LX10 modules used, a complete input/output cycle of 0,924 ms will occur.

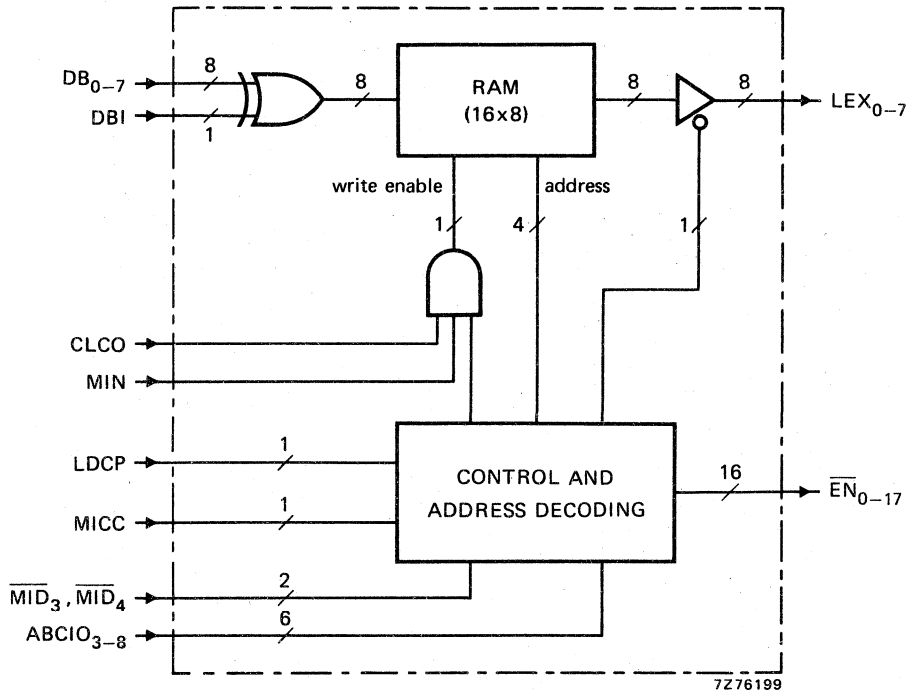


Fig. 1.

Truth Table

data inputs DB ₀ to DB ₇	data input DBI	data output LEX ₀ to LEX ₇
active	active	0
non-active	active	1
active	non-active	1
non-active	non-active	0

ELECTRICAL DATA

Supply

Logic supply voltage (d.c.)

V_p 5 V \pm 5%

Logic supply current (d.c.)

I_p max. 0,7 A
typ. 0,6 A

Supply voltage (d.c.) to drive enable outputs

5 V \pm 5%
24 V \pm 25%

Supply current (d.c.) to drive enable outputs

max. 3 mA
typ. 2,5 mA

Input data

The data inputs are DB₀ to DB₇ and DBI. They are accessible on connector 2 (see "Terminal location" and Fig. 2 for connection).

Active voltage (V_{a-c})*

5 V level	24 V level
3,5 to 6 V	18 to 30 V
0 to 0,8 V	0 to 0,8 V
typ. 10 mA	typ. 10 mA

Non-active voltage (V_{a-c})*

Input current, active at $V_{a-c} = 5$ V or 24 V resp.

Connector 2

row a, terminals 1, 3, 5, 7, 9, 11, 13, 15, 17

row a, terminals 2, 4, 6, 8, 10, 12, 14, 16, 18

row c, terminals (1,2), (3,4), (5,6), (7,8),
(9,10), (11,12), (13,14),
(15,16), (17,18)

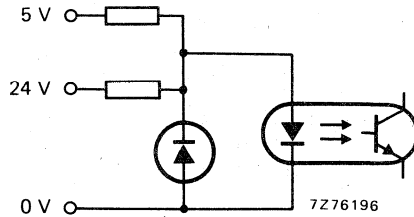


Fig. 2 Input circuit DB₀ to DB₇ and DBI.

All other inputs are connected to the CP10 and meet the standard TTL specification except the CLCO-input.

* Voltage between terminal of row a and terminal of row c of connector 2.

input	function	load	terminations (Fig. 4)	
			connector 1	connector 2
ABCIO ₃ ABCIO ₄ ABCIO ₅ ABCIO ₆ ABCIO ₇ ABCIO ₈	Address bits from central processor.	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL	a8 a10 a12 a14 a16 a18	
LDCP	Signal from central processor indicating the beginning of data processing cycle.	2 TTL	c15	
MICC	Signal from central processor; trailing edge indicates the end of the data processing cycle.	1 TTL	c5	
MIN	Module inhibit signal from external source; a LOW level applied to this input inhibits data on DB ₀ to DB ₇ to be stored in the RAM on the LX10.	2 TTL	c26	
$\overline{\text{MID}}_3$ $\overline{\text{MID}}_4$	Module identification inputs.	2 TTL 2 TTL	c16 c18	
CLCO *	Clock signal from central processor.	*	a28	

* Input with relatively high input resistance (typ. 40 k Ω).

CLCO-input, LOW level: max. 1 V;
HIGH level: min. 2.4 V.

Output data

The enable outputs are \overline{EN}_0 to \overline{EN}_{17} ; they are open-collector outputs.

Output voltage LOW, with respect to COMMON

at $I_{\overline{EN}} = 80 \text{ mA}$

$\leq 0,5 \text{ V}$

Output voltage HIGH

$\leq 30 \text{ V}$

output	function	loadability	terminations (Fig. 4)	
			connector 1	connector 2
LEX ₀ LEX ₁ LEX ₂ LEX ₃ LEX ₄ LEX ₅ LEX ₆ LEX ₇	Data outputs to be connected to LEX ₀ to LEX ₇ inputs of CP10.	10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL 10 TTL	a7 c7 a9 c9 a11 c11 a13 c13	
IDLC	Identification signal from the LX10 to the CP10. This connection forces a complete input/output cycle. This terminal is direct connected to 0 V on the LX10.		a25	

Time data

Time that a data source is enabled

when CP10 is used with non-extended input/output cycle

$t_{en} \quad 58 \mu\text{s}$

when CP10 is used with extended input/output cycle

$t_{en} \quad 14,8 \text{ ms}$

Time that data have to be present on DB₀ to DB₇

before end of enable signal

with non-extended input/output cycle

$t_{ds} \quad 12 \mu\text{s}$

with extended input/output cycle

$t_{ds} \quad 2 \text{ ms}$

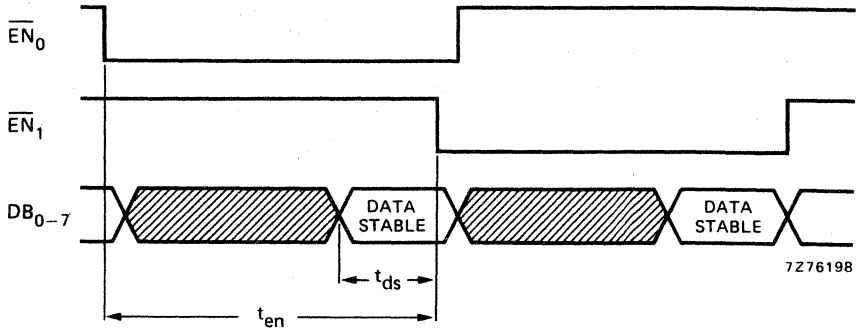


Fig. 3.

MECHANICAL DATA

Dimensions in mm

Outlines

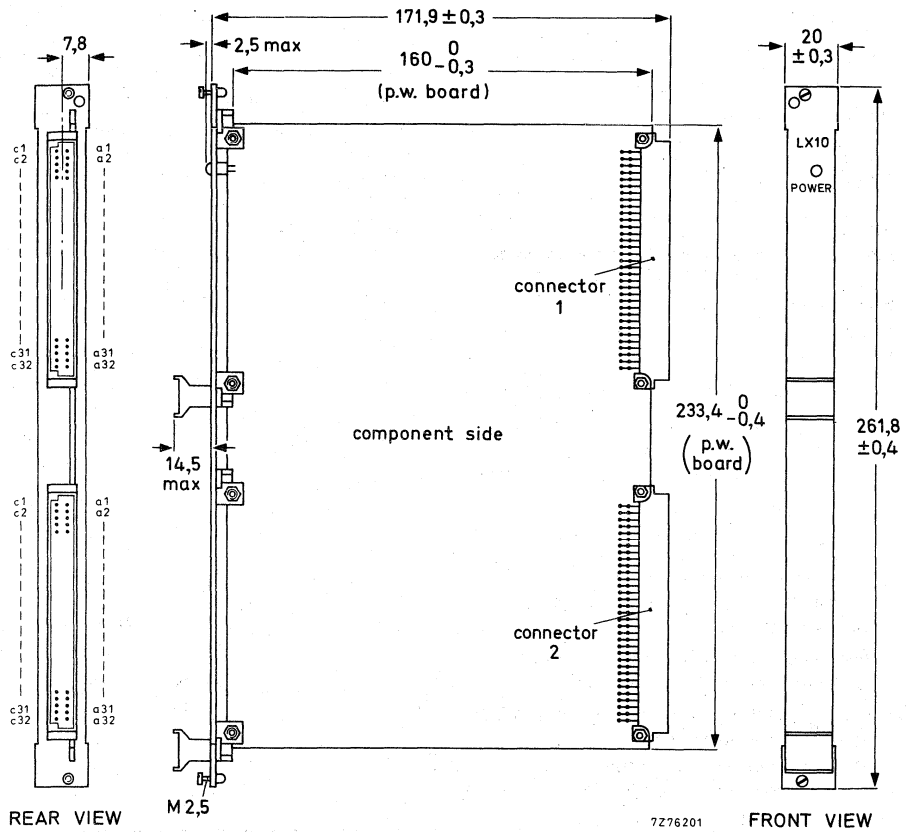


Fig. 4.

Mass 270 g

Terminal location

connector 1		connector 2	
row c	row a	row c	row a
n.c.	1	n.c.	
n.c.	2	n.c.	
n.c.	3	n.c.	
n.c.	4	n.c.	
MICC	5	n.c.	
n.c.	6	n.c.	
LEX ₁	7	LEX ₀	
n.c.	8	ABCIO ₃	
LEX ₃	9	LEX ₂	
n.c.	10	ABCIO ₄	
LEX ₅	11	LEX ₄	
n.c.	12	ABCIO ₅	
LEX ₇	13	LEX ₆	
n.c.	14	ABCIO ₆	
LDCP	15	n.c.	
\overline{MID}_3	16	ABCIO ₇	
n.c.	17	n.c.	
\overline{MID}_4	18	ABCIO ₈	
n.c.	19	n.c.	
0 V (note 1)	20	n.c.	
n.c.	21	n.c.	
0 V (note 1)	22	n.c.	
n.c.	23	n.c.	
n.c.	24	n.c.	
n.c.	25	IDLC	
MIN	26	n.c.	
n.c.	27	n.c.	
0 V (note 2)	28	CLCO	
n.c.	29	n.c.	
n.c.	30	n.c.	
(note 3) { 5 V	31	5 V	(note 5) { 24 V
0 V	32	0 V	
			32 COMMON

n.c. = not connected

Notes

1. No supply line; only to be used for coding of the $\overline{MID}_{3,4}$ lines.
2. No supply line; only to be used as a ground connection for CLCO.
3. Logic supply.
4. Interconnected.
5. Enable output drive.

MEMORY MODULE

DESCRIPTION

This memory module is intended for use in combination with the central processor CP10 (or CP11), input module IM10, output module OM10 (or OM12) and programming unit PU10 to assemble a programmable logic controller (PLC). The control program is stored in the memory module.

The memory module is a random access magnetic core memory system with a basic capacity of 1024 words of 13 bits (1 k13) and a cycle time of 1 μ s. The memory is complete in itself; it consists of a 3 D, 3-wire stack, timing selecting and inhibit circuitry, address and data registers, and a memory retention circuit including the 5 V sensing.

The memory module is built on three epoxy-glass printed-wiring boards. The module is provided with two F068-I connectors (board parts, Euro-card system); the corresponding panel parts are available under catalogue number 2422 025 89288 (pins for wire wrap), 2422 025 89298 (pins for dip soldering) or 2422 025 89326 (solder tags) ¹⁾.

ELECTRICAL DATA

Supply

Supply voltage (d. c.)	V_p	5 V \pm 5%
current (cycle time 1, 8 μ s)	I_p	operating max. 5, 1 A typ. 4 A
		standby max. 3, 6 A typ. 3, 3 A

Note: The memory is in standby position when ENCM is LOW.

Cooling

An air velocity of 0,2 m/s is required.

¹⁾ For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19 in racks and IEC 130-14 or DIN 41612 for connectors.

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminations (Fig. 3)	
			connector 1	connector 2
CICM	Cycle initiate signal from central processor to program memory (bipolar to reduce noise sensitivity).	1 TTL		a19, c19
$\overline{\text{CICM}}$		1 TTL		a18, c18
SCCM	Store command from central processor; determines read/restore and clear/write cycle.	2 TTL		a17, c17
ABCM ₀	Address bits from central processor.	2 TTL		a20, c20
ABCM ₁		2 TTL		a21, c21
ABCM ₂		2 TTL		a22, c22
ABCM ₃		2 TTL		a23, c23
ABCM ₄		2 TTL		a24, c24
ABCM ₅		2 TTL		a25, c25
ABCM ₆		2 TTL		a26, c26
ABCM ₇		2 TTL		a27, c27
ABCM ₈		2 TTL		a28, c28
ABCM ₉		2 TTL		a29, c29
ENCM ₁	Enable signal from central processor to select one out of four memory modules.	3 TTL	a1	
ENCM ₂		3 TTL	a2	
ENCM ₃		3 TTL	a3	
ENCM ₄		3 TTL	a4	
PBPM ₀	Program word bits from programming unit.	1 TTL	c1	
PBPM ₁		1 TTL	c2	
PBPM ₂		1 TTL	c3	
PBPM ₃		1 TTL	c4	
PBPM ₄		1 TTL	c5	
PBPM ₅		1 TTL	c6	
PBPM ₆		1 TTL	c7	
PBPM ₇		1 TTL	c8	
PBPM ₈		1 TTL	c9	
PBPM ₉		1 TTL	c10	
PBPM ₁₀		1 TTL	c11	
PBPM ₁₁		1 TTL	c12	
PBPM ₁₂		1 TTL	c13	
ENPB	Enables outputs $\overline{\text{PBMCP}}_0-12$; when LOW these outputs are enabled, when HIGH these outputs are disabled.	2 TTL	a6	

Output data

All outputs meet the standard TTL specifications.

output	function	loadability	terminations (Fig. 3)	
			connector 1	connector 2
PBMCP ₀	Program word bits from program memory to central processor and programming unit. Open collector output with pull-up resistor (3, 9 kΩ).	9 TTL		a2, c2
PBMCP ₁		9 TTL		a3, c3
PBMCP ₂		9 TTL		a4, c4
PBMCP ₃		9 TTL		a5, c5
PBMCP ₄		9 TTL		a6, c6
PBMCP ₅		9 TTL		a7, c7
PBMCP ₆		9 TTL		a8, c8
PBMCP ₇		9 TTL		a9, c9
PBMCP ₈		9 TTL		a10, c10
PBMCP ₉		9 TTL		a11, c11
PBMCP ₁₀		9 TTL		a12, c12
PBMCP ₁₁		9 TTL		a13, c13
PBMCP ₁₂		9 TTL		a14, c14
PBMCP ₀	Inverted PBMCP ₀₋₁₂ enabled by ENPB (three-state outputs).	10TTL	c17	
PBMCP ₁		10TTL	c18	
PBMCP ₂		10TTL	c19	
PBMCP ₃		10TTL	c20	
PBMCP ₄		10TTL	c21	
PBMCP ₅		10TTL	c22	
PBMCP ₆		10TTL	c23	
PBMCP ₇		10TTL	c24	
PBMCP ₈		10TTL	c25	
PBMCP ₉		10TTL	c26	
PBMCP ₁₀		10TTL	c27	
PBMCP ₁₁		10TTL	c28	
PBMCP ₁₂		10TTL	c29	
DA	Data available signal. This signal becomes LOW max. 150 ns after C _{ICM} (or $\overline{C_{ICM}}$), and goes HIGH as soon as the data become available at the outputs (max. 500 ns after C _{ICM} or $\overline{C_{ICM}}$). Open collector output with pull-up resistor (3, 9 kΩ).	9 TTL		a16, c16

Time data

The relationship between the different input and output signals are given when the memory module is operating in a programmable logic controller system.

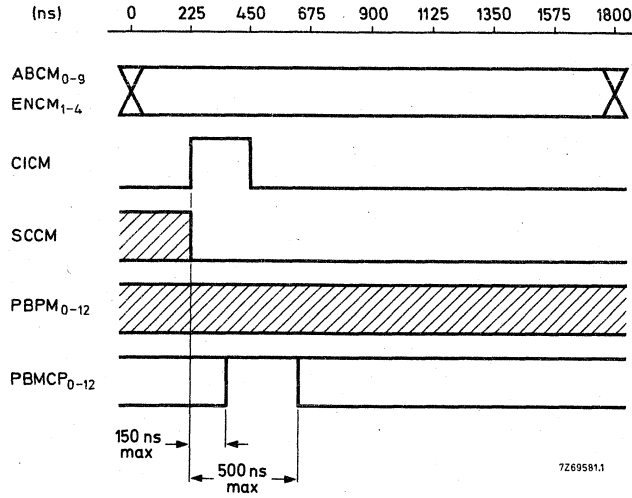


Fig. 1. Timing of read/restore mode.

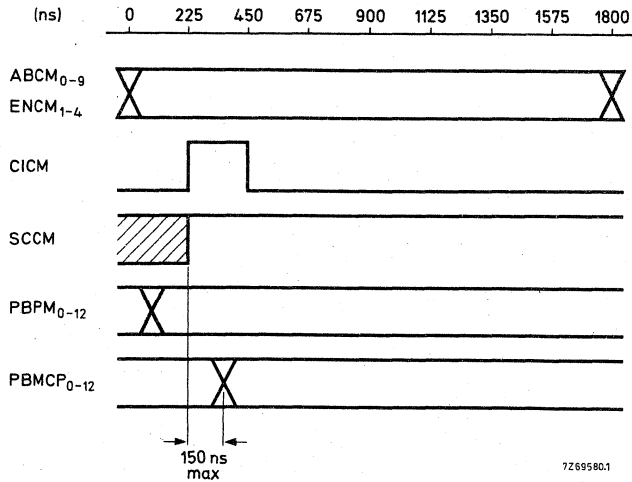


Fig. 2. Timing of clear/write mode.

MECHANICAL DATA

Dimensions in mm

Outlines

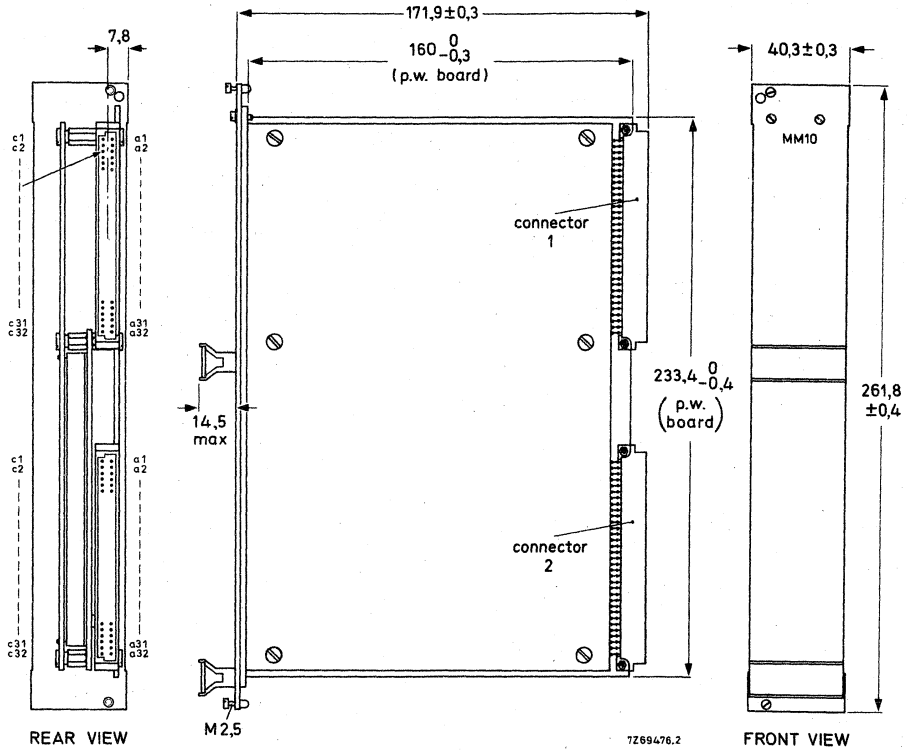


Fig. 3

Mass

780 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
PBPM ₀	1	ENCM ₁	n.c.	1	n.c.
PBPM ₁	2	ENCM ₂	PBMCP ₀	2	PBMCP ₀
PBPM ₂	3	ENCM ₃	PBMCP ₁	3	PBMCP ₁
PBPM ₃	4	ENCM ₄	PBMCP ₂	4	PBMCP ₂
PBPM ₄	5	n.c.	PBMCP ₃	5	PBMCP ₃
PBPM ₅	6	ENPB	PBMCP ₄	6	PBMCP ₄
PBPM ₆	7	n.c.	PBMCP ₅	7	PBMCP ₅
PBPM ₇	8	n.c.	PBMCP ₆	8	PBMCP ₆
PBPM ₈	9	n.c.	PBMCP ₇	9	PBMCP ₇
PBPM ₉	10	n.c.	PBMCP ₈	10	PBMCP ₈
PBPM ₁₀	11	n.c.	PBMCP ₉	11	PBMCP ₉
PBPM ₁₁	12	n.c.	PBMCP ₁₀	12	PBMCP ₁₀
PBPM ₁₂	13	n.c.	PBMCP ₁₁	13	PBMCP ₁₁
n.c.	14	n.c.	PBMCP ₁₂	14	PBMCP ₁₂
n.c.	15	n.c.	i.c.	15	i.c.
n.c.	16	n.c.	DA	16	DA
<u>PBMCP₀</u>	17	n.c.	<u>SCCM</u>	17	<u>SCCM</u>
<u>PBMCP₁</u>	18	n.c.	<u>CICM</u>	18	<u>CICM</u>
<u>PBMCP₂</u>	19	n.c.	CICM	19	CICM
<u>PBMCP₃</u>	20	n.c.	ABCM ₀	20	ABCM ₀
<u>PBMCP₄</u>	21	n.c.	ABCM ₁	21	ABCM ₁
<u>PBMCP₅</u>	22	n.c.	ABCM ₂	22	ABCM ₂
<u>PBMCP₆</u>	23	n.c.	ABCM ₃	23	ABCM ₃
<u>PBMCP₇</u>	24	n.c.	ABCM ₄	24	ABCM ₄
<u>PBMCP₈</u>	25	n.c.	ABCM ₅	25	ABCM ₅
<u>PBMCP₉</u>	26	n.c.	ABCM ₆	26	ABCM ₆
<u>PBMCP₁₀</u>	27	n.c.	ABCM ₇	27	ABCM ₇
<u>PBMCP₁₁</u>	28	n.c.	ABCM ₈	28	ABCM ₈
<u>PBMCP₁₂</u>	29	n.c.	ABCM ₉	29	ABCM ₉
n.c.	30	n.c.	i.c.	30	i.c.
V _P	31	V _P	V _P	31	V _P
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.

i.c. = internal connection.

MEMORY MODULE

DESCRIPTION

The memory module MM11 is intended for use in the PLC system as a program memory or as an auxiliary unit for programming EPROMs (2708); see also Remark below. It contains 4 IC sockets in which 4 UV-erasable EPROMs can be plugged. The MM11 also contains an address buffer, output buffers, and 3 d.c./d.c. converters (5 V to 12 V, 5 V to -5 V and 5 V to 27 V).

The MM11 has three operation modes which can be selected by two mode-selection inputs MSI_1 and MSI_2 (see also truth table under "Input data"):

- Read mode (RD): the module can be used as a read only memory (ROM), that is the situation when the module is used in an operating PLC system.
- Write into master mode (WIM): data from MM10, MM11 or MM12* can program the EPROMs in the IC sockets.
- Write into RAM mode (WIR): the contents of the EPROMs on the MM11 can be written into an MM10*.

The last two modes will be started after pressing a push button, to be connected between terminal 24a of connector 1 and 0 V, or by applying a LOW level to that terminal.

When the MM11 is in the WIM mode the data flow will be as follows:

- the MM11 sends an address ($ABCM_0$ to $ABCM_9$), an enable signal ($ENCM_1$ or $ENCM_2$) and a cycle initiate signal ($CICM/CICM$) to the data source which may be an MM10, MM11 or MM12 (the MM12 does not need a $CICM$ signal);
- the data source will send the data to be programmed into the EPROMs on the MM11.

When the MM11 is in the WIR mode the data flow will be:

- the MM11 sends an address ($ABCM_0$ to $ABCM_9$), an enable signal ($ENCM_1$ or $ENCM_2$), a cycle initiate signal ($CICM/CICM$) and a store command to the MM10;
- data from MM11 will go via $PBPM_0$ to $PBPM_{12}$ to the MM10 and be stored into the MM10.

The MM11 has a capacity of 1k13 or 2k13 depending on whether there are 2 or 4 EPROMs on the module.

The enable input $ENCM_1$ or $ENCM_3$ (addresses 0000 to 1777 and 4000 to 5777 respectively) corresponds with the EPROMs in sockets 1A and 1B. The enable input $ENCM_2$ or $ENCM_4$ (addresses 2000 to 3777 and 6000 to 7777 respectively) corresponds with the EPROMs in sockets 2A and 2B. This means that one program word is stored into 2 EPROMs, A and B, of which EPROMs A contain the instruction and the most significant digit of the address (address part of the program word), and EPROMs B contain the remaining two digits.

The MM11 is supplied with two empty EPROMs 2708.

Remark

Correct programming of EPROMs is only guaranteed, when completely erased EPROMs are used; for the correct erase procedure consult the relevant data sheet of the 2708 EPROMs.

* The connections between these modules have to be done in a separate module set-up, outside the system. No special programming apparatus is required.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)

 V_p 5 V \pm 5%

Supply current

 I_p max. 2,4 A
typ. 2 A

Remark

There are several terminals on the connectors which act as inputs or outputs depending on the mode in which the MM11 is operating (see below). These terminals are described under "Input data" and "Output data".

terminal	operation mode		
	WIM	WIR	RD
CICM/CICM	output	output	input
ENCM ₁ to ENCM ₄	output	output	input
ABCM ₀ to ABCM ₉	output	output	input
PBMCP ₀ to PBMCP ₁₂	input	output	output

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminations (Fig.1)	
			connector 1	connector 2
ABCM ₀	Address inputs (RD mode).	1 TTL		a20, c20
ABCM ₁		1 TTL		a21, c21
ABCM ₂		1 TTL		a22, c22
ABCM ₃		1 TTL		a23, c23
ABCM ₄		1 TTL		a24, c24
ABCM ₅		1 TTL		a25, c25
ABCM ₆		1 TTL		a26, c26
ABCM ₇		1 TTL		a27, c27
ABCM ₈		1 TTL		a28, c28
ABCM ₉		1 TTL		a29, c29
CICM CICM	Cycle initiate signal; bipolar to reduce noise sensitivity (RD mode).	2 TTL 2 TTL		a19, c19 a18, c18
ENCM ₁ ENCM ₂ ENCM ₃ ENCM ₄	Enable inputs; memory is enabled when ENCM is HIGH (RD mode).	2 TTL 2 TTL 2 TTL 2 TTL	a1 a2 a3 a4	
PBMCP ₀ PBMCP ₁ PBMCP ₂ PBMCP ₃ PBMCP ₄ PBMCP ₅	Data inputs for data to be programmed into the EPROMs (WIM mode).	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL		a2, c2 a3, c3 a4, c4 a5, c5 a6, c6 a7, c7

input	function	load	terminations (Fig.1)	
			connector 1	connector 2
PBMCP ₆ PBMCP ₇ PBMCP ₈ PBMCP ₉ PBMCP ₁₀ PBMCP ₁₁ PBMCP ₁₂	Data inputs for data to be programmed into the EPROMs (WIM mode).	1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL 1 TTL		a8, c8 a9, c9 a10, c10 a11, c11 a12, c12 a13, c13 a14, c14
START	Input to start the WIM or the WIR mode (active LOW).	2 TTL	a24	
REST	Input to restart the stopped WIM or WIR mode (active LOW)	1 TTL	a19	
INH	Inhibit and stop input; when LOW the start input is inoperative.	2 TTL	a25	
MSI ₁ MSI ₂	Mode selection inputs.	6 TTL 6 TTL	a26 a27	

Operation mode truth table

mode	mode selection inputs	
	MSI ₁	MSI ₂
RD	HIGH (floating)	HIGH (floating)
WIM	active LOW	arbitrary level
WIR	HIGH (floating)	active LOW

Output data

All outputs meet the standard TTL specifications.

output	function	loadability	terminations (Fig.1)	
			connector 1	connector 2
PBMCP ₀	Program word bits to central processor (RD mode) or MM10 (WIR mode).	10 TTL		a2, c2
PBMCP ₁		10 TTL		a3, c3
PBMCP ₂		10 TTL		a4, c4
PBMCP ₃		10 TTL		a5, c5
PBMCP ₄		10 TTL		a6, c6
PBMCP ₅		10 TTL		a7, c7
PBMCP ₆		10 TTL		a8, c8
PBMCP ₇		10 TTL		a9, c9
PBMCP ₈		10 TTL		a10, c10
PBMCP ₉		10 TTL		a11, c11
PBMCP ₁₀		10 TTL		a12, c12
PBMCP ₁₁		10 TTL		a13, c13
PBMCP ₁₂		10 TTL		a14, c14
ABCM ₀	Address bits to MM10, MM11 or MM12 (WIM mode) or to MM10 (WIR mode).	10 TTL		a20, c20
ABCM ₁		10 TTL		a21, c21
ABCM ₂		10 TTL		a22, c22
ABCM ₃		10 TTL		a23, c23
ABCM ₄		10 TTL		a24, c24
ABCM ₅		10 TTL		a25, c25
ABCM ₆		10 TTL		a26, c26
ABCM ₇		10 TTL		a27, c27
ABCM ₈		10 TTL		a28, c28
ABCM ₉		10 TTL		a29, c29
CICM	Cycle initiate signal to MM10 or MM11 (WIM mode) or to MM10 (WIR mode).	9 TTL		a19, c19
CICM		9 TTL		a18, c18
SCCM	Read-write output (three-state) to MM10. The output is LOW in the WIM mode, HIGH in the WIR mode, floating in the RD mode.	10 TTL		a17, c17
ENCM ₁	Enable signal to MM10, MM11 or MM12 (WIM mode) or to MM10 (WIR mode).	9 TTL	a1	
ENCM ₂		9 TTL	a2	
ENCM ₃		9 TTL	a3	
ENCM ₄		9 TTL	a4	
PRB	Program busy output signal to external equipment. When LOW it indicates that WIM mode or WIR mode is active and becomes HIGH as soon as these actions are finished.	10 TTL	a23	

output	function	loadability	terminations (Fig.1)	
			connector 1	connector 2
PBPM ₀	Program word bits to MM10 (WIR mode). These three-state outputs are only active in the WIR mode.	10 TTL	c1	
PBPM ₁		10 TTL	c2	
PBPM ₂		10 TTL	c3	
PBPM ₃		10 TTL	c4	
PBPM ₄		10 TTL	c5	
PBPM ₅		10 TTL	c6	
PBPM ₆		10 TTL	c7	
PBPM ₇		10 TTL	c8	
PBPM ₈		10 TTL	c9	
PBPM ₉		10 TTL	c10	
PBPM ₁₀		10 TTL	c11	
PBPM ₁₁		10 TTL	c12	
PBPM ₁₂		10 TTL	c13	

Time data*RD mode*

Time between leading edges of $\overline{\text{CICM}}$ / $\overline{\text{CICM}}$ and data valid
PBMCP₀ to PBMCP₁₂

max. 550 ns

Time between address changes on ABCM₀ to ABCM₉ and
leading edges of $\overline{\text{CICM}}$ / $\overline{\text{CICM}}$

min. 0 ns

WIM mode

Time to program 1k or 2k EPROM memory

max. 18 min
typ. 15 min

WIR mode

Time to read-out MM11 and store into MM10

max. 4,2 s
typ. 3,5 s

MECHANICAL DATA

Outlines

Dimensions in mm

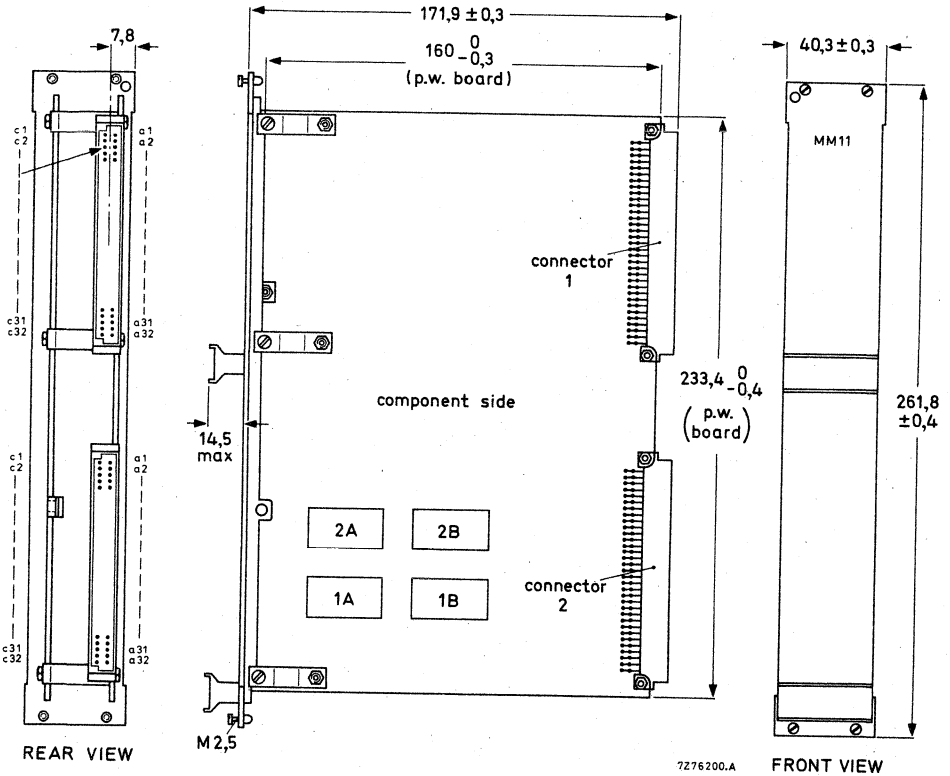


Fig. 1.

Mass 350 g

Terminal location

connector 1		connector 2			
row c	row a	row c	row a	row c	row a
PBPM ₀	1	ENCM ₁	n.c.	1	n.c.
PBPM ₁	2	ENCM ₂	PBMCP ₀	2	PBMCP ₀ (O _{5A} *)
PBPM ₂	3	ENCM ₃	PBMCP ₁	3	PBMCP ₁ (O _{6A})
PBPM ₃	4	ENCM ₄	PBMCP ₂	4	PBMCP ₂ (O _{7A})
PBPM ₄	5	n.c.	PBMCP ₃	5	PBMCP ₃ (O _{8A})
PBPM ₅	6	n.c.	PBMCP ₄	6	PBMCP ₄ (O _{1B})
PBPM ₆	7	n.c.	PBMCP ₅	7	PBMCP ₅ (O _{2B})
PBPM ₇	8	n.c.	PBMCP ₆	8	PBMCP ₆ (O _{3B})
PBPM ₈	9	n.c.	PBMCP ₇	9	PBMCP ₇ (O _{5B})
PBPM ₉	10	n.c.	PBMCP ₈	10	PBMCP ₈ (O _{6B})
PBPM ₁₀	11	n.c.	PBMCP ₉	11	PBMCP ₉ (O _{7B})
PBPM ₁₁	12	n.c.	PBMCP ₁₀	12	PBMCP ₁₀ (O _{1A})
PBPM ₁₂	13	n.c.	PBMCP ₁₁	13	PBMCP ₁₁ (O _{2A})
n.c.	14	n.c.	PBMCP ₁₂	14	PBMCP ₁₂ (O _{3A})
n.c.	15	n.c.	n.c.	15	n.c.
n.c.	16	n.c.	n.c.	16	n.c.
n.c.	17	n.c.	SCCM	17	SCCM
n.c.	18	n.c.	CICM	18	CICM
n.c.	19	REST	CICM	19	CICM
n.c.	20	n.c.	ABCM ₀	20	ABCM ₀
n.c.	21	n.c.	ABCM ₁	21	ABCM ₁
n.c.	22	n.c.	ABCM ₂	22	ABCM ₂
n.c.	23	PRB	ABCM ₃	23	ABCM ₃
n.c.	24	START	ABCM ₄	24	ABCM ₄
n.c.	25	INH	ABCM ₅	25	ABCM ₅
n.c.	26	MSI ₁	ABCM ₆	26	ABCM ₆
n.c.	27	MSI ₂	ABCM ₇	27	ABCM ₇
n.c.	28	n.c.	ABCM ₈	28	ABCM ₈
n.c.	29	n.c.	ABCM ₉	29	ABCM ₉
n.c.	30	n.c.	n.c.	30	n.c.
V _p	31	V _p	V _p	31	V _p
0 V	32	0 V	0 V	32	0 V

n.c. = not connected

* Corresponding output number of EPROM.

MEMORY MODULE

DESCRIPTION

The memory module MM12 is intended for use in the PLC system as a program memory. It contains 4 IC sockets in which 4 UV-erasable PROMs (2708) can be plugged. The MM12 also contains 10 buffered address inputs, 4 enable inputs, 16 buffered outputs and 2 d.c./d.c. converters (5 V to 12 V and 5 V to -5 V).

The MM12 has a capacity of 2k16. Although the PLC system operates with program words of 13 bits, the remaining 3 bits are also brought out (Q_{4A}, Q_{4B}, Q_{8B}), so that the module can be used in other applications which require 16 bits.

The enable input ENCM₁ or ENCM₃ (addresses 0000 to 1777 and 4000 to 5777 respectively) corresponds with the EPROMs in sockets 1A and 1B. The enable input ENCM₂ or ENCM₄ (addresses 2000 to 3777 and 6000 to 7777 respectively) corresponds with the EPROMs in sockets 2A and 2B. This means that one program word is stored into 2 EPROMs, A and B, of which EPROMs A contain the instruction and the most significant digit of the address (address part of the program word), and EPROMs B contain the remaining two digits.

Programming of the EPROMs cannot be done on the MM12: this has to be done on the MM11 or by existing programming equipment.

The MM12 is supplied with two empty EPROMs 2708.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)

V_p 5 V ± 5%

Supply current

I_p max. 1,2 A
typ. 1 A

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminations (Fig. 2)	
			connector 1	connector 2
ABCM ₀	Address bits from central processor	1 TTL		a20, c20
ABCM ₁		1 TTL		a21, c21
ABCM ₂		1 TTL		a22, c22
ABCM ₃		1 TTL		a23, c23
ABCM ₄		1 TTL		a24, c24
ABCM ₅		1 TTL		a25, c25
ABCM ₆		1 TTL		a26, c26
ABCM ₇		1 TTL		a27, c27
ABCM ₈		1 TTL		a28, c28
ABCM ₉		1 TTL		a29, c29
ENCM ₁	Enable inputs from central processor	1 TTL	a1	
ENCM ₂		1 TTL	a2	
ENCM ₃		1 TTL	a3	
ENCM ₄		1 TTL	a4	

Output data

All outputs are three-state outputs and meet the standard TTL specifications.

output	function	loadability	terminations (Fig. 2)	
			connector 1	connector 2
PBMCP ₀	Program word bits from memory module to central processor	10 TTL		a2, c2
PBMCP ₁		10 TTL		a3, c3
PBMCP ₂		10 TTL		a4, c4
PBMCP ₃		10 TTL		a5, c5
PBMCP ₄		10 TTL		a6, c6
PBMCP ₅		10 TTL		a7, c7
PBMCP ₆		10 TTL		a8, c8
PBMCP ₇		10 TTL		a9, c9
PBMCP ₈		10 TTL		a10, c10
PBMCP ₉		10 TTL		a11, c11
PBMCP ₁₀		10 TTL		a12, c12
PBMCP ₁₁		10 TTL		a13, c13
PBMCP ₁₂		10 TTL		a14, c14
Q4A	Buffered output from output O4 of EPROM A.	10 TTL		a1, c1
Q4B	Buffered output from output O4 of EPROM B.	10 TTL		a15, c15
Q8B	Buffered output from output O8 of EPROM B.	10 TTL		a16, c16

Time data

The relationship between the different input and output signals are given when the memory module is operating in the PLC system.

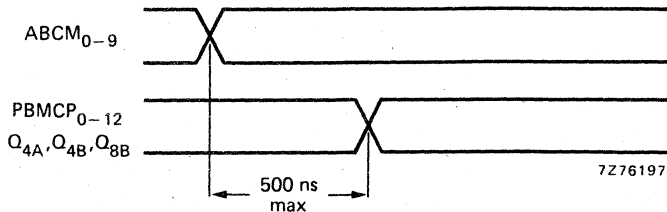


Fig. 1.

MECHANICAL DATA
Outlines

Dimensions in mm

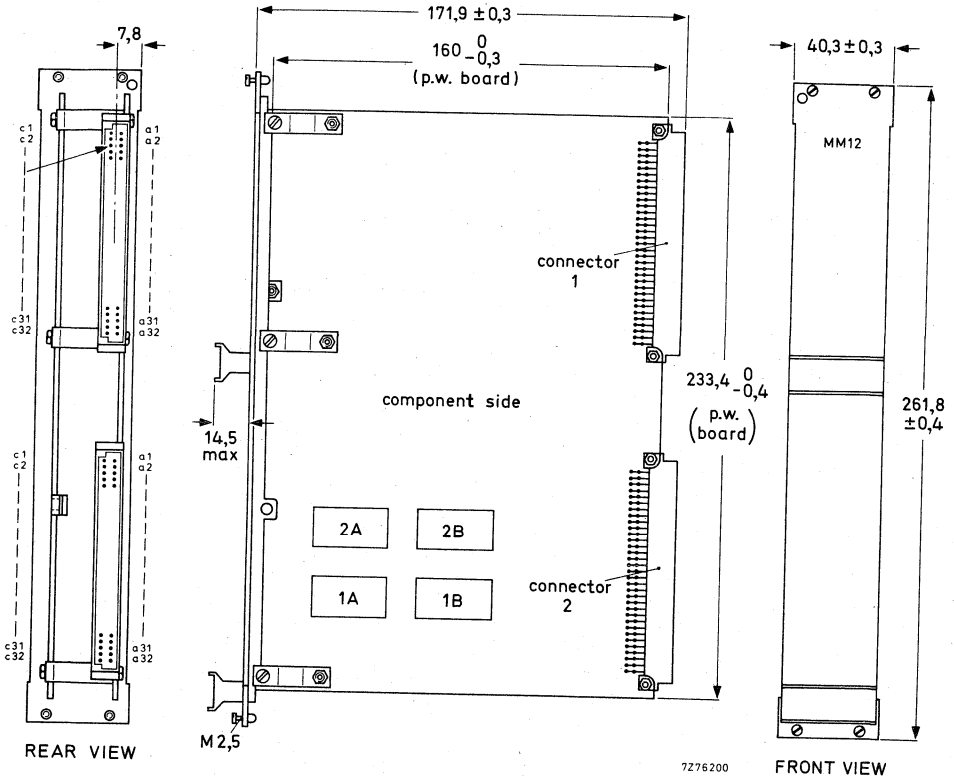


Fig. 2.

Mass 290 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
n.c.	1	ENCM ₁	Q _{4A}	1	Q _{4A} (O _{4A} *)
n.c.	2	ENCM ₂	PBMCP ₀	2	PBMCP ₀ (O _{5A})
n.c.	3	ENCM ₃	PBMCP ₁	3	PBMCP ₁ (O _{6A})
n.c.	4	ENCM ₄	PBMCP ₂	4	PBMCP ₂ (O _{7A})
n.c.	5	n.c.	PBMCP ₃	5	PBMCP ₃ (O _{8A})
n.c.	6	n.c.	PBMCP ₄	6	PBMCP ₄ (O _{1B})
n.c.	7	n.c.	PBMCP ₅	7	PBMCP ₅ (O _{2B})
n.c.	8	n.c.	PBMCP ₆	8	PBMCP ₆ (O _{3B})
n.c.	9	n.c.	PBMCP ₇	9	PBMCP ₇ (O _{5B})
n.c.	10	n.c.	PBMCP ₈	10	PBMCP ₈ (O _{6B})
n.c.	11	n.c.	PBMCP ₉	11	PBMCP ₉ (O _{7B})
n.c.	12	n.c.	PBMCP ₁₀	12	PBMCP ₁₀ (O _{1A})
n.c.	13	n.c.	PBMCP ₁₁	13	PBMCP ₁₁ (O _{2A})
n.c.	14	n.c.	PBMCP ₁₂	14	PBMCP ₁₂ (O _{3A})
n.c.	15	n.c.	Q _{4B}	15	Q _{4B} (O _{4B})
n.c.	16	n.c.	Q _{8B}	16	Q _{8B} (O _{8B})
n.c.	17	n.c.	n.c.	17	n.c.
n.c.	18	n.c.	n.c.	18	n.c.
n.c.	19	n.c.	n.c.	19	n.c.
n.c.	20	n.c.	ABCM ₀	20	ABCM ₀
n.c.	21	n.c.	ABCM ₁	21	ABCM ₁
n.c.	22	n.c.	ABCM ₂	22	ABCM ₂
n.c.	23	n.c.	ABCM ₃	23	ABCM ₃
n.c.	24	n.c.	ABCM ₄	24	ABCM ₄
n.c.	25	n.c.	ABCM ₅	25	ABCM ₅
n.c.	26	n.c.	ABCM ₆	26	ABCM ₆
n.c.	27	n.c.	ABCM ₇	27	ABCM ₇
n.c.	28	n.c.	ABCM ₈	28	ABCM ₈
n.c.	29	n.c.	ABCM ₉	29	ABCM ₉
n.c.	30	n.c.	n.c.	30	n.c.
V _p	31	V _p	V _p	31	V _p
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.

* Corresponding output number of EPROM.

OUTPUT MODULE

DESCRIPTION

The output module is intended for use in combination with the central processor CP10 (or CP11), input module IM10 (or IM11 or LX10), memory module MM10 (or MM11 or MM12) and programming unit PU10 to assemble a programmable logic controller (PLC).

The output module contains 16 addressable output stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All outputs are floating with respect to each other.

Each output stage has a suppressor diode, to allow it to switch inductive loads.

Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

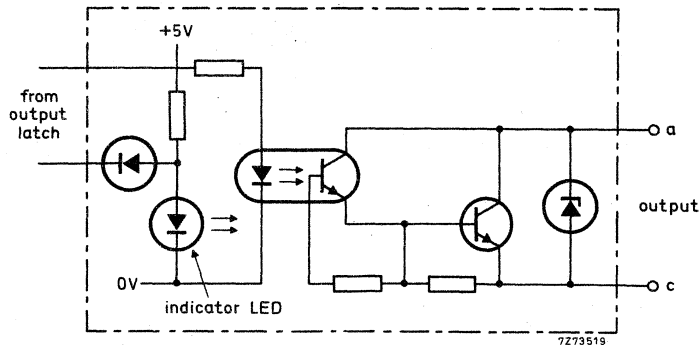


Fig. 1. Circuit diagram of an output stage.

The output module has nine address inputs ($ABCIO_{0-8}$) and five module identification inputs (MID_{0-4}), which are accessible on the connectors at the rear (Fig. 2).

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (Euro-card system). The board is provided with two F068-1 connectors (board parts); the corresponding panel parts are available under catalogue number 2422 025 89291 (pins for wire wrap), 2422 025 89299 (pins for dip soldering) or 2422 025 89327 (solder tags) ¹⁾.

¹⁾ For a general description of the Euro-card system see IEC297 or DIN41494 for 19-in racks and IEC 130-14 or DIN41612 for connectors.

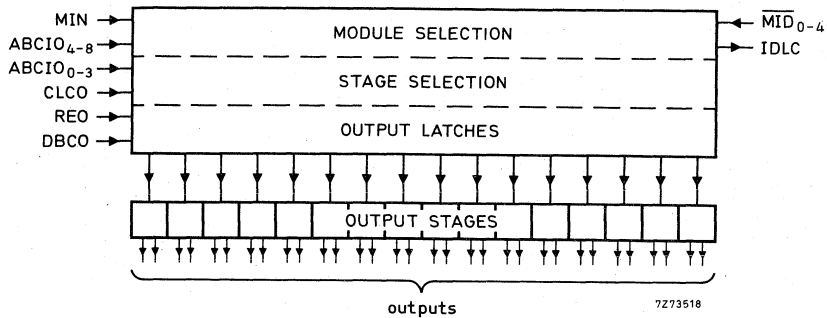


Fig. 2. Block diagram of the output module.

ELECTRICAL DATA

Supply

Supply voltage (d. c.)	V_p	$5\text{ V} \pm 5\%$
current	I_p	max. 1 A (all stages "ON") typ. 0,75 A (8 stages "ON", 8 stages "OFF")

Input data

All inputs meet the standard TTL specification except the CLCO-input.

input	function	load	terminations of connector 1 (Fig. 3)
ABCIO ₀ ABCIO ₁ ABCIO ₂ ABCIO ₃ ABCIO ₄ ABCIO ₅ ABCIO ₆ ABCIO ₇ ABCIO ₈	Address bits from central processor; ABCIO ₀₋₃ select the output stage, ABCIO ₄₋₈ select the output module.	1 TTL	a2, c2
1 TTL		a4, c4	
1 TTL		a6, c6	
1 TTL		a8, c8	
1 TTL		a10	
1 TTL		a12	
1 TTL		a14	
1 TTL		a16	
1 TTL		a18	
DBCO	Data bit from central processor; data is stored in output stage by CLCO.	1 TTL	a22
MIN	Module inhibit signal from external source; a low level applied to this input inhibits data on DBCO to be stored in the output stage.	2 TTL	c26
REO	Reset output module line; a low level on this input will reset all output latches (output transistor non-conducting).	1 TTL	a24
$\overline{\text{MID}}_0$ $\overline{\text{MID}}_1$ $\overline{\text{MID}}_2$ $\overline{\text{MID}}_3$ $\overline{\text{MID}}_4$	Module identification inputs; provide module with individual identity.	2 TTL	c10
2 TTL		c12	
2 TTL		c14	
2 TTL		c16	
2 TTL		c18	
CLCO*	Clock signal from central processor to output module, stores data on DBCO into output stage during input/output cycle.	*	a28

*) Input with relatively high input resistance (typ. 40 k Ω).

CLCO-input, LOW level: max. 1 V;

HIGH level: min. 2, 4 V.

Output data

The data outputs are DO_{XY0} to DO_{XY7} and DO_{XZ0} to DO_{XZ7}. They are accessible on connector 2, see "Terminal location".

Output transistor conducting : output current = max. 100 mA at V_{a-c}^1) = max. 1,5 V

Output transistor non-conducting: output current = max. 10 μ A at V_{a-c}^1) = max. 30 V

Each data output has a suppressor diode, which allows the switching of loads with an inductance of max. 10 H.

¹) Voltage between terminal of row a and terminal of row c of connector 2.

The output (open collector) below meets the standard TTL specifications.

output	function	loadability	terminations of connector 1 (Fig. 3)
IDLC	Identification signal from last output module to central processor (active HIGH); only the IDLC output of the last output module has to be connected with the IDLC input of the central processor.	2 TTL	a26

MECHANICAL DATA

Dimensions in mm

Outlines

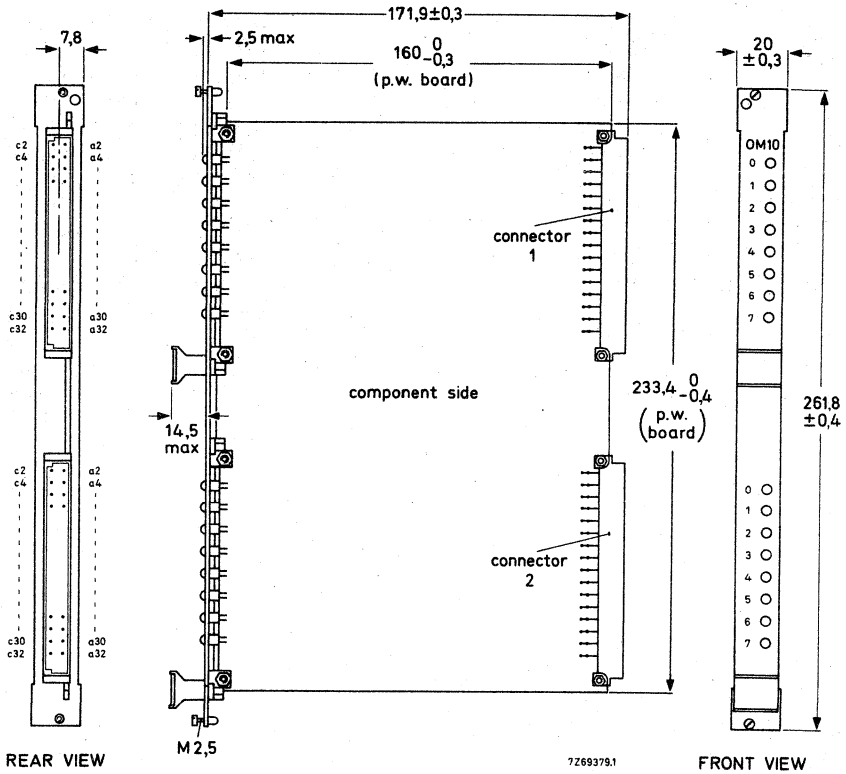


Fig. 3

Mass

230 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
ABCIO ₀	2	ABCIO ₀	DOXY0	2	DOXY0
ABCIO ₁	4	ABCIO ₁	DOXY1	4	DOXY1
ABCIO ₂	6	ABCIO ₂	DOXY2	6	DOXY2
ABCIO ₃	8	ABCIO ₃	DOXY3	8	DOXY3
MID ₀	10	ABCIO ₄	DOXY4	10	DOXY4
MID ₁	12	ABCIO ₅	DOXY5	12	DOXY5
MID ₂	14	ABCIO ₆	DOXY6	14	DOXY6
MID ₃	16	ABCIO ₇	DOXY7	16	DOXY7
MID ₄	18	ABCIO ₈	DOXZ0	18	DOXZ0
0V ¹⁾	20	n. c.	DOXZ1	20	DOXZ1
0V ¹⁾	22	DBCO	DOXZ2	22	DOXZ2
n. c.	24	REO	DOXZ3	24	DOXZ3
MIN	26	IDLC	DOXZ4	26	DOXZ4
0V ²⁾	28	CLCO	DOXZ5	28	DOXZ5
V _p	30	V _p	DOXZ6	30	DOXZ6
0V	32	0V	DOXZ7	32	DOXZ7

n. c. = not connected.

¹⁾ No supply line; only to be used for coding of the MID₀₋₄ lines.

²⁾ No supply line; only to be used as a ground connection for CLCO.

OUTPUT MODULE

DESCRIPTION

The output module is intended for use in combination with the central processor CP10 (or CP11), input module IM10 (or IM11 or LX10), memory module MM10 (or MM11 or MM12) and programming unit PU10 to assemble a programmable logic controller (PLC).

The output module contains 8 addressable output stages, equipped with photocouplers to obtain electrical isolation between external and internal circuitry (Fig. 1). All outputs are open-collector outputs. Each output stage has a suppressor diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages feature electronic short-circuit protection which can only be de-activated by resetting the input signal. Short-circuit indication is provided by the lower row of LEDs on the front panel. If the status indicator LED and the short-circuit indicator LED with the same number are both lit, these output stages are working correctly. If the former LED is lit and the latter extinguished, this will indicate a short-circuit condition.

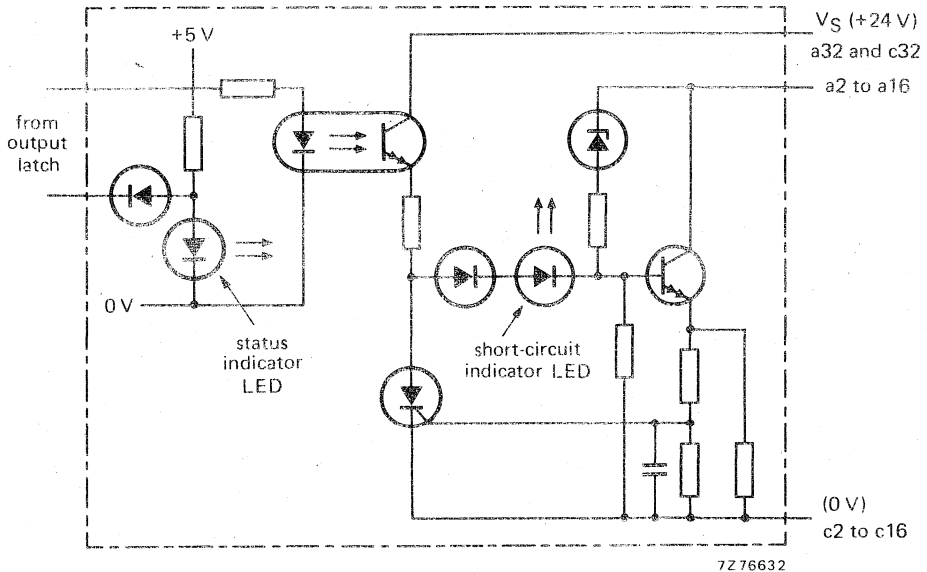


Fig. 1 Circuit diagram of an output stage.

The output module has 9 address inputs ($ABCIO_{0-8}$) and 5 module identification inputs (\overline{MID}_{0-4}) at the rear, for selecting 16 addresses. Because 8 are used as output stages (with even second digit e.g. 162), the remaining 8 addresses can be used as internal places (with odd second digit e.g. 172).

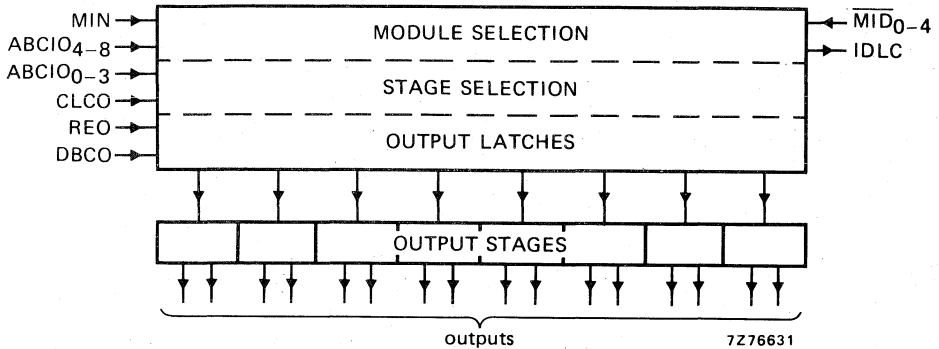


Fig.2 Block diagram of the output module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (Euro-card system). The board is provided with two F068-I connectors (board parts), the corresponding panel parts are available too, but should be ordered additionally: 2422 025 89291 (with wire-wrap pins), 2422 025 89299 (with dip-solder pins), or 2422 025 89327 (with solder tags). For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	} logic	V_p	$5\text{ V} \pm 5\%$
Supply current		I_p	typ 0,75 A
Supply voltage (d.c.)	} for output circuitry	V_S	$24\text{ V} \pm 25\%$
Supply current (excluding load current)		I_S	typ 0,1 A

Input data

All inputs meet the standard TTL specification except the CLCO-input.

input	function	load	terminations of connector 1 (Fig.3)
ABCIO ₀	address bits from central processor; ABCIO ₀₋₃ select the output stage, ABCIO ₄₋₈ select the output module.	1 TTL	a2, c2
ABCIO ₁		1 TTL	a4, c4
ABCIO ₂		1 TTL	a6, c6
ABCIO ₃		1 TTL	a8, c8
ABCIO ₄		1 TTL	a10
ABCIO ₅		1 TTL	a12
ABCIO ₆		1 TTL	a14
ABCIO ₇		1 TTL	a16
ABCIO ₈		1 TTL	a18
DBCO	Data bit from central processor; data are stored in output stage by CLCO.	1 TTL	a22
MIN	Module inhibit signal from external source; a low level applied to this input inhibits data on DBCO to be stored in the output stage.	2 TTL	c26
REO	Reset output module line; a low level on this input will reset all output latches (output transistor non-conducting).	1 TTL	a24
$\overline{\text{MID}}_0$	Module identification inputs; provide module with individual identity.	2 TTL	c10
$\overline{\text{MID}}_1$		2 TTL	c12
$\overline{\text{MID}}_2$		2 TTL	c14
$\overline{\text{MID}}_3$		2 TTL	c16
$\overline{\text{MID}}_4$		2 TTL	c18
CLCO *	Clock signal from central processor to output module, stores data on DBCO into output stage during input/output cycle.	*	a28

* Input with relatively high input resistance (typical 40 kΩ). CLCO-input: LOW level, maximum 1 V;
HIGH level, minimum 2,4 V.

Output data

The data outputs are DO_XY₀ to DO_XY₇ (Y is always even). They are accessible on connector 2, see terminal location.

Output transistor conducting: $V_{a-c}^* = \text{max. } 2,53 \text{ V}$ at output current (I_O) is 2 A.

Output transistor non-conducting: $I_O = \text{max. } 10 \mu\text{A}$ at V_{a-c}^* is 30 V.

Maximum load inductance (L_{max}) see Table 1

Maximum switching frequency at maximum output current ($I_{O\text{max}}$) see Table 2

Table 1

I_O A	L_{max} mH
2,0	50
1,8	60
1,6	80
1,4	100
1,2	140
1,0	200
0,8	310
0,6	560
0,4	1300
0,2	5000
0,1	20000

Table 2

duty cycle %	max. switching frequency Hz
≤ 40	3
≤ 60	2
≤ 80	1
≤ 90	0,5

Output current at operation with forced air cooling of 1 m/s, for all stages

max. 2 A per stage

Output current at operation without forced air cooling

for all stages

max. 0,915 A per stage

for maximum 4 stages

max. 2 A per stage

Short-circuit protection trip level

2,16 A

The output (open collector) meets the standard TTL specifications

output	function	loadability	terminations of connector 1 (Fig.3)
IDLC	Identification signal from last output module to central processor (active HIGH); only the IDLC output of the last output module has to be connected with the IDLC input of the central processor.	2 TTL	a26

* Voltage between terminal of row a and terminal of row c of connector 2.

MECHANICAL DATA

Dimensions in mm

Outlines

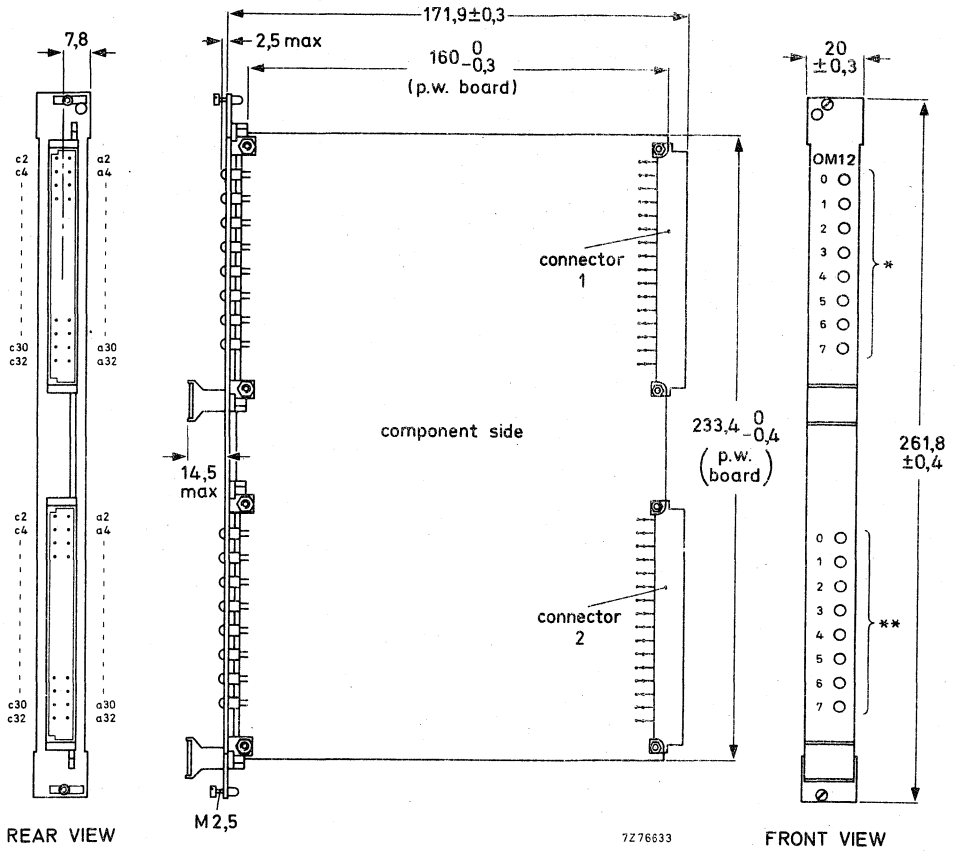


Fig.3 The LEDs identified with * are for status indication, those identified with ** are for short-circuit indication.

Mass 260 g

Terminal location

connector 1			connector 2			
row c		row a	row c		row a	
ABCIO ₀	2	ABCIO ₀	0 V	} (note 3)	2	DOXY ₀
ABCIO ₁	4	ABCIO ₁	0 V		4	DOXY ₁
ABCIO ₂	6	ABCIO ₂	0 V		6	DOXY ₂
ABCIO ₃	8	ABCIO ₃	0 V		8	DOXY ₃
<u>MID</u> ₀	10	ABCIO ₄	0 V		10	DOXY ₄
<u>MID</u> ₁	12	ABCIO ₅	0 V		12	DOXY ₅
<u>MID</u> ₂	14	ABCIO ₆	0 V		14	DOXY ₆
<u>MID</u> ₃	16	ABCIO ₇	0 V		16	DOXY ₇
<u>MID</u> ₄	18	ABCIO ₈	i.c.		18	i.c.
0 V (note 1)	20	n.c.	i.c.		20	i.c.
0 V (note 1)	22	DBCO	i.c.	22	i.c.	
n.c.	24	REO	n.c.	24	n.c.	
MIN	26	IDLC	i.c.	26	n.c.	
0 V (note 2)	28	CLCO	n.c.	28	n.c.	
V _p	30	V _p	n.c.	30	n.c.	
0 V	32	0 V	V _S	32	V _S	

n.c. = not connected.

i.c. = internally connected.

Notes

1. No supply line; only to be used for coding of the MID₀₋₄ lines.
2. No supply line; only to be used as a ground connection for CLCO.
3. 0-line of V_S.

PROGRAMMING UNIT

DESCRIPTION

The programming unit is intended for use in combination with the central processor CP10 (or CP11), input module IM10 (or IM11 or LX10), memory module MM10 (or MM11 or MM12) and output module OM10 (or OM12) to assemble a programmable logic controller (PLC). The control program is written into the program memory with the aid of this unit, by means of the built-in keyboard, or from a punched tape.

The unit can also be used to read the contents of the program memory: eight seven-segments LED displays show the program line number (memory address) and the program word belonging to it. Each program word contains a scratch-pad memory address; the content of this address (1 or 0) is indicated by the status indicator LED.

Programming a system by means of the keyboard (or a punched tape) is only possible when the key switch of the programming unit is set to the on position. The key switch determines the authority of the unit: with a key the user has the complete command of the PLC, without a key he can only monitor its actions.

The keyboard comprises 13 keys (Fig. 3):

- 9 keys, marked 0 to 7 and *, with which the program word is typed in;
- 1 key, marked ENTER; by pressing this key the displayed program word is transferred to the program memory. As soon as the key is released the program memory is set to the read mode; the programming unit reads the contents of the program memory and the program word is again displayed as a check that it is written correctly into the program memory.
- 1 key marked STEP; by pressing this key the next memory address is selected. Each time this key is pressed the line number is incremented by one.
- 1 key, marked CIRC, a repetitive STEP key; by pressing this key the line number is incremented continuously with a frequency of approx. 50 Hz.
- 1 key, marked DECR; by pressing this key simultaneously with either the STEP or CIRC keys, the line number is decremented by one or continuously respectively.

When the key switch is in the off position only the STEP, CIRC and DECR keys are operative. When selecting a particular address by means of these keys, the program word is displayed and the status of the scratch-pad memory address specified in the program word is indicated. In this way the PLC can be monitored without disrupting the working system.

If a punched tape is used, it must be coded according to the ASCII code. The characters to be used for the ENTER and the STEP commands are > and < respectively.

The unit is so constructed that it can be plugged into the PLC; after loading the program into the memory module the PU10 can be removed to be used in another PLC system.

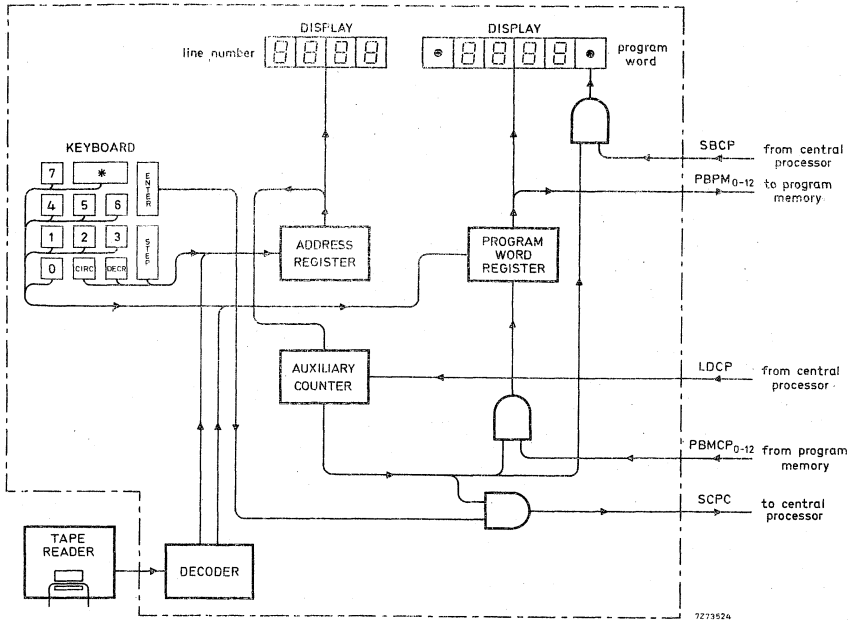


Fig. 1. Simplified block diagram of the programming unit.

The circuit is built on two epoxy-glass printed-wiring boards, mounted in a metal housing, which fits into the Euro-card system. The unit is provided with two F068-I connectors (board parts); the corresponding panel parts are available under catalogue number 2422 025 89291 (pins for wire wrap), 2422 025 89299 (pins for dip soldering) or 2422 025 89327 (solder tags) ¹⁾.

¹⁾ For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATASupply

Supply voltage (d. c.)
current

V_p 5 V \pm 5%
 I_p max. 2 A
typ. 1,8 A

Input data

All inputs meet the standard TTL specifications.

input	function	load	terminations (Fig. 2)	
			connector 1	connector 2
PBMCP ₀	Program word bits from program memory.	1 TTL		c2
PBMCP ₁		1 TTL		a2
PBMCP ₂		1 TTL		c4
PBMCP ₃		1 TTL		a4
PBMCP ₄		1 TTL		c6
PBMCP ₅		1 TTL		a6
PBMCP ₆		1 TTL		c8
PBMCP ₇		1 TTL		a8
PBMCP ₈		1 TTL		c10
PBMCP ₉		1 TTL		a10
PBMCP ₁₀		1 TTL		c12
PBMCP ₁₁		1 TTL		a12
PBMCP ₁₂		1 TTL		c14
LDCP	Synchronization input from central processor; synchronizes auxiliary address counter in programming unit with address counter in central processor.	1 TTL	a14	
$\overline{CL23}$	Inverted clock input from central processor.	1 TTL		c16
$\phi 57$	Clock signal for status indication from central processor.	1 TTL		c16
SBCP	Status bit from central processor; clocked by $\phi 57$ it indicates state 1 or 0 at selected scratch-pad memory address.	1 TTL	a16	
TB ₁	Tape bits (ASCII code) from tape reader	2 TTL		c18
TB ₂				a18
TB ₃				c20
TB ₄				a20
TB ₅				c22
TB ₆				a22
TB ₇				c24

input	function	load	terminations (Fig. 2)	
			connector 1	connector 2
STROBE	Signal from tape-reader sprocket.	2 TTL	a24	
SLTP	Selection signal from tape reader or external switch; if tape reader is used the input must be connected to the logic LOW level.	2 TTL	c28	

Output data

All outputs meet the standard TTL specifications.

output	function	loadability	terminations (Fig. 2)	
			connector 1	connector 2
PBPM ₀	Program word bits to program memory.	9 TTL	c2	
PBPM ₁		9 TTL	a2	
PBPM ₂		9 TTL	c4	
PBPM ₃		9 TTL	a4	
PBPM ₄		9 TTL	c6	
PBPM ₅		9 TTL	a6	
PBPM ₆		9 TTL	c8	
PBPM ₇		9 TTL	a8	
PBPM ₈		9 TTL	c10	
PBPM ₉		9 TTL	a10	
PBPM ₁₀		9 TTL	c12	
PBPM ₁₁		9 TTL	a12	
PBPM ₁₂		9 TTL	c14	
ABP ₀	Inverted address bits (line number bits to external printer).	10 TTL		c18
ABP ₁		10 TTL		a18
ABP ₂		10 TTL		c20
ABP ₃		10 TTL		a20
ABP ₄		10 TTL		c22
ABP ₅		10 TTL		a22
ABP ₆		10 TTL		c24
ABP ₇		10 TTL		a24
ABP ₈		10 TTL		c26
ABP ₉		10 TTL		a26
ABP ₁₀		10 TTL		c28
ABP ₁₁		10 TTL		a28
READY	Signal indicating that contents of program memory address counter agrees with line number.	10 TTL		a16

output	function	loadability	terminations (Fig. 2)	
			connector 1	connector 2
SCPC	Store command to central processor.	10 TTL		a14
BSP	Busy signal to external tape reader; the output becomes LOW when a correct code has been recognized, and becomes HIGH when this code has been stored.	10 TTL	c26	
$\overline{\text{BSP}}$	Inverted BSP.	10 TTL	a26	

Time data

If a tape reader is used for loading the control program into the program memory the following considerations have to be taken in account.

Delay time between the level changes on TB_{1-7} and strobe signal t_1 min. 0 ns

Delay time between leading edge of strobe pulse and code recognition on BSP t_2 max. 500 ns

Strobe pulse duration t_s min. 2 μs
max. 10 ms

BSP becomes LOW when a correct code has been recognized and HIGH when this code has been stored. At this moment the tape reader can be started to give the next code.

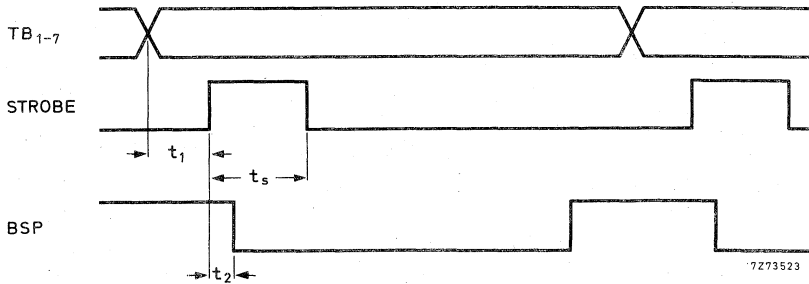
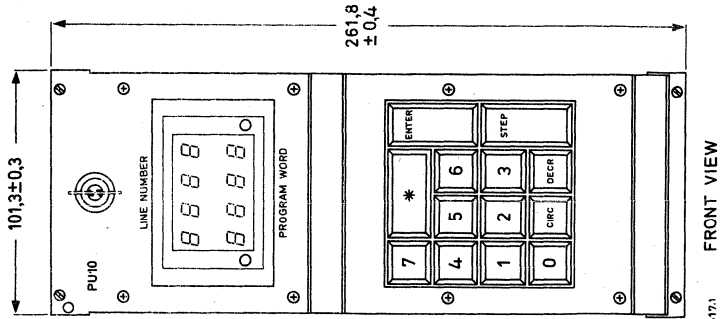
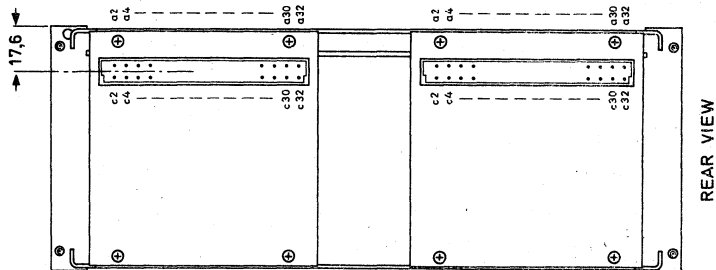
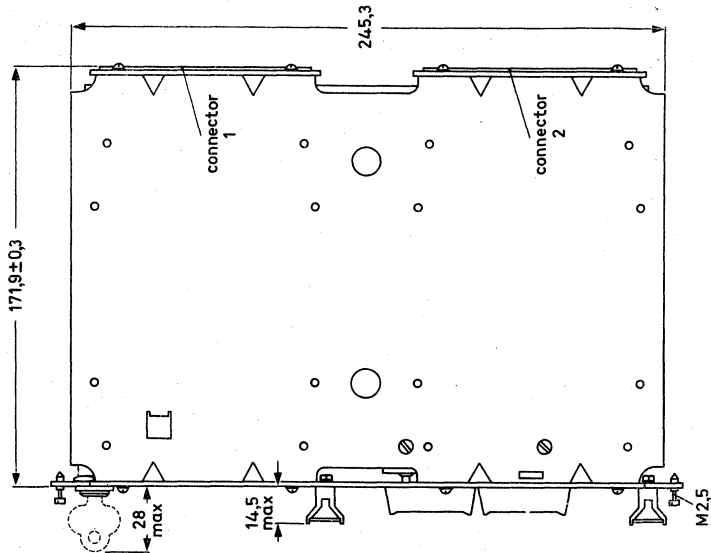


Fig. 2

Dimensions in mm



7273517.1



MECHANICAL DATA

Outlines

Fig. 3

Mass

1140 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
PBPM ₀	2	PBPM ₁	PBMCP ₀	2	PBMCP ₁
PBPM ₂	4	PBPM ₃	PBMCP ₂	4	PBMCP ₃
PBPM ₄	6	PBPM ₅	PBMCP ₄	6	PBMCP ₅
PBPM ₆	8	PBPM ₇	PBMCP ₆	8	PBMCP ₇
PBPM ₈	10	PBPM ₉	PBMCP ₈	10	PBMCP ₉
PBPM ₁₀	12	PBPM ₁₁	PBMCP ₁₀	12	PBMCP ₁₁
PBPM ₁₂	14	LDCP	PBMCP ₁₂	14	SCPC
CL23	16	SBCP	$\phi 57$	16	READY
TB ₁	18	TB ₂	\overline{ABP}_0	18	\overline{ABP}_1
TB ₃	20	TB ₄	\overline{ABP}_2	20	\overline{ABP}_3
TB ₅	22	TB ₆	\overline{ABP}_4	22	\overline{ABP}_5
TB ₇	24	STROBE	\overline{ABP}_6	24	\overline{ABP}_7
BSP	26	\overline{BSP}	\overline{ABP}_8	26	\overline{ABP}_9
SLTP	28	n. c.	\overline{ABP}_{10}	28	\overline{ABP}_{11}
Vp	30	Vp	Vp	30	Vp
0 V	32	0 V	0 V	32	0 V

n. c. = not connected.

BACK PANELS

APPLICATION

Back panels BP11 to BP16 are designed for use as mother boards in 19-inch racks in the PLC system. Use of these panels removes the work of wiring separate connectors to receive the modules. The range avoids system redundancy and allows the rack space to be fully utilized.

DESCRIPTION

The back panels are equipped with female connectors, matching the male counterparts of the PLC modules. They have solder bridges for determining the addresses of an input/output/LX10 module (MID), the addresses of the MM modules (ENCM), the last IM/OM module or cycle time (IDLC), the last MM module (MICC), and connecting blocks for external connections.

Types BP11 to BP14 each consist of two back panels. The upper panel provides the required interconnections for connector 1 of each PLC module. The lower panel provides the interconnections for connector 2 of each MM, PU and CP module (see Figs 1 to 4). External connections are made to the lower connectors of the IM, OM and LX10 modules; these must be received by the separately mounted female connectors.

As the layout of the panels depends on the number of MM modules used, four different types have been developed. Table 1 surveys the various back panels and the type and number of each module which can be placed in the rack. Since a greater number of MM modules generally requires a greater number of IM/OM modules, need will be felt for an extension rack to accommodate these extra modules. Two back panel types are available for this purpose: the BP15 is for 15 IM/OM modules; the BP16 is for 21. These, of course, are only upper back panels.

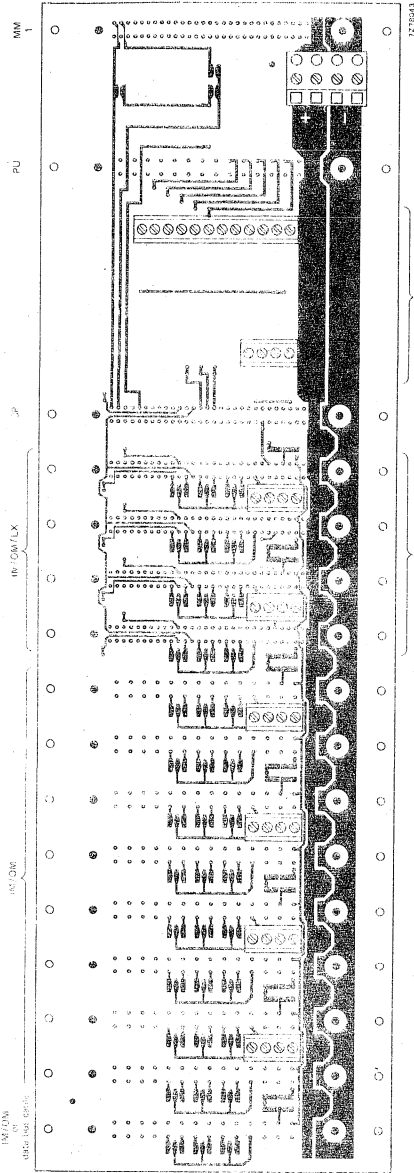
Table 1 Back panels

no. of MM modules	no. of IM/OM/LX* modules	no. of CP modules	no. of PU modules	type of back panel	catalogue number 9390 269
1	13	1	1	BP11	30112
2	11	1	1	BP12	40112
3	9	1	1	BP13	50112
4	7	1	1	BP14	60112
-	15**	-	-	BP15	70112
-	21**	-	-	BP16	80112

The back panels are screwed to the rack by M2,5 screws, using threaded rails and isolation strips.

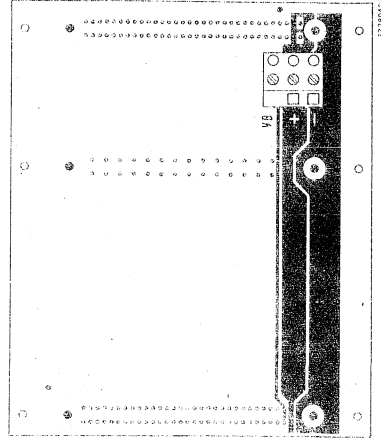
* A maximum of 4 LX modules can be inserted at positions IM/OM1 to IM/OM4. If an extension rack is used, one place in each rack must be reserved for data bus cable, thus the number of modules is one less than the number stated in this column.

** Back panels type BP15 and BP16 are extension panels for use in a second rack to accommodate additional IM/OM modules.



detail Fig.5

detail Fig.7



1271043

Fig. 1 Back panel BP11.

- IM = input module
- OM = output module
- LX = load external interface module
- CP = central processor
- PU = programming unit
- MM = program memory module
- + = +5 V ± 5% supply voltage
- = 0 V
- VB = +4,5 V to +7,5 V (battery voltage)

Data bus cable is only used for connecting a BP15 or BP16 panel.

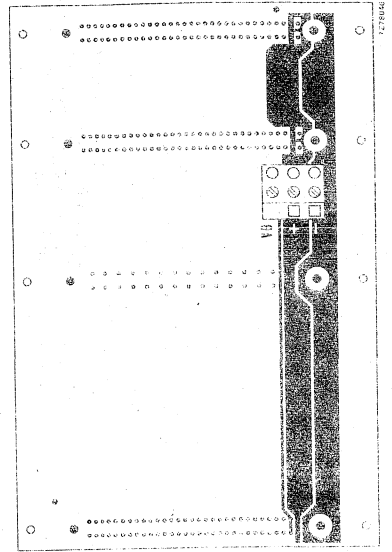
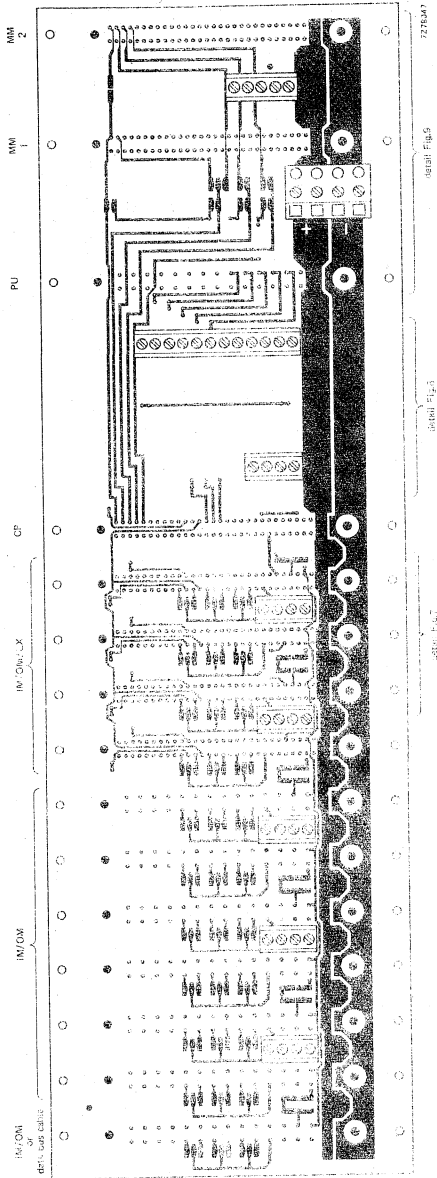


Fig. 2 Back panel BP12.

- IM = input module
- OM = output module
- LX = load external interface module
- CP = central processor
- PU = programming unit
- MM = program memory module
- + = +5 V \pm 5% ; supply voltage
- = 0 V
- V_B = +4.5 V to +7.5 V (battery voltage)

Data bus cable is only used for connecting a BP15 or BP16 panel.

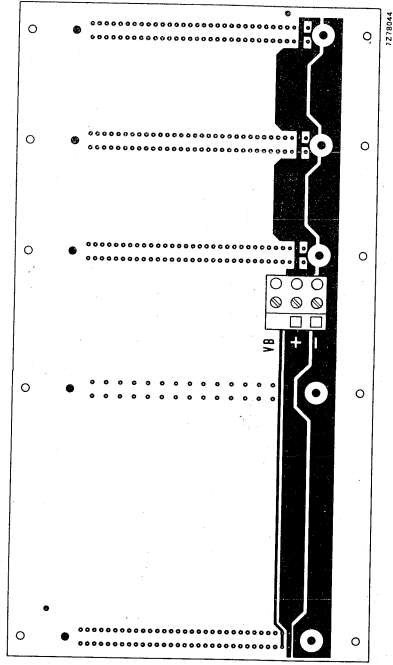
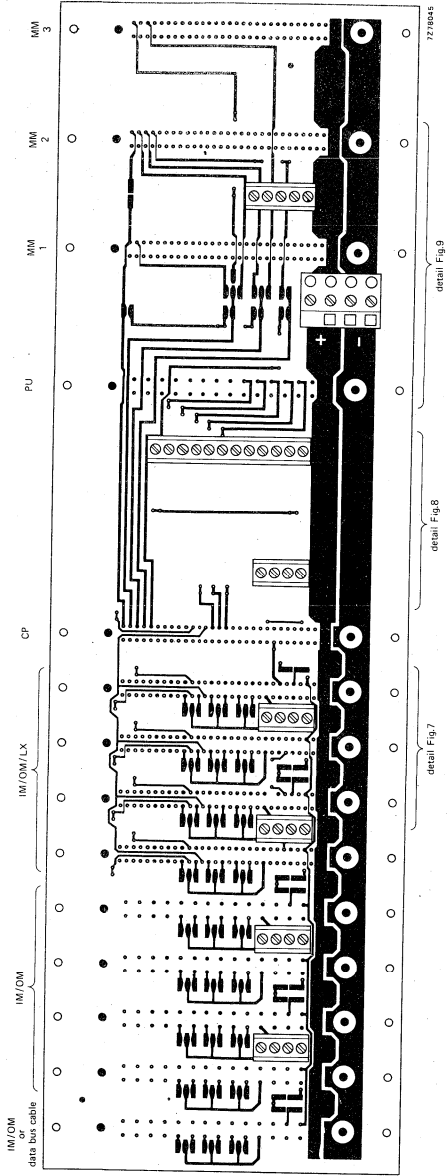


Fig. 3 Back panel BP13.

- IM = input module
- OM = output module
- LX = load external interface module
- CP = central processor
- PU = programming unit
- MM = program memory module
- + = +5 V ± 5% } supply voltage
- = 0
- VB = +4,5 V to +7,5 V (battery voltage)

Data bus cable is only used for connecting a BP15 or BP16 panel.

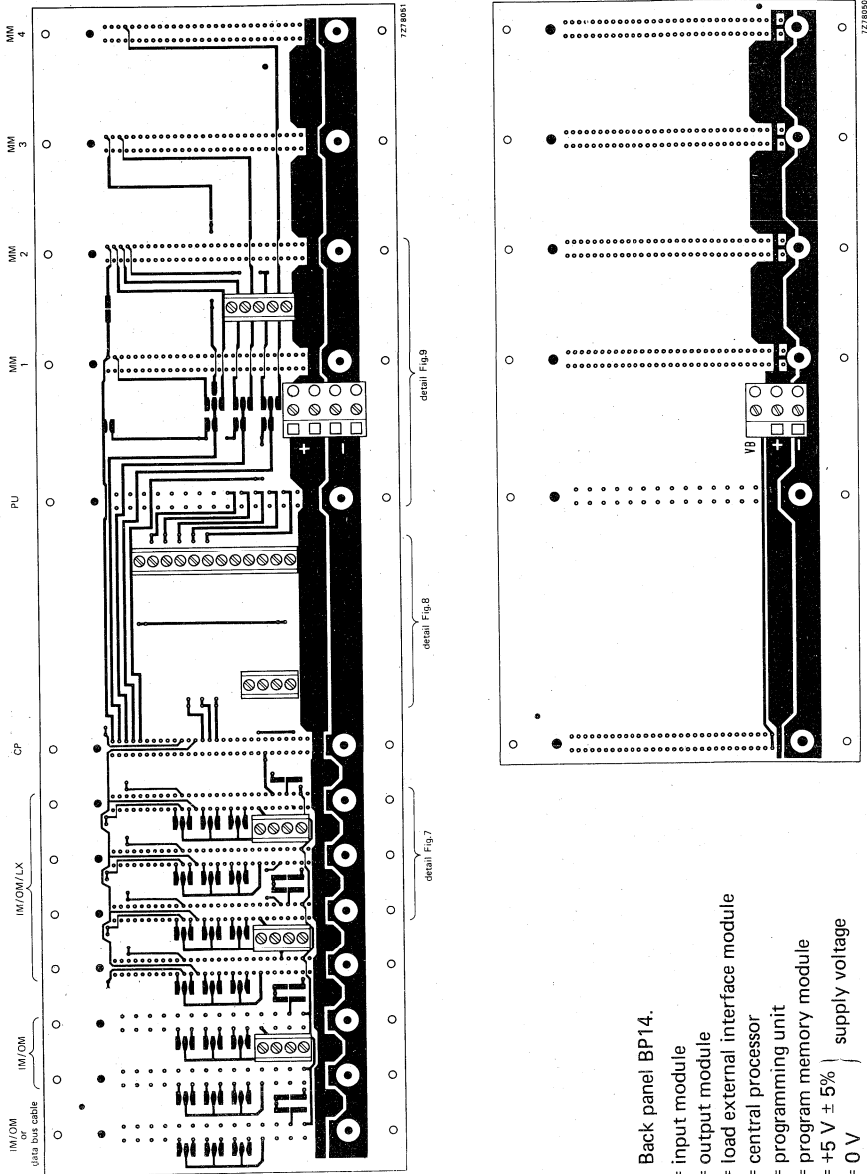


Fig. 4 Back panel BP14.

- IM = input module
- OM = output module
- LX = load external interface module
- CP = central processor
- PU = programming unit
- MM = program memory module
- + = +5 V \pm 5% } supply voltage
- = 0 V
- V_B = +4,5 V to +7,5 V (battery voltage)

Data bus cable is only used for connecting a BP15 or BP16 panel.

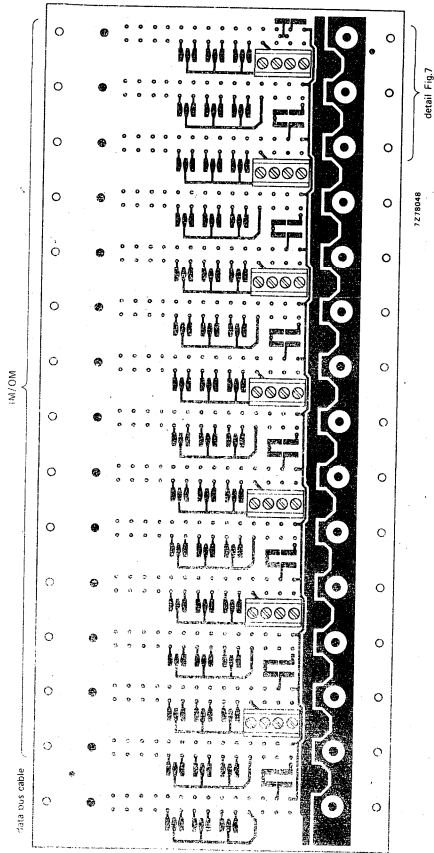


Fig. 5 Back panel BP15.
 IM = input module
 OM = output module

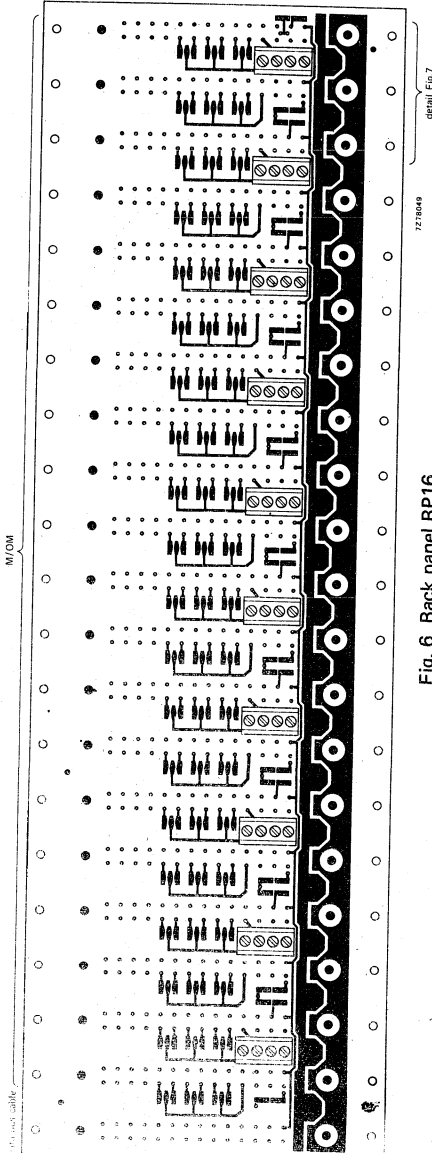


Fig. 6 Back panel BP16.
 IM = input module
 OM = output module

Each of the IM and OM modules has a discrete address so that the central processor can address each in turn during an input/output cycle. This address is formed by bridging the appropriate MID pad ($\overline{\text{MID}}_{0,4}$) and the adjacent 0 V pad (connected to connector 1, pin c22). Table 2 gives the address codes for the IM and OM modules. The $\overline{\text{MID}}_5$ pad is not used.

If no LX modules are used, it is important to assign the $\overline{\text{MID}}$ addresses to the IM and OM modules, so that the spare addresses, if any, are of a higher order than the used addresses. If this is not done, the input/output cycle will take longer than necessary. If no LX modules are inserted, the IDLC pad of the last IM/OM module (the one with the highest address) must be bridged to the adjacent r or n-shaped pad. If output modules are inserted at places IM/OM/LX2 and IM/OM/LX3, for instance, a logic LOW level applied via wires, connected to REO_2 and REO_3 of the connector block between places IM/OM/LX2 and IM/OM/LX1, will reset all the output latches in the relevant modules. Consequently the output transistors are driven in the non-conductive state. A logic LOW (inhibit) applied via wires connected to MIN_1 or MIN_2 of the same connector block, causes data from input modules (IM/LX) inserted at places IM/OM/LX1 or IM/OM/LX2 respectively, to be ignored by the central processor. It also prevents data stored during the preceding input/output cycle in output modules, inserted in the same places, from changing. If one or more LX modules are inserted, pin a25 automatically connects the IDLC line of the central processor to zero (maximum cycle time of 0,924 ms). Removal of all LX modules will affect the 0,924 ms cycle time. As the maximum number of LX modules in any one PLC system is 4, only two MID pads are used for addressing (see Table 3).

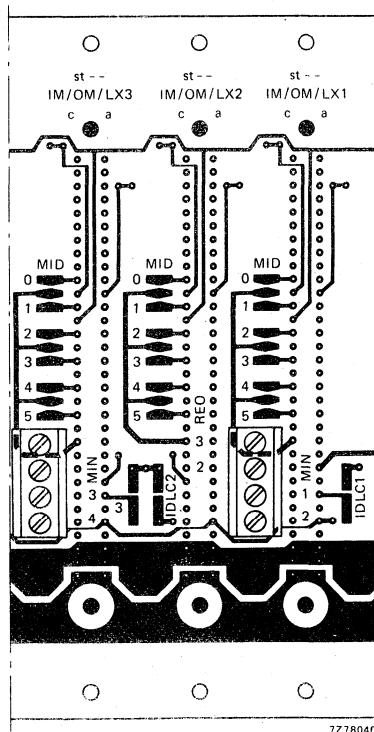


Fig. 7 Detail of back panels BP11 to BP16.
Note: $\overline{\text{MID}}_5$ is normally not used.

Table 2 IM and OM module address codes

\overline{MID}_0	\overline{MID}_1	\overline{MID}_2	\overline{MID}_3	\overline{MID}_4	input/output stage address — scratch-pad locations
—	—	—	—	—	000 to 017
0 V	—	—	—	—	020 to 037
—	0 V	—	—	—	040 to 057
0 V	0 V	—	—	—	060 to 077
—	—	0 V	—	—	100 to 117
0 V	—	0 V	—	—	120 to 137
—	0 V	0 V	—	—	140 to 157
0 V	0 V	0 V	—	—	160 to 177
—	—	—	0 V	—	200 to 217
0 V	—	—	0 V	—	220 to 237
—	0 V	—	0 V	—	240 to 257
0 V	0 V	—	0 V	—	260 to 277
—	—	0 V	0 V	—	300 to 317
0 V	—	0 V	0 V	—	320 to 337
—	0 V	0 V	0 V	—	340 to 357
0 V	0 V	0 V	0 V	—	360 to 377
—	—	—	—	0 V	400 to 417
0 V	—	—	—	0 V	420 to 437
—	0 V	—	—	0 V	440 to 457
0 V	0 V	—	—	0 V	460 to 477
—	—	0 V	—	0 V	500 to 517
0 V	—	0 V	—	0 V	520 to 537
—	0 V	0 V	—	0 V	540 to 557
0 V	0 V	0 V	—	0 V	560 to 577
—	—	—	0 V	0 V	600 to 617
0 V	—	—	0 V	0 V	620 to 637
—	0 V	—	0 V	0 V	640 to 657
0 V	0 V	—	0 V	0 V	660 to 677
—	—	0 V	0 V	0 V	700 to 717
0 V	—	0 V	0 V	0 V	720 to 737
—	0 V	0 V	0 V	0 V	740 to 757
0 V	0 V	0 V	0 V	0 V	760 to 777

Table 3 LX module address codes

\overline{MID}_3	\overline{MID}_4	address of eight-bit data source
—	—	00o to 17o
0 V	—	20o to 37o
—	0 V	40o to 57o
0 V	0 V	60o to 77o

Notes to Tables 2 and 3.

- 0 V indicates that the \overline{MID} terminal is connected to connector 1, pin c22 (0 V).
- indicates that the \overline{MID} terminal is floating.
- The least significant digit of each LX address is always 0, e.g. 00o to 17o in the table signifies addresses 00o, 01o, 02o, 03o etc., up to 17o.

Fig. 8 shows the connector blocks on the back panels BP11 to BP14. The left-hand block contains connections for the REO₁ wire and the MIN wire with the number of the highest IM/OM place (13, 11, 9 or 7). A CLCP wire can be connected to the upper terminal, carrying a disable signal from external source (switch) to central processor (active LOW). The operation of this signal in combination with the SPCE signal, carried by a wire connected to the lower terminal, is given in Table 4.

The right-hand connector block contains the output connection ALARM, which will become LOW when the supply voltage drops below 4,75 V. The tape reader connections TB₁ to TB₇ and STROBE can be connected to the corresponding tape bit outputs of a tape reader. Connection BSP or $\overline{\text{BSP}}$ must then be connected to the start/stop input of the tape reader. Connection SLTP must be switched to 0 V during tape reader programming and left floating during keyboard programming.

Fig. 8 Detail of back panels BP11 to BP14.

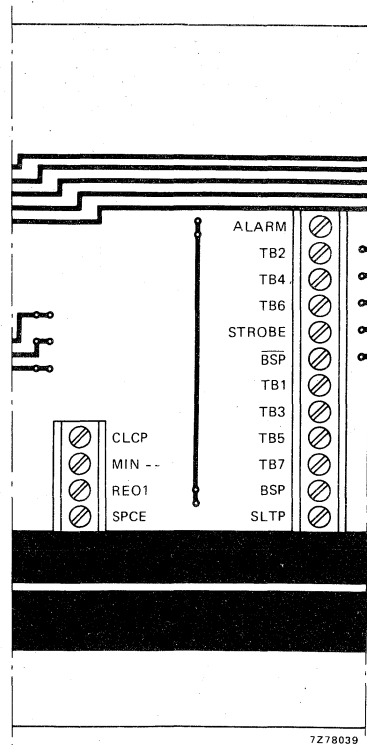


Table 4 Operation of CLCP and SPCE

CLCP	SPCE	operation
0	X*	The central processor is held at the beginning of an input/output cycle.
1	X*	The central processor is running.
0 → 1	1	The central processor starts running at the beginning of an input/output cycle. All scratch-pad locations, except those corresponding to inputs are reset to '0' during the first input/output cycle. All outputs from the PLC output modules are passive after the first input/output cycle.
0 → 1	0	The central processor starts running at the beginning of an input/output cycle. Any data existing in the scratch-pad locations corresponding to outputs determine the state of the output stages in the output modules during the first input/output cycle.

* X indicates either 0 or 1.

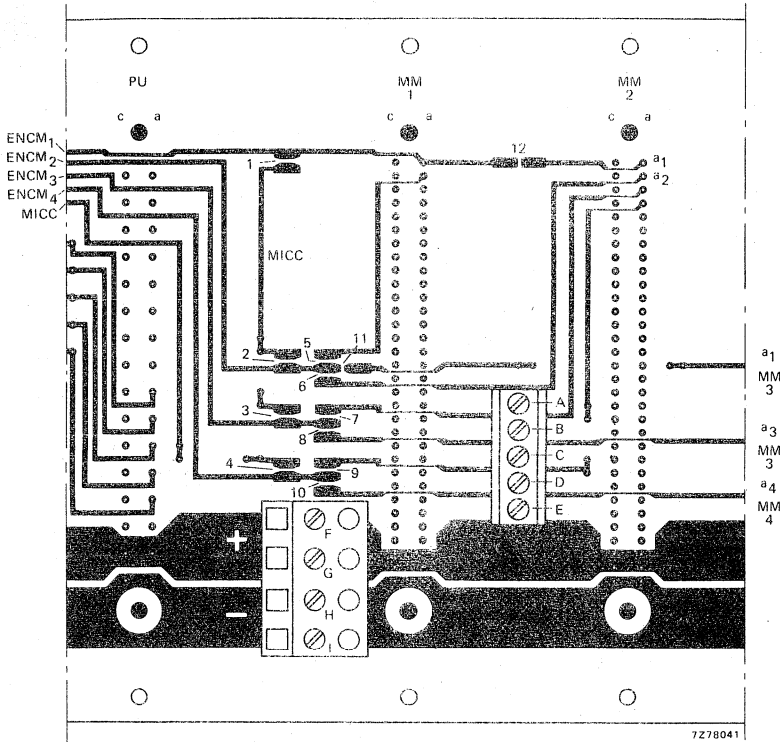


Fig. 9 Detail of back panels BP12 to BP14.

A = PRB; B = START; C = INH; D = MSI₁; E = MSI₂; F = +5 V, ± 5%; G = +5 V, ± 5%; H = 0 V; I = 0 V.

Pads 11 and 12 and connections A to E are used for program copying with the MM11 module.

ENCM₁₋₄ = enable signal from central processor to program memory;


























MICC = memory identification signal derived from MM module in highest position;

PRB = program busy output signal to external equipment;



INH = inhibit input, when LOW the start input is inoperative;

MSI = mode selection inputs (see data sheets MM11).

Table 5 MM module address codes

total byte content	number and type of MM modules	MM module position				pad pairs to be bridged		module position in which a ₁ must be connected with a ₂
		1	2	3	4	MICC	ENCM	
1k	1 MM10					1		
	1 MM12					1		
2k	2 MM10					2	6	
	2 MM12					2	6	1 2
	1 MM12					2	5	
3k	3 MM10					3	6 8	
	3 MM12					3	6 8	1 2 3
	2 MM12					3	5 7 9	
4k	4 MM10					4	6 8 10	
	4 MM12					4	6 8 10	1 2 3 4
	2 MM12					4	5 7 9	

Note

-  = MM12 equipped with 1 k only (PROMs in position 1A and 1B).
-  = MM12 equipped with 2 k.

PC20 MODULES



MODULES FOR PROGRAMMABLE CONTROLLERS

GENERAL

The programmable controller PC20 is used for controlling machines and/or processes. It can be easily programmed and re-programmed.

The modular design of the PC20 enables a user to build a programmable controller which is 'tailor-made' for his control task. By specifying the number and the types of PC20 modules that he requires he only has to purchase the electronic capability he needs.

The PC20 modules are on standard double Eurocards*. Optically isolated interface circuits, specifically designed for an industrial environment, provide excellent noise immunity and a high degree of isolation. The internationally accepted machine signal level of 24 V is used and generous tolerances on operational margins and thresholds ensures good compatibility.

Besides these modules, the PC20 comprises back panels, a frame (19 in rack) and a standard power supply. The frame must conform to IEC 297 or DIN 41494 (for racks) and IEC 130-14 or DIN 41612 (for connectors). The adoption of these standards means that the frame and the power supply (for smaller controllers available as SC20 and SO20 respectively) should be easily obtainable.

The following modules and accessories are available (see also Fig. 1).

type	description	catalogue number
AI20	analogue input module	9360 023 90112
AO20	analogue output module	9360 024 00112
BP22	terminal strip for inputs/outputs in controller cabinet	4322 027 92140
BP23	back panel for Eurorack	4322 027 94010
BP25	back panel for half extension rack	4322 027 94030
BP26	back panel for full extension rack	4322 027 94040
CP20	central processor with program memory (2 k (E) PROM)	4322 027 92040
CP21	central processor with program memory (1 k RAM)	4322 027 92050
CP22	central processor without program memory	4322 027 92060
CP24	central processor with program memory (2 k RAM)	4322 027 94140
FP20	front plate, 15 mm width	4322 027 92150
FP21	front plate, 20 mm width	4322 027 92160
IM20	input module	4322 027 92000
MM20	program memory module (8 k (E) PROM)	4322 027 92070
MM21	program memory module (8 k RAM)	4322 027 92080
MM22	program memory module (4 k RAM)	4322 027 94160
OM20	output module (0,5 A)	4322 027 92010
OM21	output module (2 A)	4322 027 92020
PU20	programming unit	4322 027 92090
PU21	programming unit interface	4322 027 92100
RP20	bidirectional parallel interface	4322 027 92170
RS20	bidirectional serial interface	4322 027 92180
SC20	small controller cabinet	4322 027 92110
SO20	supply and output module (0,5 A)	4322 027 92030
VI20	bidirectional RS449/423 interface	4322 027 92200

* Except programming unit PU20, which is a desk top apparatus.

Figure 1 shows, in a simplified form, the function of each of the PC20 modules. In operation the PC20 cycles continuously through a data input/output cycle and a data processing cycle.

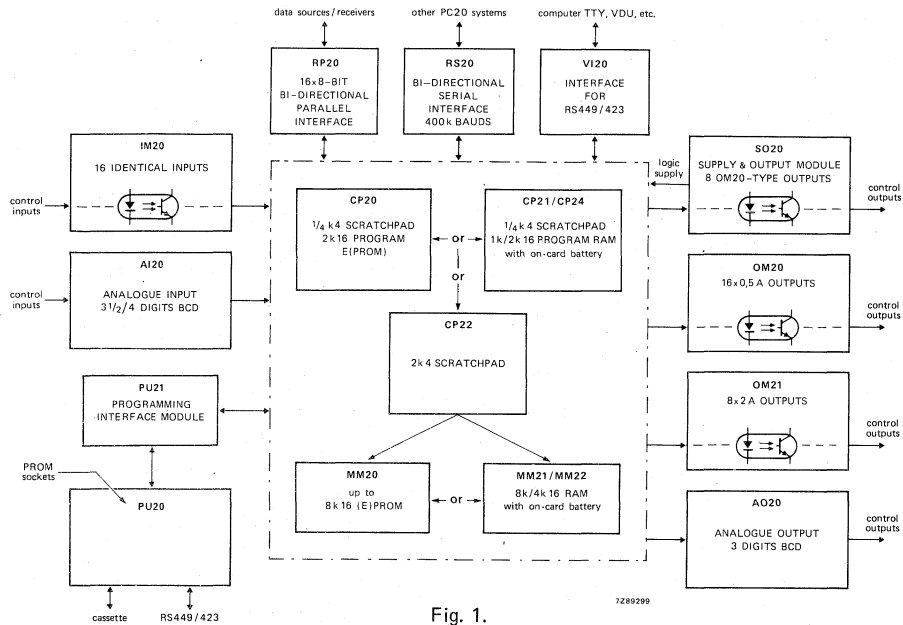


Fig. 1.

The input module converts the signals from the plant into a binary form acceptable to the central processor.

The central processor reads the data from the input module, performs logic equations on it in accordance with the program instructions and transfers the results to the output module.

The output module converts the binary data from the central processor to electrical signals suitable for the control of the plant.

The program memory is the store in which the set of instruction that compose the program are stored. These instructions dictate the actions which must be taken in response to the condition of each input.

The programming unit PU20 is the means by which an operator can write a program, or changes to a program, into the program memory. The unit is a portable desk-top apparatus so that only one is required to serve any number of PC20 systems. It is connected to the PC20 system via the programming unit interface PU21, which is not too expensive to leave in the PC20 system.

GENERAL CHARACTERISTICS

Operating temperature range	0 to +60 °C (0 to +45 °C*)
Storage temperature range	-40 to +70 °C
Dimensions	160 mm x 233 mm (double Eurocard) according to IEC 297 or DIN 41494 **
Supply voltage (d.c.)	$V_p = 10\text{ V} \pm 10\%$; $24\text{ V} \pm 25\%$ **
Number of input + output signals	2000
Maximum program length	8 k instructions
Cycle time	1 ms for a typical program of 1 k instructions

TESTS AND REQUIREMENTS

All modules are designed to meet the tests below.

Vibration test

IEC 68-2, test method Fc: 5 to 55 Hz, amplitude 0,75 mm (0,35 mm*) or 5g (whichever is less).

Shock test

IEC 68-2, test method Ea: 3 shocks in 6 directions, pulse duration 11 ms, peak acceleration 50g (30g*)

Rapid change of temperature test

IEC 68-2, test method Na: 5 cycles of 2 h at -40 °C and 2 h at +85 °C.

Damp heat test

IEC 68-2, test method Ca; 21 days at 40 °C, R.H. 90 to 95%.

* Valid for PU20.

** For PU20 see the relevant data sheet.

CENTRAL PROCESSOR

DESCRIPTION

The central processor CP20 is for use with other PC20 modules, to assemble a programmable controller.

The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates clock pulses for the controller.

The central processor block diagram is given in Fig. 1. The *data processor* controls the system and the complete timing. It includes the instruction decoder, the 1-bit logic processor, the 4-bit arithmetic processor and the data control.

The *address processor* generates addresses for the program memory under program control. It also generates addresses for the input and output modules.

The *program memory* consists of 2 EPROMs 2716 (2k), for which 2 sockets (A and B, Fig. 3) are provided. The system operates with program words of 16 bits, which are distributed over 2 EPROMs.

The capacity of the *scratchpad memory* is $\frac{1}{4}k4$. Depending on the instruction, the scratchpad memory can be addressed word by word (addresses run from 000 to 255) or bit by bit (addresses run from 000.0 to 255.3). In the latter case the address notation is, for example, 147.2 or 076.0. The CP20 has no on-board battery back-up; provisions for an external battery for data retention in the scratchpad memory are present.

The *UDC-circuit* (Up-Date and Check) controls the switch-on/off procedure; it informs the system of power failures. It also controls the access of the programming unit to the system memories.

The *reset scratchpad memory circuit* allows the central processor to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after switch-on of the system.

The *timer clock circuit* provides 5 crystal-controlled timer clocks: 10 ms, 100 ms, 1 s, 10 s, 1 min (50% duty factor).



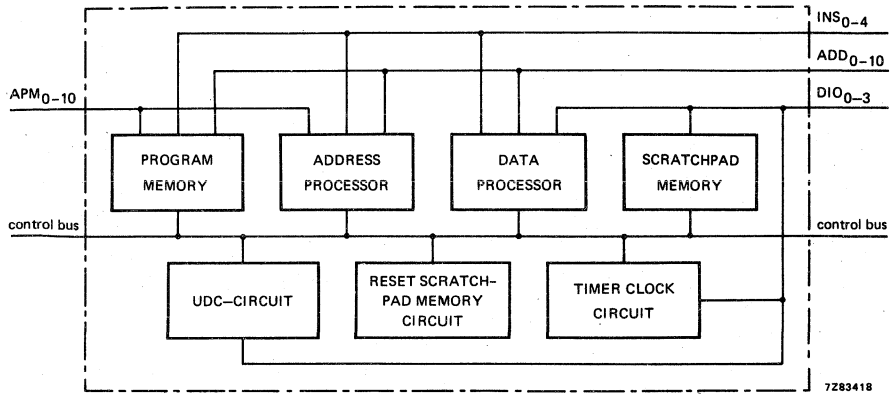


Fig. 1 Block diagram.

Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs PHC_0 and PHC_1 , are:

- up-date and check phase (UDC): $PHC_0 = 0$, $PHC_1 = 0$;
- reset scratchpad memory (RSM): $PHC_0 = 1$, $PHC_1 = 0$;
- data processing (DP): $PHC_0 = 0$; $PHC_1 = 1$;
- up-date input/output (I/O): $PHC_0 = 1$, $PHC_1 = 1$.

Each central processor is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels.

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

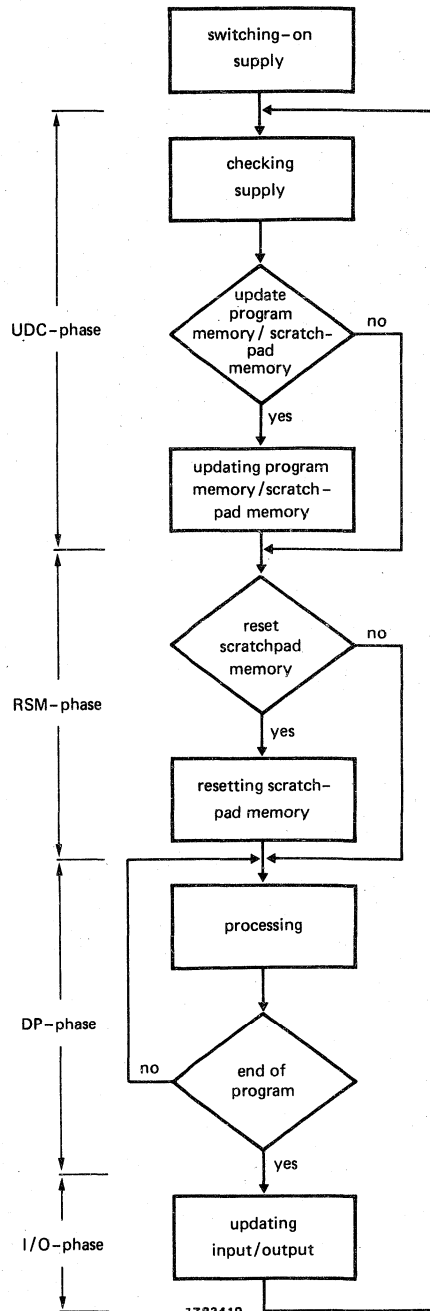


Fig. 2 Flow chart. The UDC-phase and RSM-phase are only executed if required.

7Z83419

ELECTRICAL DATA**Supply**

Supply voltage (d.c.)
current

V_P 10 V \pm 10%
 I_P max. 270 mA

Requirements of the external battery to retain the contents of the scratchpad memory during power failure.

Battery voltage

V_B 3 to 4,5 V

Battery current ($V_P = 0$ V)

I_B max. 2 mA

Trickle charge current ($V_P = 10$ V)

typ. -6 mA

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function	terminations (Fig. 4)	
		connector 1	connector 2

BI-DIRECTIONAL BUSES

ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉ ADD ₁₀	Address bus interconnected with PU21 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules.	a6, a7, a8, a9, a10, a11, a12, a13, a14, a15, a16,	c6 c7 c8 c9 c10 c11 c12 c13 c14 c15 c16
APM ₀ APM ₁ APM ₂ APM ₃ APM ₄ APM ₅ APM ₆ APM ₇ APM ₈ APM ₉ APM ₁₀	Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase).		a16, a17, a18, a19, a20, a21, a22, a23, a24, a25, a26, c16 c17 c18 c19 c20 c21 c22 c23 c24 c25 c26
APM ₁₁ APM ₁₂	Pseudo address bits connected via resistor to 0 V.		a27, a28, c27 c28
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bus; receives data for scratchpad memory from input modules and PU21, transmits data from scratchpad memory to output modules and PU21; data bus is controlled by WEPC or by R/WSM.	a19, a20, a21, a22,	c19 c20 c21 c22

	function	terminations (Fig. 4)	
		connector 1	connector 2
INS ₀ INS ₁ INS ₂ INS ₃ INS ₄	Instruction bus, interconnected with PU21; commanded by PDBE.	a1, a2, a3, a4, a5,	c1, c2, c3, c4, c5
<i>INPUTS</i>			
ALI	Alarm input for internal use. Active HIGH: input current = 2 mA.	a29,	c29
CPSD	Central processor slow down; input commanded by PU21.		a3, c3
CPSI	Central processor stop initiate; command from PU21 stops central processor in UDC-phase (active HIGH).		a4, c4
DEF	Data exchange finished; signal from output modules indicating that data from central processor has been stored.	a25	
HOLD	Command from PU21 to stop central processor in DP-phase (active LOW).		a6, c6
PABE	Program memory address bus enable; active during UDC-phase. When LOW APM bus functions as input.		a1, c1
PDBE	Program memory data bus enable; active during UDC-phase. When LOW, INS and ADD-bus function as inputs.		a2, c2
PRF	Preparation input/output modules finished.	a24	
$\overline{\text{RCP}}$	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current = 2 mA.		a12, c12
RSME	Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current = 2 mA) the RSM- phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.		a10, c10

	function	terminations (Fig. 4)	
		connector 1	connector 2
R/ $\overline{\text{WSM}}$	Read-write level from input and output modules; only effective during I/O-phase.	c24	
WEPC	Write enable signal from PU21; prepares central processor to store data from PU21 into scratchpad memory.	c28	
WPSM	Write pulse for scratchpad memory; signal from PU21 to store data on DIO _{0,3} into scratchpad memory.		a13, c13

OUTPUTS

APF	Address processing for input and output modules finished; address stable.	a26	
CLOCK	Clock output to PU21.		a7, c7
CPSC	Central processor stop completed; command (HIGH) to PU21 indicating that central processor has been stopped in UDC-phase.		a5, c5
PB ₀ PB ₁	Page bits, connected to 0 V.	a17 c17	
PHC ₀ PHC ₁	Phase control to PU21 and input and output modules.	a23 c23	
$\overline{\text{RCO}}$	Reset output to output modules; becomes LOW during switch-on of the system, or if $\overline{\text{RCP}}$ is LOW. When a wire jump has been inserted between the $\overline{\text{RCO}}$ points on the module (Fig. 3), $\overline{\text{RCO}}$ output will also become LOW if $V_p < 9 \text{ V}$ or $> 11 \text{ V}$.	c27	
RR	Result Register.	a18, c18	
SBI	Storage command to store data on data bus into output modules and PU21.	c26	

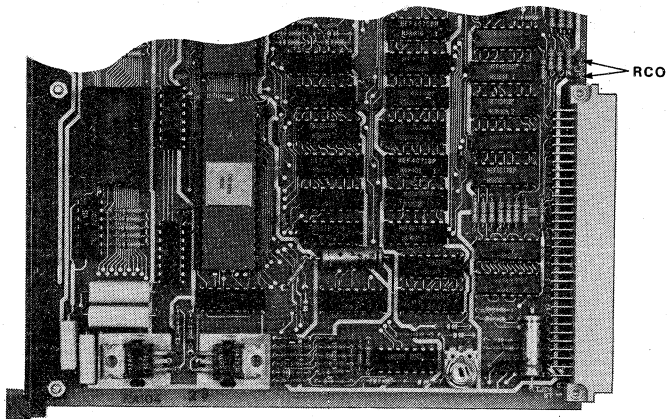


Fig. 3 Location of RCO points.

Fixed scratchpad memory addresses

address	description
000.0	Overflow bit for arithmetic operations.
000.1	Constant "1" level.
000.2	24 V alarm output.
000.3	Timer clock 10 ms.
001.0	Timer clock 100 ms.
001.1	Timer clock 1 s.
001.2	Timer clock 10 s.
001.3	Timer clock 1 min.

MECHANICAL DATA

Dimensions in mm

Outlines

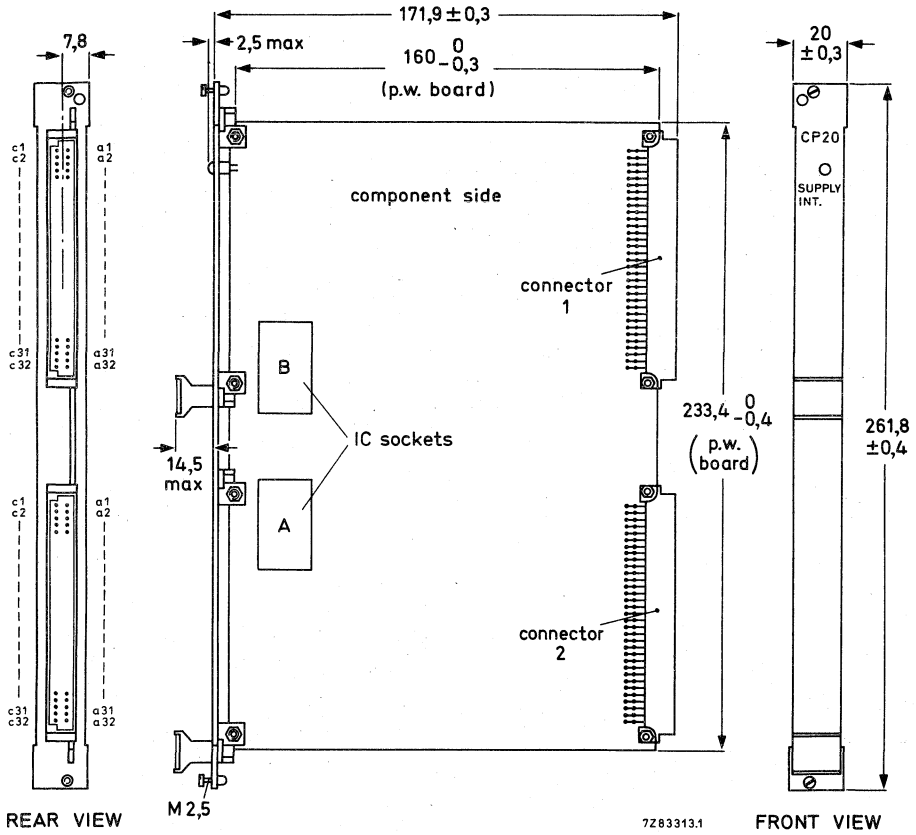


Fig. 4.

Mass

approx. 270 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
INS ₀	1	INS ₀	PABE	1	PABE
INS ₁	2	INS ₁	PDBE	2	PDBE
INS ₂	3	INS ₂	CPSD	3	CPSD
INS ₃	4	INS ₃	CPSI	4	CPSI
INS ₄	5	INS ₄	CPSC	5	CPSC
ADD ₀	6	ADD ₀	HOLD	6	HOLD
ADD ₁	7	ADD ₁	CLOCK	7	CLOCK
ADD ₂	8	ADD ₂	n.c.	8	n.c.
ADD ₃	9	ADD ₃	n.c.	9	n.c.
ADD ₄	10	ADD ₄	RSME	10	RSME
ADD ₅	11	ADD ₅	n.c.	11	n.c.
ADD ₆	12	ADD ₆	RCP	12	RCP
ADD ₇	13	ADD ₇	WPSM	13	WPSM
ADD ₈	14	ADD ₈	n.c.	14	n.c.
ADD ₉	15	ADD ₉	n.c.	15	n.c.
ADD ₁₀	16	ADD ₁₀	APM ₀	16	APM ₀
PB ₁	17	PB ₀	APM ₁	17	APM ₁
RR	18	RR	APM ₂	18	APM ₂
DIO ₀	19	DIO ₀	APM ₃	19	APM ₃
DIO ₁	20	DIO ₁	APM ₄	20	APM ₄
DIO ₂	21	DIO ₂	APM ₅	21	APM ₅
DIO ₃	22	DIO ₃	APM ₆	22	APM ₆
PHC ₀	23	PHC ₁	APM ₇	23	APM ₇
R/WSM	24	PRF	APM ₈	24	APM ₈
0 V *	25	DEF	APM ₉	25	APM ₉
SBI	26	APF	APM ₁₀	26	APM ₁₀
RCO	27	n.c.	APM ₁₁	27	APM ₁₁
WEPC	28	n.c.	APM ₁₂	28	APM ₁₂
ALI	29	ALI	n.c.	29	n.c.
n.c.	30	n.c.	VB	30	VB
V _p	31	V _p	V _p	31	V _p
0 V	32	0 V	0 V	32	0 V

n.c. = not connected.

* No supply line; is used as return line for control signals.

CENTRAL PROCESSOR

DESCRIPTION

The central processor CP21 is for use with other PC20 modules, to assemble a programmable controller.

The central processor is the heart of the PC20 controller; it requests data from the input modules, processes the data according to the instructions written in the program memory, and applies the results to the output modules. It also generates clock pulses for the controller.

The central processor block diagram is given in Fig. 1. The *data processor* controls the system and the complete timing. It includes the instruction decoder, the 1-bit logic processor, the 4-bit arithmetic processor and the data control.

The *address processor* generates addresses for the program memory under program control. It also generates addresses for the input and output modules.

The *program memory* is a C-MOS RAM (1 k16). The CP21 has on-board battery back-up and a provision to connect an external battery for longer memory retention.

The capacity of the *scratchpad memory* is $\frac{1}{4}k4$. Depending on the instruction, the scratchpad memory can be addressed word by word (addresses run from 000 to 255) or bit by bit (addresses run from 000.0 to 255.3). In the latter case, the address notation is, for example, 147.2 or 076.0. The on-board battery for data retention in the program memory RAM, is also used for data retention of the scratchpad memory.

The *UDC-circuit* (Up-Date and Check) controls the switch-on/off procedure; it informs the system of power failures. It also controls the access of the programming unit to the system memories.

The *reset scratchpad memory circuit* allows the central processor to set all scratchpad memory locations to zero, dependent on the RSME level, immediately after switch-on of the system.

The *timer clock circuit* provides 5 crystal-controlled timer clocks: 10 ms, 100 ms, 1 s, 10 s, 1 min (50% duty factor).

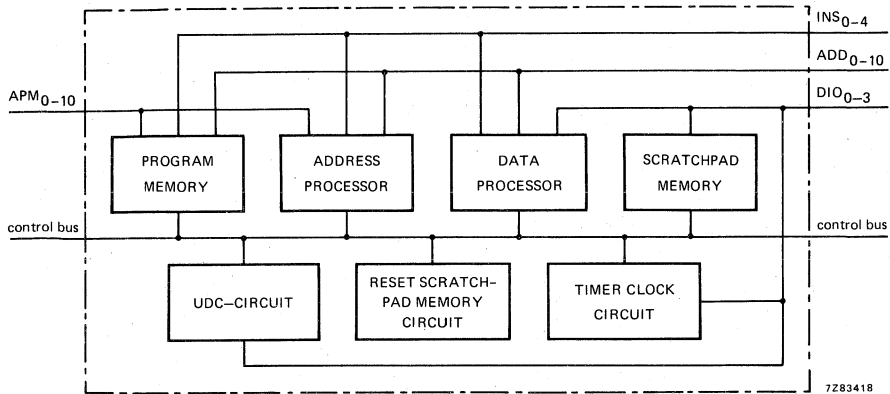


Fig. 1 Block diagram.

Figure 2 illustrates the system operation. The system operates in four phases, which are continuously repeated. The phases, indicated by levels on outputs PHC_0 and PHC_1 , are:

- up-date and check phase (UDC): $PHC_0 = 0$, $PHC_1 = 0$;
- reset scratchpad memory (RSM): $PHC_0 = 1$, $PHC_1 = 0$.
- data processing (DP): $PHC_0 = 0$, $PHC_1 = 1$.
- up-date input/output (I/O): $PHC_0 = 1$, $PHC_1 = 1$.

Each central processor is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels.

* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

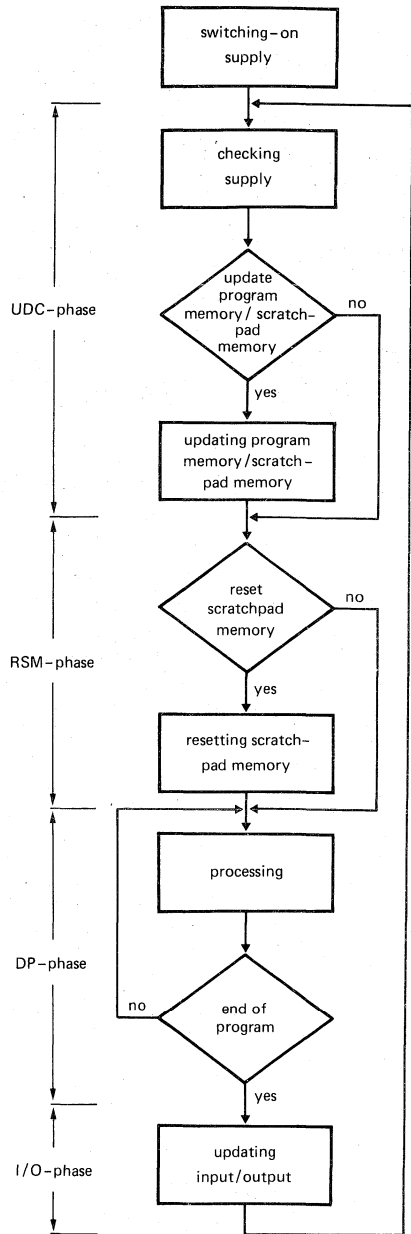


Fig. 2 Flow chart. The UDC-phase and RSM-phase are only executed if required.

7283419

ELECTRICAL DATA**Supply**

Supply voltage (d.c.)
current

V_p 10 V \pm 10%
 I_p max. 160 mA

Requirements of the external battery to retain the contents of the program memory and the scratchpad memory during power failure.

Battery voltage

V_B 3 to 4,5 V

Battery current ($V_p = 0$ V)

I_B max. 2 mA

Trickle charge current ($V_p = 10$ V)

typ. -6 mA

Data retention with on-board battery at 40 °C

typ. 40 h, provided the module
is in operation for at least
20 h

Input and output data

The voltage levels of inputs and outputs are in accordance with standard LOCMOS specifications.

	function	terminations (Fig. 4)	
		connector 1	connector 2
BI-DIRECTIONAL BUSES			
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉ ADD ₁₀	Address bus interconnected with PU21 and input and output modules; commanded by PDBE; during DP-phase address bits for the scratchpad memory; during I/O-phase address bits for the input and output modules.	a6, c6 a7, c7 a8, c8 a9, c9 a10, c10 a11, c11 a12, c12 a13, c13 a14, c14 a15, c15 a16, c16	
APM ₀ APM ₁ APM ₂ APM ₃ APM ₄ APM ₅ APM ₆ APM ₇ APM ₈ APM ₉ APM ₁₀	Program memory address bus; APM act as inputs when PABE is LOW (only during UDC-phase).		a16, c16 a17, c17 a18, c18 a19, c19 a20, c20 a21, c21 a22, c22 a23, c23 a24, c24 a25, c25 a26, c26
APM ₁₁ APM ₁₂	Pseudo address bits connected via resistor to 0 V.		a27, c27 a28, c28
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bus; receives data for scratchpad memory from input modules and PU21, transmits data from scratchpad memory to output modules and PU21; data bus is controlled by WEPC or by R/W _{SM} .	a19, c19 a20, c20 a21, c21 a22, c22	

	function	terminations (Fig. 4)	
		connector 1	connector 2
INS ₀ INS ₁ INS ₂ INS ₃ INS ₄	Instruction bus, interconnected with PU21; commanded by PDBE,	a1, c1 a2, c2 a3, c3 a4, c4 a5, c5	
<i>INPUTS</i>			
ALI	Alarm input for internal use. Active HIGH: input current = 2 mA.	a29, c29	
CPSD	Central processor slow down; input commanded by PU21.		a3, c3
CPSI	Central processor stop initiate; command from PU21 stops central processor in UCD-phase (active HIGH).		a4, c4
DEF	Data exchange finished; signal from output modules indicating that data from central processor has been stored.	a25	
HOLD	Command from PU21 to stop central processor in DP-phase (active LOW).		a6, c6
PABE	Program memory address bus enable; active during UDC-phase. When LOW APM bus functions as input.		a1, c1
PDBE	Program memory data bus enable; active during UDC-phase. When LOW, INS and ADD-bus function as inputs.		a2, c2
PRF	Preparation input/output modules finished.	a24	
$\overline{\text{RCP}}$	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active LOW: input current = 2 mA.		a12, c12
RSME	Reset scratchpad memory enable. When HIGH or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When LOW (input current = 2 mA) the RSM- phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.		a10, c10
$\overline{\text{R/WPM}}$	Write signal from PU21 to CP21, to store data in program memory (active HIGH).		a14, c14

	function	terminations (Fig. 4)	
		connector 1	connector 2
R \overline{W} SM	Read-write level from input and output modules; only effective during I/O-phase.	c24	
WEPC	Write enable signal from PU21; prepares central processor to store data from PU21 into scratchpad memory.	c28	
WPSM	Write pulse for scratchpad memory; signal from PU21 to store data on DIO ₀₋₃ into scratchpad memory.		a13, c13

OUTPUTS

APF	Address processing for input and output modules finished; address stable.	a26	
CLOCK	Clock output to PU21.		a7, c7
CPSC	Central processor stop completed; command (HIGH) to PU21 indicating that central processor has been stopped in UDC-phase.		a5, c5
PB ₀ PB ₁	Page bits, connected to 0 V.	a17 c17	
PHC ₀ PHC ₁	Phase control to PU21 and input and output modules.	a23 c23	
\overline{RCO}	Reset output to output modules; becomes LOW during switch-on of the system, or if \overline{RCP} is LOW. When a wire jump has been inserted between the RCO points on the module (Fig. 3), \overline{RCO} output will also become LOW if $V_P < 9$ V or > 11 V.	c27	
RR	Result Register	a18, c18	
SBI	Storage command to store data on data bus into output modules and PU21.	c26	

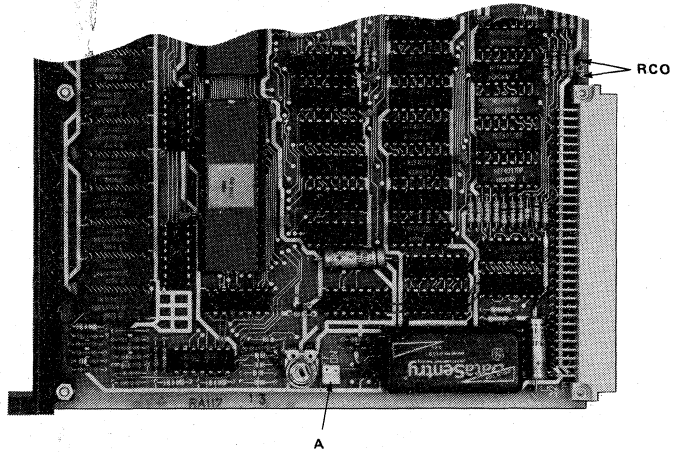


Fig. 3 Location of RCO points and switch (jumper A) of on-board battery.

Fixed scratchpad memory addresses

address	description
000.0	Overflow bit for arithmetic operations.
000.1	Constant "1" level.
000.2	24 V alarm output.
000.3	Timer clock 10 ms.
001.0	Timer clock 100 ms.
001.1	Timer clock 1 s.
001.2	Timer clock 10 s.
001.3	Timer clock 1 min.

MECHANICAL DATA

Dimensions in mm

Outlines

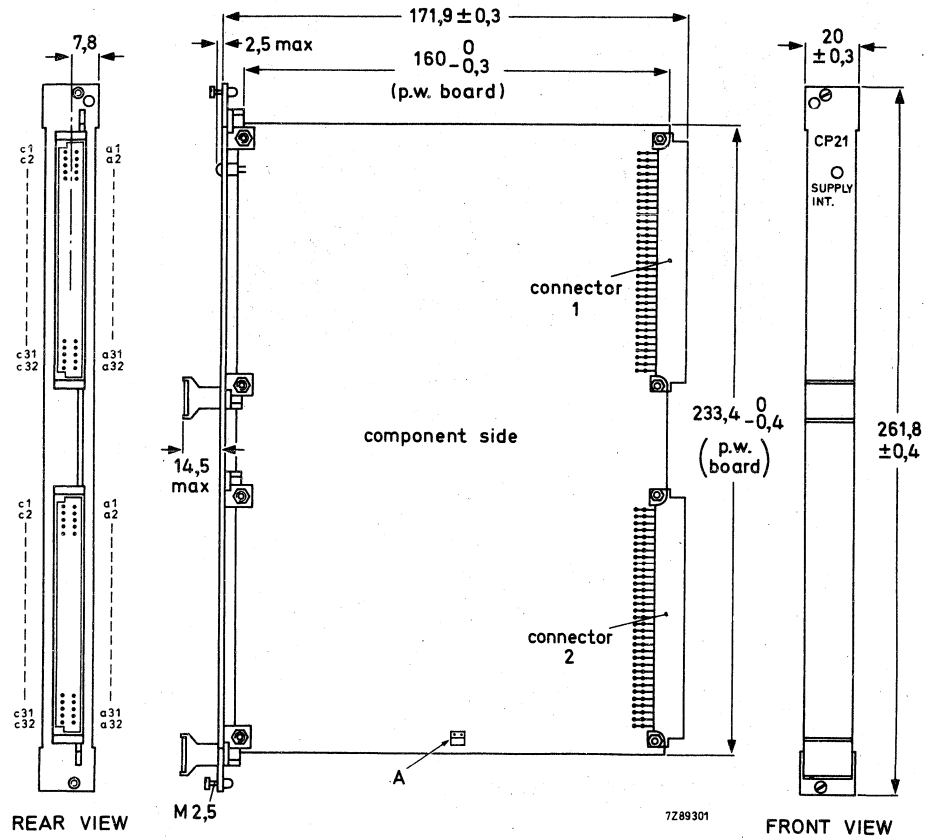


Fig. 4.

Mass approx. 270 g

Notes

1. At delivery of the central processor the on-board battery is switched off (jumper A, Figs 3 and 4, in off-position).
2. If the central processor is removed from the rack, ensure that it is put on an insulated surface to prevent short-circuiting of the on-board battery.

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
INS ₀	1	INS ₀	PABE	1	PABE
INS ₁	2	INS ₁	PDBE	2	PDBE
INS ₂	3	INS ₂	CPSD	3	CPSD
INS ₃	4	INS ₃	CPSI	4	CPSI
INS ₄	5	INS ₄	CPSC	5	CPSC
ADD ₀	6	ADD ₀	HOLD	6	HOLD
ADD ₁	7	ADD ₁	CLOCK	7	CLOCK
ADD ₂	8	ADD ₂	n.c.	8	n.c.
ADD ₃	9	ADD ₃	n.c.	9	n.c.
ADD ₄	10	ADD ₄	RSME	10	RSME
ADD ₅	11	ADD ₅	n.c.	11	n.c.
ADD ₆	12	ADD ₆	\overline{RCP}	12	\overline{RCP}
ADD ₇	13	ADD ₇	WPSM	13	WPSM
ADD ₈	14	ADD ₈	$\overline{R/WPM}$	14	$\overline{R/WPM}$
ADD ₉	15	ADD ₉	n.c.	15	n.c.
ADD ₁₀	16	ADD ₁₀	APM ₀	16	APM ₀
PB ₁	17	PB ₀	APM ₁	17	APM ₁
RR	18	RR	APM ₂	18	APM ₂
DIO ₀	19	DIO ₀	APM ₃	19	APM ₃
DIO ₁	20	DIO ₁	APM ₄	20	APM ₄
DIO ₂	21	DIO ₂	APM ₅	21	APM ₅
DIO ₃	22	DIO ₃	APM ₆	22	APM ₆
PHC ₀	23	PHC ₁	APM ₇	23	APM ₇
$\overline{R/WSM}$	24	PRF	APM ₈	24	APM ₈
0 V*	25	DEF	APM ₉	25	APM ₉
SBI	26	APF	APM ₁₀	26	APM ₁₀
\overline{RCO}	27	n.c.	APM ₁₁	27	APM ₁₁
WEPC	28	n.c.	APM ₁₂	28	APM ₁₂
ALI	29	ALI	n.c.	29	n.c.
n.c.	30	n.c.	VB	30	VB
V _p	31	V _p	V _p	31	V _p
0 V	32	0 V	0 V	32	0 V

n.c. = not connected

* No supply line; is used as return line for control signals.

INPUT MODULE

DESCRIPTION

This input module is used with the other PC20 modules to assemble a programmable controller.

The input module contains 16 addressable input stages, with photo-isolators between external and internal circuitry (Fig. 1). All inputs are floating with respect to each other. Each input stage has a LED for status indication: it is lit when the input is active. Furthermore, to limit power consumption, these LEDs can be switched-off. A delay circuit (symmetrical delay time typ. 1 ms) is incorporated in each input stage to increase the noise immunity. The delay time can be increased by adding extra capacitance.

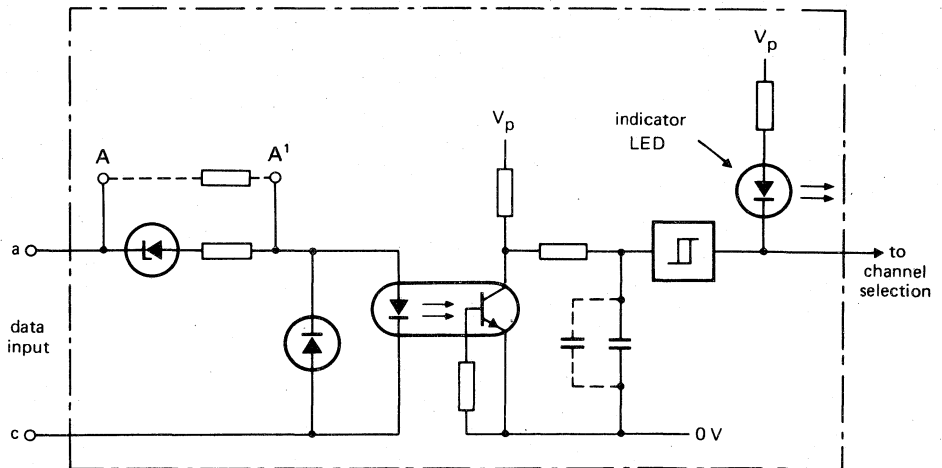


Fig. 1 Circuit diagram of an input stage.

7Z83209

Each input module has 11 address inputs (ADD_{0-10}) and 9 module identification inputs (MID_{1-9}), which are accessible on the connectors at the rear (Fig. 2).

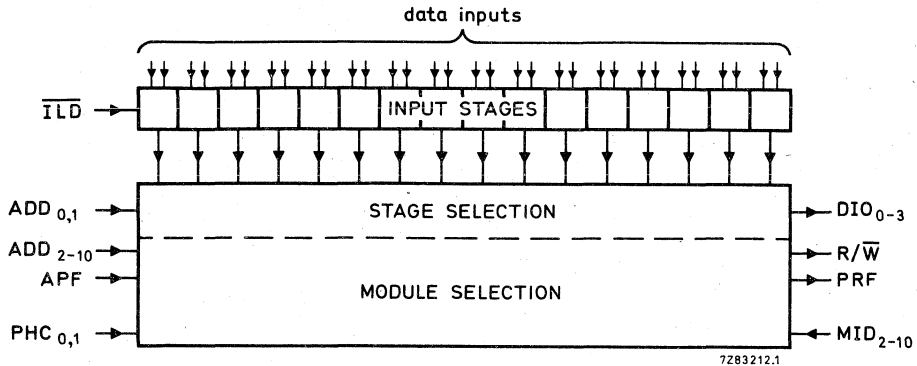


Fig. 2 Block diagram of the input module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard). The board has two F068-1 connectors (board parts); the corresponding rack part of connector 1 (Fig. 4) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89291 (pins for wire wrapping), 2422 025 89299 (pins for dip-soldering) or 2422 025 89327 (solder tags).*

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	V_p	$10\text{ V} \pm 10\%$
		typ. 45 mA (all inputs inactive)
current	I_p	typ. 175 mA (all inputs active)
		max. 200 mA (all inputs active)

Input data

The data inputs are $DI_{W,0}$ to $DI_{W,3}$, $DI_{X,0}$ to $DI_{X,3}$, $DI_{Y,0}$ to $DI_{Y,3}$ and $DI_{Z,0}$ to $DI_{Z,3}$. They are accessible on connector 2, see "Terminal location".

	5 V level (note 2)	24 V level
Active voltage (V_{a-c})	3,5 to 6 V	17 to 30 V
Non-active voltage (V_{a-c})	0 to 0,8 V or floating	0 to 7 V or floating
Input current, active at $V_{a-c} = 5\text{ V}$ or 24 V resp.	typ. 10 mA	typ. 10 mA

} note 1

The delay time of the delay circuit can be increased by inserting capacitors (approx. 0,015 $\mu\text{F/ms}$) between connecting points B and B' (Fig. 3).

Notes

- V_{a-c} is the voltage between terminal of row a and terminal of row c of connector 2.
- For 5 V-level operation a resistor of $360\ \Omega \pm 5\%$, style CR25, has to be connected to each input stage between connecting points A and A' (Fig. 3).

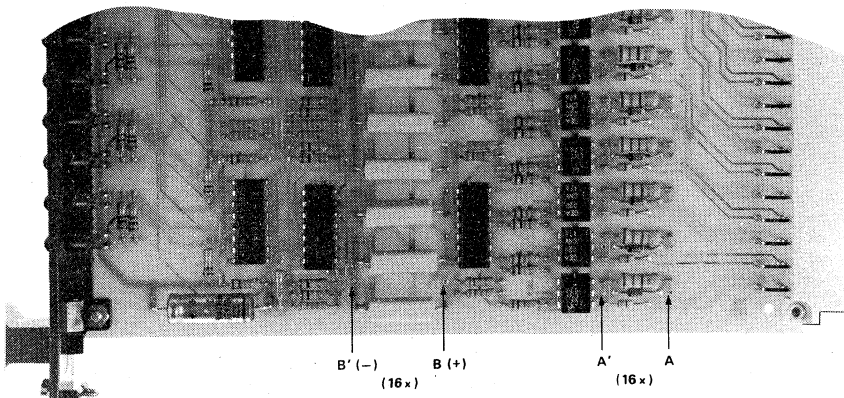


Fig. 3 Part of the printed-wiring board, showing the connecting points for the additional delay capacitors and the resistors for 5 V-level operation.

The inputs mentioned below meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 4)	
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉ ADD ₁₀	Address bits from central processor: ADD ₀₋₁ select a group of 4 input stages, ADD ₂₋₁₀ select the input module.	a11 a12 a13 a14 a15	c11 c12 c13 c14 c15 c16
MID ₂ MID ₃ MID ₄ MID ₅ MID ₆ MID ₇ MID ₈ MID ₉ MID ₁₀	Module identification inputs; provide module with individual identity.		c2 c3 c4 c5 c6 c7 c8 c9 c10
APF	Handshake signal; input/output address correct.	a26	
PHC ₀ PHC ₁	Phase control signals.	a23	c23
$\overline{\text{ILD}}$	Indication LED disable; input current LOW: 0,1 mA		c28

Output data

All outputs meet the standard LOCMOS specifications, except the R/\bar{W} and PRF outputs.

output	function	terminations of connector 1 (Fig. 4)
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bits to central processor; data is stored in scratchpad memory of central processor.	a21 c21 a22 c22
R/\bar{W}	Signal to central processor (active LOW); prepares central processor for data on DIO ₀₋₃ to be written in the scratchpad memory (open collector output).	c24
PRF	Preparation R/\bar{W} level finished (open collector output).	a24



MECHANICAL DATA
Outlines

Dimensions in mm

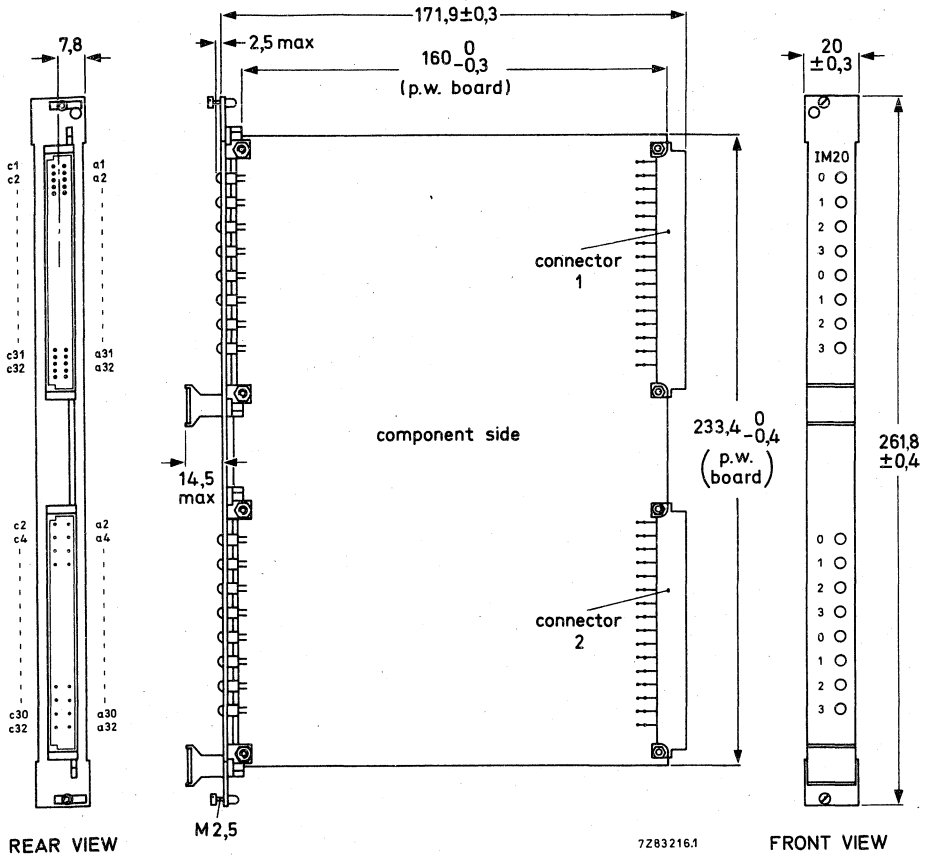


Fig. 4.

Mass 250 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
n.c.	1	HIGH level	DIW.0	2	DIW.0
MID2	2	HIGH level	DIW.1	4	DIW.1
MID3	3	HIGH level	DIW.2	6	DIW.2
MID4	4	HIGH level	DIW.3	8	DIW.3
MID5	5	HIGH level	DIx.0	10	DIx.0
MID6	6	HIGH level	DIx.1	12	DIx.1
MID7	7	HIGH level	DIx.2	14	DIx.2
MID8	8	HIGH level	DIx.3	16	DIx.3
MID9	9	HIGH level	DIy.0	18	DIy.0
MID10	10	HIGH level	DIy.1	20	DIy.1
ADD0	11	ADD1	DIy.2	22	DIy.2
ADD2	12	ADD3	DIy.3	24	DIy.3
ADD4	13	ADD5	DIz.0	26	DIz.0
ADD6	14	ADD7	DIz.1	28	DIz.1
ADD8	15	ADD9	DIz.2	30	DIz.2
ADD10	16	n.c.	DIz.3	32	DIz.3
n.c.	17	n.c.			
n.c.	18	n.c.			
n.c.	19	n.c.			
n.c.	20	n.c.			
DIO0	21	DIO1			
DIO2	22	DIO3			
PHC0	23	PHC1			
R/W	24	PRF			
0 V *	25	n.c.			
n.c.	26	APF			
n.c.	27	n.c.			
ILD	28	n.c.			
n.c.	29	n.c.			
n.c.	30	n.c.			
Vp	31	Vp			
0 V	32	0 V			

n.c. = not connected.

* No supply line; is used as return line for control signals.

** For coding MID lines.

OUTPUT MODULE

DESCRIPTION

This output module is used with the other PC20 modules to assemble a programmable controller.

The output module contains 16 addressable output stages, with photo-isolators between external and internal circuitry (Fig. 1). All outputs have grounded loads. Each output stage has a flywheel diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages have electronic short-circuit protection with automatic reset.

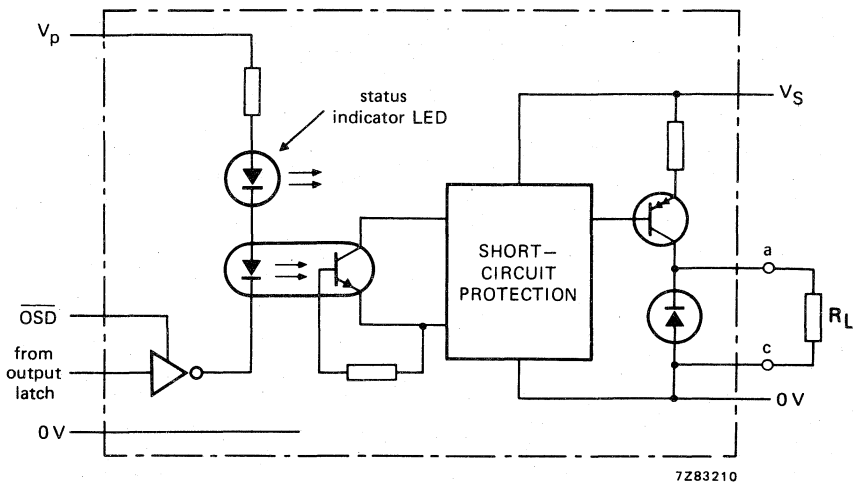


Fig. 1 Circuit diagram of an output stage.

The output module has 11 address inputs (ADD₀₋₁₀) and 9 module identification inputs (MID₁₋₉), which are accessible on the connectors at the rear (Fig. 2).

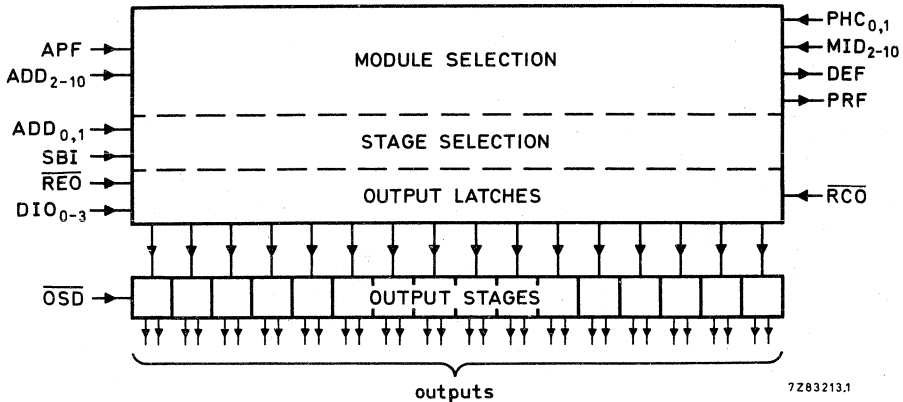


Fig. 2 Block diagram of the output module.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 3) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	} logic	V _p	10 V ± 10%
Supply current		I _p	typ. 120 mA (all stages ON) max. 150 mA (all stages ON) typ. 25 mA (all stages OFF)
Supply voltage (d.c.)	} for output circuitry	V _S	24 ± 25%**
Supply current (excluding load current)		I _S	typ. 75 mA (all stages ON) max. 110 mA (all stages ON) typ. 50 mA (all stages OFF)

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

** If V_S drops below 16 V, all output stages are forced into the non-conducting state for protection of the output circuitry.

Input data

All inputs meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 3)
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉ ADD ₁₀	Address bits from central processor; ADD ₀₋₁ select a group of four output stages, ADD ₂₋₁₀ select the output module.	a11 c11 a12 c12 a13 c13 a14 c14 a15 c15 c16
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bits from central processor; data are stored in output stages by SBI.	a21 c21 a22 c22
$\overline{\text{REO}}$	Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current LOW: 10 mA.	a27
$\overline{\text{RCO}}$	Reset from central processor (low level) during switch-on.	c27
MID ₂ MID ₃ MID ₄ MID ₅ MID ₆ MID ₇ MID ₈ MID ₉ MID ₁₀	Module identification inputs; provide module with individual identity.	c2 c3 c4 c5 c6 c7 c8 c9 c10
SBI	Clock signal from central processor to output module, stores data on DIO ₀₋₃ into output stages during input/output cycle.	c26
PHC ₀ PHC ₁	Phase control signals.	a23 c23
APF	Handshake signal; input/output address correct.	a26
$\overline{\text{OSD}}$	Output stage disable for all stages; input current LOW: 10 mA.	a28

Output data

The data outputs are $DO_{W,0}$ to $DO_{W,3}$, $DO_{X,0}$ to $DO_{X,3}$, $DO_{Y,0}$ to $DO_{Y,3}$ and $DO_{Z,0}$ to $DO_{Z,3}$. They are accessible on connector 2, see "Terminal location".

Minimum load resistance $R_L = 48 \Omega$.

Output transistor conducting: $R_L = 48 \Omega$; $V_{a-c}^* = \min. V_S - 1,5 V$.

Output transistor non-conducting: $I_o = \max. 2 \text{ mA}$ at $V_S = 30 V$.

The outputs are continuously tested for short-circuiting. As soon as the short-circuiting is removed, the output stage is automatically reset to normal operation.

Output current (limited to 6A per module)

for all stages

max. 0,375 A per stage

for maximum 12 stages

max. 0,5 A per stage

Logic outputs (open collector)

output	function	terminations of connector 1 (Fig. 3)
PRF	Preparation of output module finished.	a24
DEF	Data exchange finished.	a25

* Voltage between terminal of row a and terminal of row c of connector 2.

MECHANICAL DATA

Outlines

Dimensions in mm

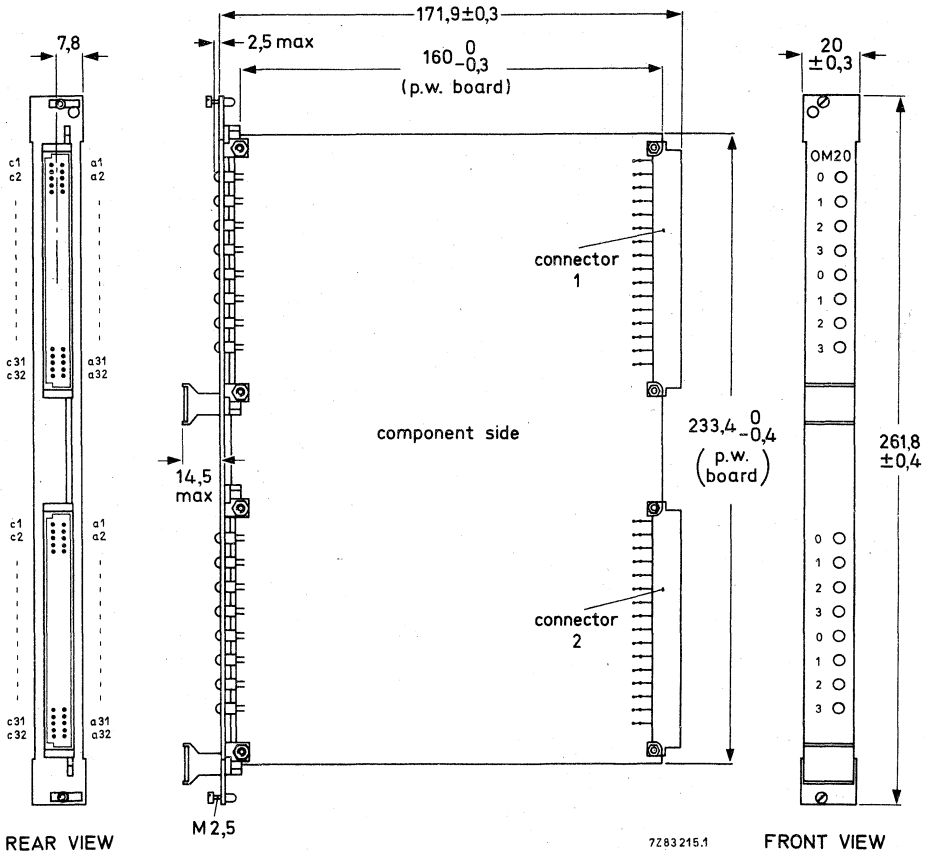


Fig. 3.

Mass

230 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
n.c.	1	HIGH level	0 V	1	V _S
MID ₂	2	HIGH level	DO _{W.0}	2	DO _{W.0}
MID ₃	3	HIGH level	0 V	3	V _S
MID ₄	4	HIGH level	DO _{W.1}	4	DO _{W.1}
MID ₅	5	HIGH level	0 V	5	V _S
MID ₆	6	HIGH level	DO _{W.2}	6	DO _{W.2}
MID ₇	7	HIGH level	0 V	7	V _S
MID ₈	8	HIGH level	DO _{W.3}	8	DO _{W.3}
MID ₉	9	HIGH level	0 V	9	V _S
MID ₁₀	10	HIGH level	DO _{X.0}	10	DO _{X.0}
ADD ₀	11	ADD ₁	0 V	11	V _S
ADD ₂	12	ADD ₃	DO _{X.1}	12	DO _{X.1}
ADD ₄	13	ADD ₅	0 V	13	V _S
ADD ₆	14	ADD ₇	DO _{X.2}	14	DO _{X.2}
ADD ₈	15	ADD ₉	0 V	15	V _S
ADD ₁₀	16	n.c.	DO _{X.3}	16	DO _{X.3}
n.c.	17	n.c.	0 V	17	V _S
n.c.	18	n.c.	DO _{Y.0}	18	DO _{Y.0}
n.c.	19	n.c.	0 V	19	V _S
n.c.	20	n.c.	DO _{Y.1}	20	DO _{Y.1}
DIO ₀	21	DIO ₁	0 V	21	V _S
DIO ₂	22	DIO ₃	DO _{Y.2}	22	DO _{Y.2}
PHC ₀	23	PHC ₁	0 V	23	V _S
n.c.	24	PRF	DO _{Y.3}	24	DO _{Y.3}
0 V *	25	DEF	0 V	25	V _S
SBI	26	APF	DO _{Z.0}	26	DO _{Z.0}
RCO	27	REO	0 V	27	V _S
n.c.	28	OSD	DO _{Z.1}	28	DO _{Z.1}
n.c.	29	n.c.	0 V	29	V _S
n.c.	30	n.c.	DO _{Z.2}	30	DO _{Z.2}
V _p	31	V _p	0 V	31	V _S
0 V	32	0 V	DO _{Z.3}	32	DO _{Z.3}

n.c. = not connected.

Note

Supply-voltage lines (V_S) have to be connected to each group of 4 outputs.

* No supply line; is used as return line for control signals.

** For coding MID lines.

PROGRAMMING UNIT

DESCRIPTION

This mains-powered programming unit is for loading, checking, dumping and monitoring the control program of the PC20-system. It provides access to the program memory and the scratchpad memory. The programming unit is a desk-top apparatus. The program is written into the program memory via the keyboard (Fig. 1) or other sources e.g. tape readers, cassette recorders, program developing systems. The program is monitored by the display or, for example, by an external VDU.

The programming unit must be used in conjunction with the programming unit interface PU21 (placed in the PC rack), to which it is connected via an 8-core cable. The circuits of the PU20 and the PU21 are galvanically isolated from each other by means of photo-isolators. The data transport via the data-in and data-out lines is serial.

After loading the program into the program memory, the programming unit can be removed to be used in another PC-system. If necessary, for monitoring purposes for example, it is very easy to connect the PU20 to the system again.

The programming unit is provided with two sockets for EPROMs, type 2716 (2k bytes) or 2758 (1k bytes).

The programming unit has the following 10 modes of operation.

1. EDIT: creating a new program or changing an existing program.
2. MONITOR CONT: continuous monitoring the PC20-system in operation; on-line change facilities.
3. MONITOR CYCLE: monitoring the PC20-system, which operates on command for one cycle.
4. MONITOR STEP: monitoring the PC20-system, which executes on command one program line.
5. PROM PROG: dumping the program from the PC20-system into the EPROMs in the sockets of the programming unit.
6. DUMP CASS: dumping the program from the PC20-system onto cassette tape.
7. DUMP RS449/423: dumping the program from the PC20-system into peripheral equipment with EIA-standard specification RS449/423.
8. LOAD PROM SOCK: loading the program from the EPROMs in the sockets of the programming unit into the PC20-system.
9. LOAD CASS: loading the program from cassette tape into the PC20-system.
10. LOAD RS449/423: loading the program from peripheral equipment with EIA-standard specification RS449/423 into the PC20-system.

A keyswitch is provided. Without the key a user can only monitor system operation and check the states of scratchpad memory locations; a user with a key has full command over all functions.

MECHANICAL DATA

Dimensions

Mass

see Fig. 2

approx. 6,3 kg

ENVIRONMENTAL DATA

Operating temperature range

Storage temperature range

0 to 45 °C

-40 to +70 °C

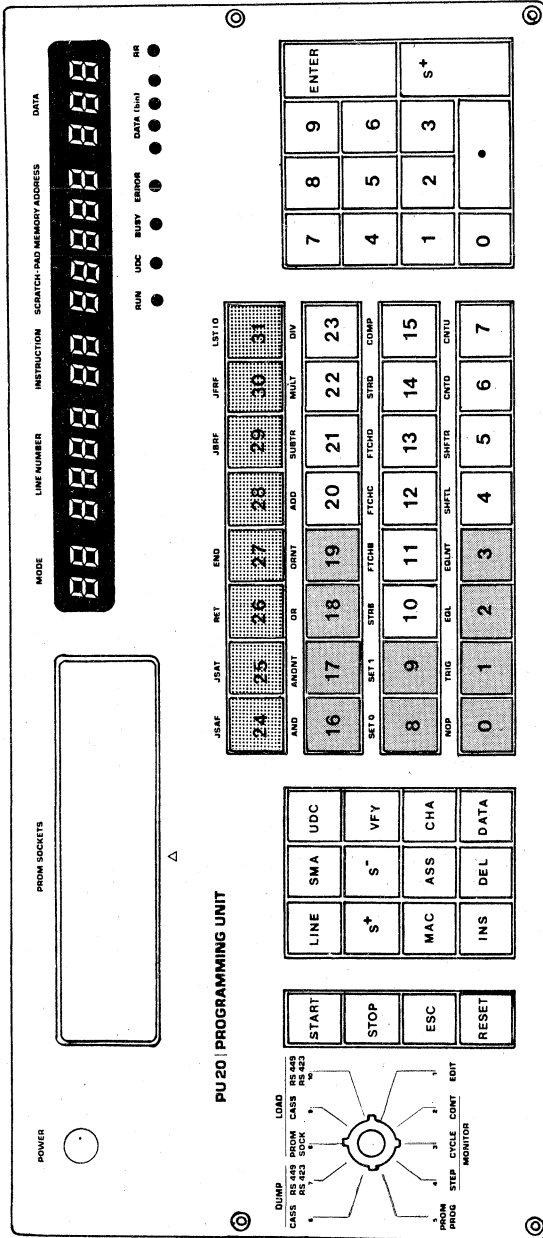
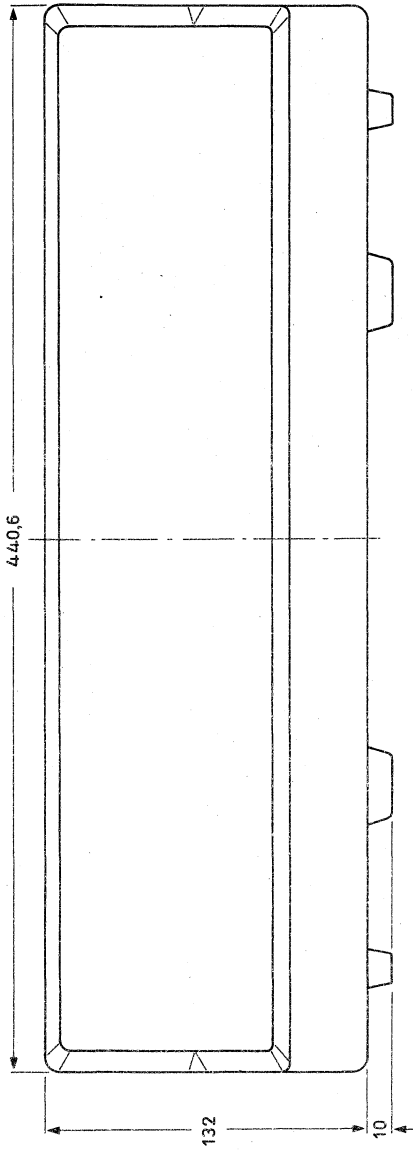
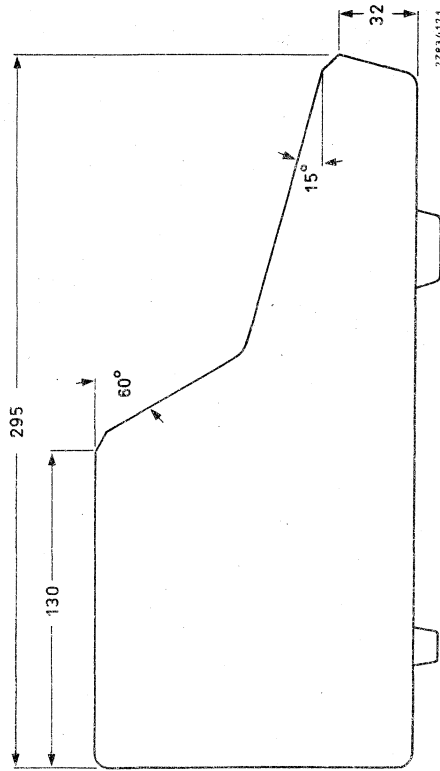


Fig. 1 Keyboard and display lay-out.



front view



side view

Fig. 2 Outline dimensions (in mm).



ELECTRICAL DATA

Mains voltage	110, 127, 220 or 240 V; tolerance + 10%, -15%
Mains frequency	46 to 65 Hz
Fusing	
for 110 or 127 V mains	200 mA (delayed action fuse)
for 220 or 240 V mains	100 mA (delayed action fuse)
Power consumption	20 VA

On delivery the programming unit is adjusted to 220 V mains voltage. If the local voltage is different, the switch at the rear must be set to the required position and the fuse must be replaced.

CONNECTING FACILITIES (see Fig. 4)

- Fixed mains cable (1) with plug with side earth-contact; length 2,4 m.
- Fixed 8-core cable (2) with 9-pole female plug F161, for connection to programming unit interface PU21; length 2,5 m. For terminal location see Table 1.
- EIA-standard interface connector plug (3), according to RS449/423, for connecting data terminal equipment (DTE), like CRT terminals, punchers, printers, readers. The pins 4, 6 and 19 are operational, along which data exchange can take place. For data terminal equipment, which requires more interconnections, Table 2 should be consulted.

Note: The programming unit is data circuit terminating equipment (DCE), configuration type DT (Data and Timing only).

- DIN-socket (4) for connecting a normal audio cassette recorder (see also Fig. 3). To avoid drop-outs it is recommended that C60 Super Quality Ferrochromium cassette tape be used.
- Two sockets for EPROMs, type 2716 (2k bytes) or 2758 (1k bytes).

Note: At the rear of the programming unit provisions (5) are made for stowage of the mains cable and the 8-core cable during transport.

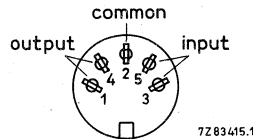


Fig. 3 DIN audio socket.

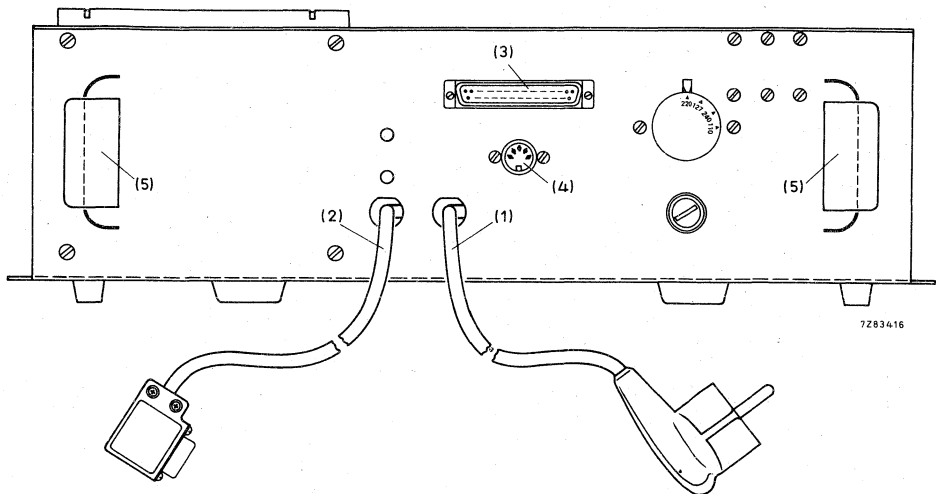


Fig. 4 Rear view.

Table 1 Terminal location of connecting cable to PU21

terminal	function
1.	connected to terminal 6
2. $\overline{\text{CLDT}}$	clock signal for data transfer between PU20 and PU21
3. $\overline{\text{TRANSFER}}$	data transfer required by PU20
4. $\overline{\text{SSE}}$	system stop enable
5.	+ 5 V *
6.	connected to terminal 1
7. $\overline{\text{DPI}}$	data from PU20 to PU21
8. $\overline{\text{DIP}}$	data from PU21 to PU20
9. $\overline{\text{READY}}$	ready signal to PU20, indicating that PU21 is available for data transfer

* No supply line; is used as a common line for the control signals.

Table 2 Terminal location of RS449/423 plug

terminal	function	operational	dummy ON	dummy OFF	jumper 1	jumper 2
2	SI — signalling route indicator		X			
4	SD — send data	X				
6	RD — receive data	X				
9	CS — clear to send					X
11	DM — data mode					X
12	TR — terminal ready					X
13	RR — receiver ready					X
15	IC — incoming call			X		
18	TM — test mode			X		
19	SG — signal ground	X			X	
20	RC — receive common				X	
33	SQ — signal quality		X			
36	SB — stand-by indicator			X		
37	SC — send common				X	

PROGRAMMING UNIT INTERFACE

DESCRIPTION

The programming unit interface can be used between a PC20-system and the programming unit PU20 which obtains access to the system via this interface. The programming unit interface does not form an essential part of an operating PC20-system which can function normally without it.

Figure 1 is a block diagram of the programming unit interface PU21 which has direct access to the data, address and control lines of the PC20-system. Furthermore it is connected to the PU20 via an 8-core cable, which contains a data-in, data-out, transfer, clock, ready, system stop enable and a common line. These lines are galvanically isolated from the PU21-circuitry by photo-isolators. The data transport via the data-in and data-out lines is serial. All actions to be executed are commanded by the PU20 through a 4-bit function mode code. This code is transmitted, with the other data to the programming unit interface, in both normal and inverted form so that correct reception can be verified.

The circuit is built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Euro-card*). The board has two F068-I connectors (male parts); the corresponding female parts are on the back panels. At the front of the unit a 9-pole male connector F161 allows connection of the cable from the programming unit.



* For a general description of the Euro-card system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

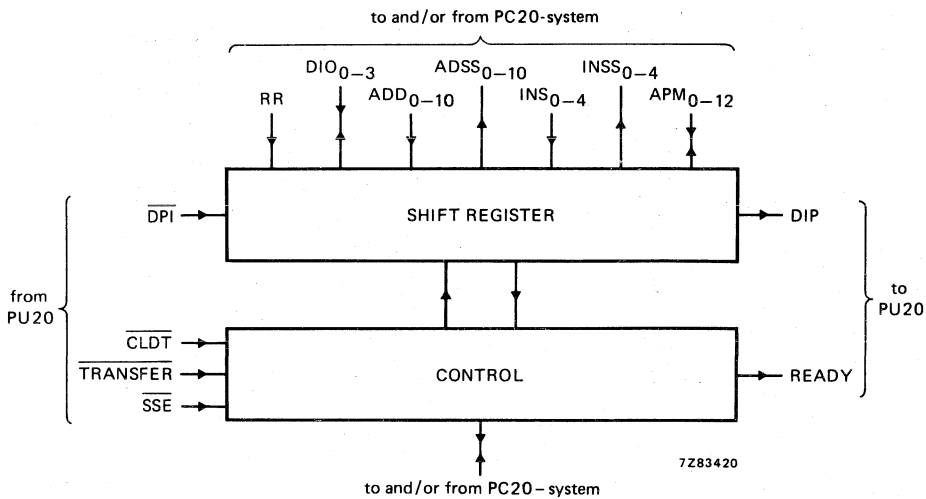


Fig. 1 Simplified block diagram.

ELECTRICAL DATA

Supply

Supply voltage (d.c.)
current

V_p 10 V ± 10%
 I_p max. 20 mA

Input and output data

All inputs and outputs meet the standard LOCMOS specifications.

	function	terminations (Fig. 2)	
		connector 1	connector 2
<i>BI-DIRECTIONAL DATA BUSES</i>			
APM ₀ APM ₁ APM ₂ APM ₃ APM ₄ APM ₅ APM ₆ APM ₇ APM ₈ APM ₉ APM ₁₀ APM ₁₁ APM ₁₂	Program memory address bus; APM ₀₋₁₂ act as outputs when PABE is LOW (only during UDC-phase).		a16, c16 a17, c17 a18, c18 a19, c19 a20, c20 a21, c21 a22, c22 a23, c23 a24, c24 a25, c25 a26, c26 a27, c27 a28, c28
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data to or from scratchpad memory, controlled by WEPC.	a19, c19 a20, c20 a21, c21 a22, c22	
<i>INPUTS</i>			
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉ ADD ₁₀	Program memory data bits from central processor (address bus).	a6 a7 a8 a9 a10 a11 a12 a13 a14 a15 a16	
CLOCK	Clock input from central processor for timing purposes.		a7, c7
CPSC	Input that indicates that the central processor has been stopped (HIGH) in the UDC-phase.		a5, c5
INS ₀ INS ₁ INS ₂ INS ₃ INS ₄	Program memory data bits from central processor (instruction bus).	a1 a2 a3 a4 a5	



	function	terminations (Fig. 2)	
		connector 1	connector 2
PB ₀ PB ₁	Page bits.	a17, c17	
PHC ₀ PHC ₁	Phase control from central processor.	a23, c23	
RR	Result register.	a18, c18	
SBI	Store command.	c26	

OUTPUTS

ADDS ₀ ADDS ₁ ADDS ₂ ADDS ₃ ADDS ₄ ADDS ₅ ADDS ₆ ADDS ₇ ADDS ₈ ADDS ₉ ADDS ₁₀	Program memory data bits (address bus) to be stored in the program memory on CP21 or MM21, or address bits for scratchpad memory to read data from or to write data in the scratchpad memory. Three-state outputs, enabled when PDBE is LOW (only during UDC-phase).	c6 c7 c8 c9 c10 c11 c12 c13 c14 c15 c16	
CPSD	Central processor slow down; command to central processor is only effective when the PU20 has been connected to the PU21.		a3, c3
CPSI	Central processor stop initiate; command to central processor (active HIGH) to stop in UDC-phase.		a4, c4
HOLD	Command to stop the central processor during the DP-phase (active LOW).		a6, c6
INSS ₀ INSS ₁ INSS ₂ INSS ₃ INSS ₄	Program memory data bits (instruction bus) to be stored in the program memory of CP21 or MM21. Three-state outputs, enabled when PDBE is LOW (only during UDC-phase).	c1 c2 c3 c4 c5	
PABE	Program memory address bus enable to central processor; APM _{0,12} terminals of PU21 act as outputs when PABE is LOW (only during UDC-phase).		a1, c1
PDBE	Program memory data bus enable. INSS _{0,4} and ADDS _{0,10} act as outputs when PDBE is LOW (only during UDC-phase).		a2, c2

	function	terminations (Fig. 2)	
		connector 1	connector 2
\overline{R}/WPM	Write signal to CP21 or MM21 to store data in program memory (active HIGH).		a14, c14
WEPC	Write enable signal to central processor; prepares central processor to store data on DIO ₀₋₃ in scratchpad memory (active LOW, only during UDC-phase).	c28	
WPSM	Write pulse for scratchpad memory; signal to store data on DIO ₀₋₃ into scratchpad memory.		a13, c13

Connection to programming unit PU20

line	function	terminations (Fig. 2) connector 3
\overline{CLDT}	clock signal for data transfer between PU20 and PU21.	2
DIP	⁸ data from PU21 to PU20.	8
\overline{DPI}	data from PU20 to PU21.	7
READY	ready signal to PU20, indicating that PU21 is available for data transfer.	9
\overline{SSE}	system stop enable.	4
$\overline{TRANSFER}$	data transfer required by PU20.	3

MECHANICAL DATA

Dimensions in mm

Outlines

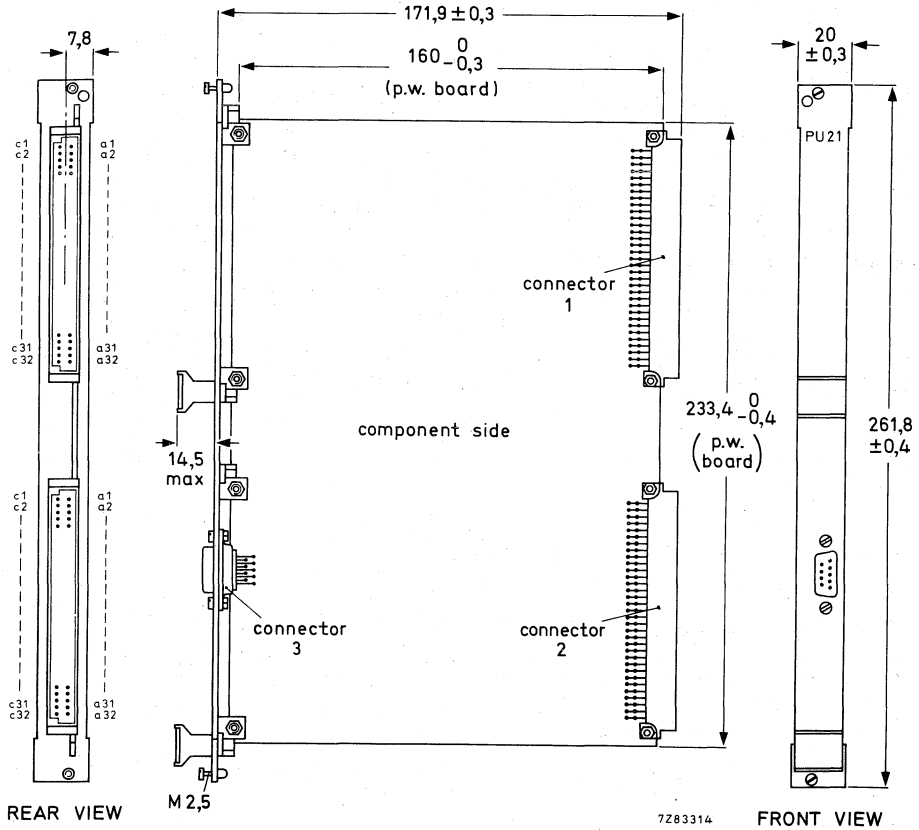


Fig. 2.

Mass

approx. 270 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
INSS0	1	INS0	PABE	1	PABE
INSS1	2	INS1	PDBE	2	PDBE
INSS2	3	INS2	CPSD	3	CPSD
INSS3	4	INS3	CPSI	4	CPSI
INSS4	5	INS4	CPSC	5	CPSC
ADDS0	6	ADD0	HOLD	6	HOLD
ADDS1	7	ADD1	CLOCK	7	CLOCK
ADDS2	8	ADD2	n.c.	8	n.c.
ADDS3	9	ADD3	n.c.	9	n.c.
ADDS4	10	ADD4	n.c.	10	n.c.
ADDS5	11	ADD5	n.c.	11	n.c.
ADDS6	12	ADD6	n.c.	12	n.c.
ADDS7	13	ADD7	WPSM	13	WPSM
ADDS8	14	ADD8	R/WPM	14	R/WPM
ADDS9	15	ADD9	n.c.	15	n.c.
ADDS10	16	ADD10	APM0	16	APM0
PB1	17	PB0	APM1	17	APM1
RR	18	RR	APM2	18	APM2
DIO0	19	DIO0	APM3	19	APM3
DIO1	20	DIO1	APM4	20	APM4
DIO2	21	DIO2	APM5	21	APM5
DIO3	22	DIO3	APM6	22	APM6
PHC0	23	PHC1	APM7	23	APM7
n.c.	24	n.c.	APM8	24	APM8
n.c.	25	n.c.	APM9	25	APM9
SBI	26	n.c.	APM10	26	APM10
n.c.	27	n.c.	APM11	27	APM11
WEPC	28	n.c.	APM12	28	APM12
n.c.	29	n.c.	n.c.	29	n.c.
n.c.	30	n.c.	n.c.	30	n.c.
V _p	31	V _p	V _p	31	V _p
0 V	32	0 V	0 V	32	0 V

Connector 3 (front panel)

1	i.c.
2	<u>CLDT</u>
3	<u>TRANSFER</u>
4	<u>SSE</u>
5	+ 5 V*
6	i.c.
7	<u>DPI</u>
8	DIP
9	READY

n.c. = not connected
i.c. = internal connected

* No supply line; is used as a common line for the control signals.

SMALL CONTROLLER CABINET

APPLICATION

This cabinet is designed for accommodating PC20 modules, for easy assembling of small controller systems.

DESCRIPTION

This metal cabinet houses a programming unit interface PU21, a central processor CP20 or CP21/CP24, a supply and output module SO20 and six input/output modules.

The cabinet has back panels, so the work of wiring separate female connectors to receive the male connectors of the modules is eliminated.

The upper panel BP20 provides the required interconnections for connector 1 of a PU21, CP20 or CP21/CP24 and an SO20 module, and of six input/output modules. It has solder bridges for allocating the addresses of the input/output modules.

The lower panel BP21 provides the interconnections for connector 2 of a PU21, CP20 or CP21/CP24 and an SO20 module; type BP22 provides for connector 2 of an input/output module. Both panels have connecting blocks with screw terminals for connection of supply voltages and input and output circuits. Furthermore, panel BP21 has connecting points for the control signals.

The cabinet is supplied with one panel BP22, but space is provided for another five BP22 panels, which can be ordered separately.

The connections to the outside world are protected by the sloping cover on the lower part of the cabinet. Openings in the underside provide entry of the input/output cables. The cabinet is intended for wall mounting.

Note: For larger controller systems, back panels BP23, BP25 and PB26 are available, to be used in 19 inch racks; see the relevant data sheet.

MECHANICAL DATA

Dimensions in mm

Outlines

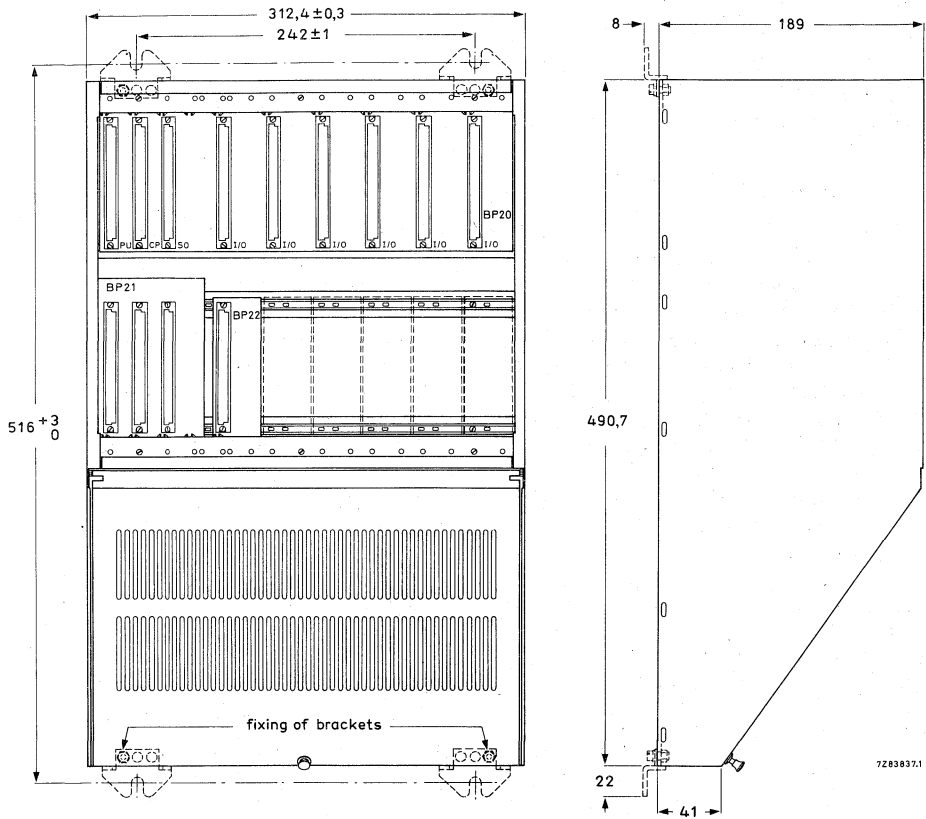


Fig. 1 Small controller cabinet.

Cabinet, material
colour

steel
black

Mass

5,2 kg

ENVIRONMENTAL DATA

Maximum permissible temperature, measured 5 cm above the cabinet

60 °C

MOUNTING OF THE CABINET

Four mounting brackets can be fitted to the cabinet (Fig. 1). They are supplied with bolts and washers with the cabinet.

The cabinet can be fixed to a wall with M6 bolts. In some cases, e.g. if the wall is not flat, it is sufficient to use three mounting brackets (one at the top and two at the bottom of the cabinet).

The cabinet must be positioned so that air has free access.

MOUNTING OF ADDITIONAL BACK PANELS BP22

The back panel BP22 has to be positioned through the openings in the bottom of the cabinet, to avoid bending of the panel. It is fitted to the mounting strip in the cabinet by means of the four M2,5 x 10 screws, which are supplied with the cabinet. Two of these screws also secure the female connector. Before tightening the screws, the panel has to be aligned. To this end an input/output module has to be slid carefully into the cabinet, so that its connectors are fully mated with their counterparts on the back panel. The lower two screws can then be tightened and, after removing the module, the fixing screws of the connector can be tightened.

Catalogue number of back panel BP22: 4322 027 92140.

ACCESSORIES

To give sufficient space for connection of the input/output cables to the connecting blocks on back panels BP22, the various input/output modules in the cabinet are 15 mm apart. To cover these spaces front plates FP20 are available.

Unused module spaces, can be covered with a front plate FP21.

Catalogue number of front plate FP20 (15 mm width): 4322 027 92150.

Catalogue number of front plate FP21 (20 mm width): 4322 027 92160.



INSTALLATION**Connection of control signals and external battery**

Control signals can be connected to the connecting points on the lower end of back panel BP21 (see Fig. 2). The functions of the control signals are indicated in the table below.

Note: Use of control signals $\overline{\text{ILD}}$, $\overline{\text{REO}}$ and $\overline{\text{OSD}}$ requires interconnections between back panels BP20 and BP21 (see Fig. 2).

connecting points	function
$\overline{\text{ILD}}$	Indication LED disable; input current low: 0,1 mA.
$\overline{\text{REO}}$	Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current low: 10 mA.
$\overline{\text{OSD}}$	Output stage disable for all stages; input current low: 10 mA.
RCP	Reset central processor; resets data processor, address processor, UDC circuitry, RSM circuitry and timer clocks. Active low: input current = 2 mA.
RSME	Reset scratchpad memory enable. When high or floating a reset of the scratchpad memory will occur during the first RSM-phase after switching on. When low (input current = 2 mA) the RSM-phase is only effective for the scratchpad memory addresses 0 to 2 inclusive.
\pm BATT	External battery connection for saving the contents of the program/scratchpad memories, in case of power failure. If central processor CP21/CP24 is used, this battery is parallel to the on-board battery and the retention time is lengthened.
ALE	Alarm external; active low as long as V_{ic} is above 17,5 V; with opto-isolater between internal and external supply.

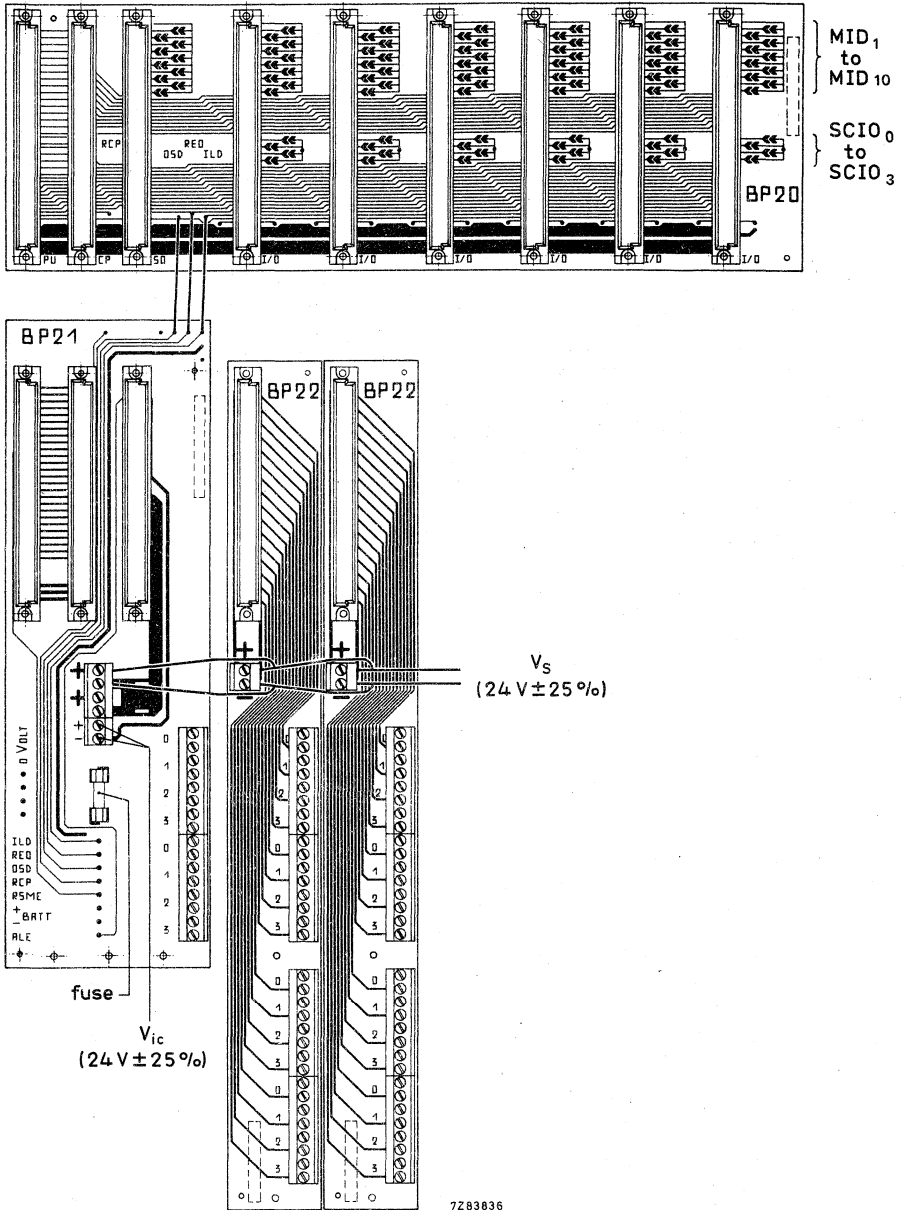


Fig. 2 Back panel arrangement.

Allocation of addresses of input/output modules

Each group of four inputs and outputs of an input/output module has a discrete address in the scratch-pad memory of the central processor. This address is allocated by bridging the appropriate MID-pads (MID₁ to MID₁₀) on back panel BP20, see Fig. 2.

Coding of inputs and outputs on modules RP20 and RS20

The coding of inputs and outputs is done by bridging the appropriate SCIO-pads (SCIO₀ to SCIO₃) on back panel BP20, see Fig. 2.

Connection of input and output circuits

The input circuits of the input modules and the output circuits of the output modules should be connected to the large connecting blocks on back panel(s) BP22. The output circuits of the SO20 module should be connected to the large connecting block of back panel BP21, see Fig. 2.

Connection of supply voltage for 24 V/10 V d.c.-d.c. converter of module SO20

The supply voltage for the converter (V_{ic}) is $24\text{ V} \pm 25\%$. It should be connected to the terminals of the small connecting block on back panel BP21, see Fig. 2. A fuse ($I_n = 1,6\text{ A}$, delayed action) protects the supply against short-circuit in the converter.

Connection of supply voltage for output modules

The supply voltage for the output modules (V_S) is $24\text{ V} \pm 25\%$. It should be connected to the double connecting block on back panel BP21 and the small connecting block on the panel(s) BP22, see Fig. 2.

Note: For full information see PC20 Manual.

SUPPLY AND OUTPUT MODULE

DESCRIPTION

This supply and output module is used with the other PC20 modules to assemble a programmable controller.

The module contains 8 addressable output stages, a 24 V/10 V d.c.-d.c. converter and an alarm circuit for the 24 V supply. The output stages have photo-isolators between external and internal circuitry (Fig. 1). All outputs have a grounded load. Each output stage has a flywheel diode, to allow it to switch inductive loads. Each output stage also has a LED for status indication: it is lit when the output transistor is conducting.

The output stages have electronic short-circuit protection with automatic reset.

The 24 V/10 V d.c.-d.c. converter provides the logic supply voltage for a small controller system with galvanic isolation from the external 24 V supply. Furthermore, it is short-circuit protected and two or more of these modules may be connected in parallel for higher current demands in larger systems.

The alarm circuit monitors the 24 V supply (V_{IC}), providing two alarm outputs. One of these is accessible for external use (hardware); the other can be used internally for processing (software). Furthermore, a LED on the front panel indicates that V_{IC} is above its minimum specified level.

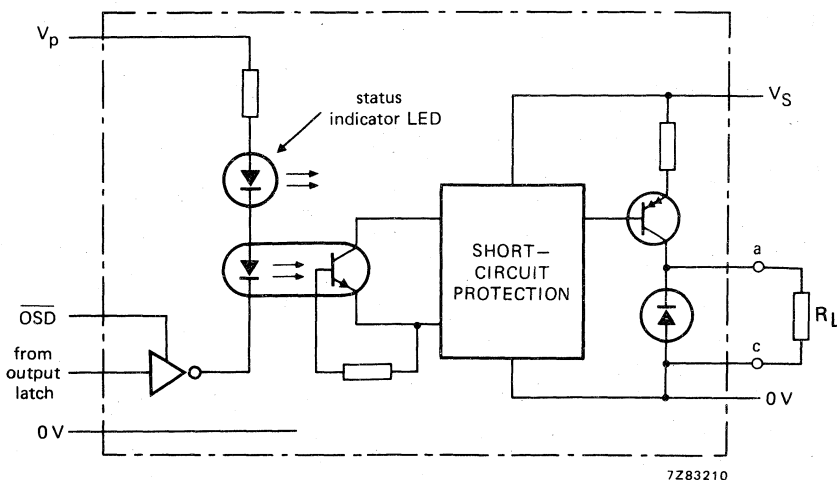


Fig. 1 Circuit diagram of an output stage.

The output part has 11 address inputs (ADD₀₋₁₀) and 10 module identification inputs (MID₀₋₉), which are accessible on the connectors at the rear (Fig. 2).

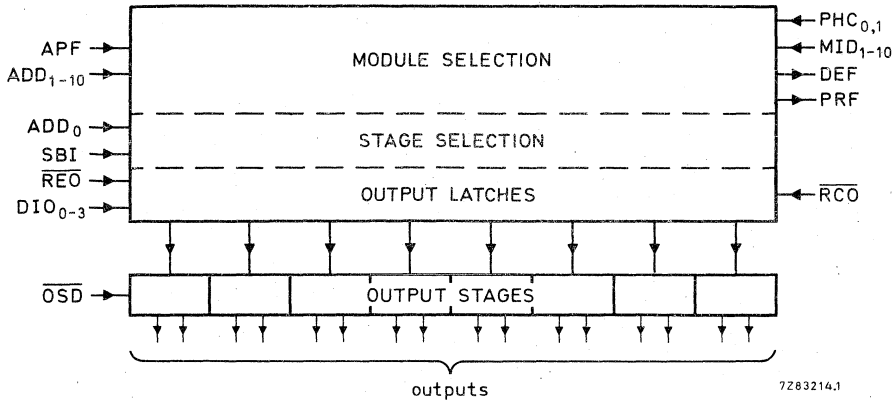


Fig. 2 Block diagram of the output part.

The circuits are built on an epoxy-glass printed-wiring board of 233,4 mm x 160 mm (double Eurocard). The board has two F068-I connectors (board parts); the corresponding rack part of connector 1 (Fig. 3) is available on the back panels, that of connector 2 (external connections) is separately available under catalogue number 2422 025 89288 (pins for wire wrapping), 2422 025 89298 (pins for dip-soldering) or 2422 025 89326 (solder tags).*

ELECTRICAL DATA

Supply

Supply voltage (d.c.)	} for output circuitry	V _S	24 V ± 25%**
Supply current (excluding load current)		I _S	typ. 50 mA (all stages ON) max. 60 mA (all stages ON) typ. 30 mA (all stages OFF)
Supply voltage (d.c.)	} for 24 V/10 V d.c.-d.c. converter	V _{ic}	24 V ± 25%
Supply current, at V _{ic} = 24 V and output current I _p = 1,7 A		I _{ic}	typ. 1,1 A

* For a general description of the Eurocard system see IEC 297 or DIN 41494 for 19-in racks and IEC 130-14 or DIN 41612 for connectors.

** If V_S drops below 16 V, all output stages are forced into the non-conducting state for protection of the output circuitry.

Input data

All inputs meet the standard LOCMOS specifications.

input	function	terminations of connector 1 (Fig. 3)
ADD ₀ ADD ₁ ADD ₂ ADD ₃ ADD ₄ ADD ₅ ADD ₆ ADD ₇ ADD ₈ ADD ₉ ADD ₁₀	Address bits from central processor; ADD ₀ selects a group of four output stages, ADD ₁₋₁₀ select the (output) module.	a11 c11 a12 c12 a13 c13 a14 c14 a15 c15 c16
DIO ₀ DIO ₁ DIO ₂ DIO ₃	Data bits from central processor; data are stored in output stages by SBI.	a21 c21 a22 c22
$\overline{\text{REO}}$	Reset output module input; a low level on this input will reset all output latches (output transistor non-conducting); input current LOW: 0,1 mA.	a27
$\overline{\text{RCO}}$	Reset from central processor (low level) during switch-on.	c27
MID ₁ MID ₂ MID ₃ MID ₄ MID ₅ MID ₆ MID ₇ MID ₈ MID ₉ MID ₁₀	Module identification inputs; provide module with individual identity.	c1 c2 c3 c4 c5 c6 c7 c8 c9 c10
SBI	Clock signal from central processor to output module, stores data on DIO ₀₋₃ into output stages during input/output cycle.	c26
PHC ₀ PHC ₁	Phase control signals.	a23 c23
APF	Handshake signal; input/output address correct.	a26
$\overline{\text{OSD}}$	Output stage disable for all stages; input current LOW: 0,1 mA.	a28

Output data

The data outputs are DO_{Y,0} to DO_{Y,3} and DO_{Z,0} to DO_{Z,3}. They are accessible on connector 2, see "Terminal location".

Minimum load resistance $R_L = 48 \Omega$.

Output transistor conducting: $R_L = 48 \Omega$; $V_{a-c}^* = \min. V_S - 1,5 V$.

Output transistor non-conducting: $I_O = \max. 2 \text{ mA}$ at $V_S = 30 V$.

The outputs are continuously tested for short-circuiting. As soon as the short-circuiting is removed, the output stage is automatically reset to normal operation.

Output current (limited to 3 A per module)

for all stages

max. 0,375 A per stage

for maximum 6 stages

max. 0,5 A per stage

Logic outputs (open collector)

output	function	terminations of connector 1 (Fig. 3)
PRF	Preparation of output module finished.	a24
DEF	Data exchange finished.	a25
ALI	Alarm internal; active LOW as long as V_{ic} is above 17,5 V; with opto-coupler isolation between internal and external supply.	a29 c29

The external alarm output ALE (connector 2, a2) has a similar function as ALI. It is an open collector output and can sink a current of 10 mA ($V_{ALE \text{ LOW}} = 1,3 V$).

Converter output

Output voltage	V_P	10 V \pm 10%
Output current	I_P	max. 1,7 A; short-circuit proof **

V_P : on terminals a31, c31 of connector 1

0 V: on terminals a32, c32 of connector 1

* Voltage between terminal of row a and terminal of row c of connector 2.

** If two or more modules are connected in parallel the output current per module is max. 1,5 A.

MECHANICAL DATA

Dimensions in mm

Outlines

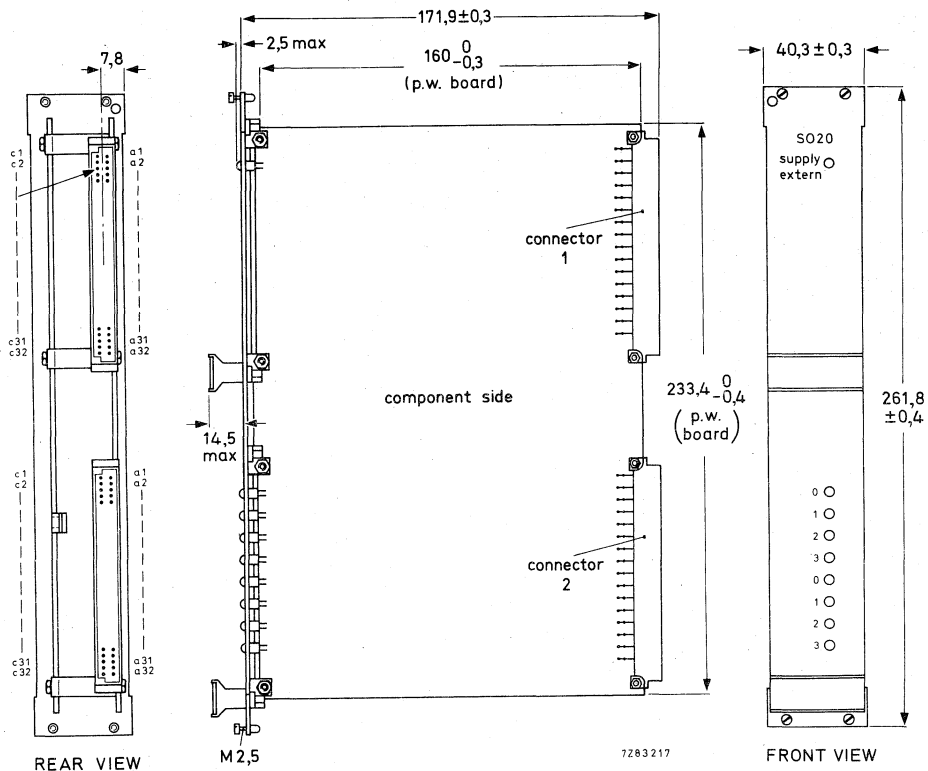


Fig. 3.

Mass 400 g

Terminal location

connector 1			connector 2		
row c		row a	row c		row a
MID ₁	1	HIGH level	n.c.	1	n.c.
MID ₂	2	HIGH level	0 V **	2	ALE
MID ₃	3	HIGH level	n.c.	3	n.c.
MID ₄	4	HIGH level	0 V **	4	V _{ic}
MID ₅	5	HIGH level	n.c.	5	n.c.
MID ₆	6	HIGH level	0 V **	6	V _{ic}
MID ₇	7	HIGH level	n.c.	7	n.c.
MID ₈	8	HIGH level	0 V **	8	V _{ic}
MID ₉	9	HIGH level	0 V *	9	V _S
MID ₁₀	10	HIGH level	0 V *	10	n.c.
ADD ₀	11	ADD ₁	0 V *	11	V _S
ADD ₂	12	ADD ₃	0 V *	12	n.c.
ADD ₄	13	ADD ₅	0 V *	13	V _S
ADD ₆	14	ADD ₇	0 V *	14	n.c.
ADD ₈	15	ADD ₉	0 V *	15	V _S
ADD ₁₀	16	n.c.	0 V *	16	n.c.
n.c.	17	n.c.	0 V *	17	V _S
n.c.	18	n.c.	DO _{Y.0}	18	DO _{Y.0}
n.c.	19	n.c.	0 V *	19	V _S
n.c.	20	n.c.	DO _{Y.1}	20	DO _{Y.1}
DIO ₀	21	DIO ₁	0 V *	21	V _S
DIO ₂	22	DIO ₃	DO _{Y.2}	22	DO _{Y.2}
PHC ₀	23	PHC ₁	0 V *	23	V _S
n.c.	24	PRF	DO _{Y.3}	24	DO _{Y.3}
0 V ****	25	DEF	0 V *	25	V _S
SBI	26	APF	DO _{Z.0}	26	DO _{Z.0}
RCO	27	REO	0 V *	27	V _S
n.c.	28	OSD	DO _{Z.1}	28	DO _{Z.1}
ALI	29	ALI	0 V *	29	V _S
n.c.	30	n.c.	DO _{Z.2}	30	DO _{Z.2}
V _p	31	V _p	0 V *	31	V _S
0 V	32	0 V	DO _{Z.3}	32	DO _{Z.3}

n.c. = not connected.

Note

Supply-voltage lines (V_S) have to be connected to each group of 4 outputs.

* 0 V for V_S.

** 0 V for V_{ic}.

*** For coding MID-lines.

**** No supply line; is used as return line for control signals.

HNIL FZ/30-SERIES



HIGH NOISE IMMUNITY LOGIC

INTRODUCTION

In noisy environments - in data handling and processing, in industrial control, in computer peripherals - you need High Noise Immunity Logic. You need the FZ/30-Series. It gives you a comprehensive range of logic elements - plus such indispensable ancillaries as timers, power amplifiers, lamp or relay drive modules, and interface modules. And they have one outstanding advantage, by adding a capacitor you can slow-down the system response and raise the a. c. noise threshold to meet your needs.

The modules are small, over a hundred would fit on this page, and have an operating temperature range up to 70 °C. Wide voltage tolerances make these circuits first choice for a host of industrial and professional applications. And they're easy to use - a simple loading table tells you what each unit can drive, and what's needed to drive it. And we supply a full set of bits to go round them - input/output devices - printed-wiring boards - connectors - sticker symbols - name it - its in the FZ/30-Series range of auxiliaries.

Check with us for full details of the FZ/30-Series. You get fast, reliable deliveries, attractive quotations, and an applications service that is second to none.

SURVEY OF TYPES

type	description	catalogue number
FZH101/4.NAND32	Quad 2-input NAND gate	2722 006 01081
FZH111/4.NAND30	Quad 2-input NAND gate Two gates can be slowed down	2722 006 01001
FZH121/2.NAND30	Dual 5-input NAND gate	2722 006 01061
FZH131/2.NAND31	Dual 5-input NAND gate Both gates can be slowed down	2722 006 01011
FZH141/2.NAND32	Dual 5-input power NAND gate Both gates can be slowed down	2722 006 01021
FZH151/2.AOR30	Dual 5-input AND-AND-OR gate One gate can be slowed down	2722 006 02001
FZH161/4.LI31	Quad logic interface gate HNIL to 5 V logic; all gates can be slowed down	2722 006 04011
FZH171/2.NAND33	Dual 4-input NAND gate With expandable inputs; both gates can be slowed down	2722 006 01091

SURVEY OF TYPES (continued)

type	description	catalogue number
FZH181/4.LI30	Quad logic interface gate 5 V logic to HNIL	2722 006 04001
FZH191/3.NAND33	Triple 3-input NAND gate Two gates can be slowed down	2722 006 01031
FZH201/6.IN30	Sextuple inverter with strobe input	2722 006 07001
FZH211/4.NAND34	Quad 2-input NAND gate Two gates can be slowed down, outputs have open collectors	2722 006 01041
FZH231/2.NAND35	Dual 5-input NAND gate Both outputs can be slowed down, outputs have open collectors	2722 006 01051
FZH241/2.AST30	Dual 4-input NAND Schmitt trigger with expandable inputs; output can be slowed down	2722 006 12001
FZH251/4.AND30	Quad 2-input AND gate Two gates can be slowed down	2722 006 13001
FZH261/2.N-4.I30	Dual NAND gate/quad inverter	2722 006 08001
FZH271/4.EO30	Quad EXCLUSIVE-OR gate Two gates can be slowed down	2722 006 11001
FZH281/4.NOR30	Quad NOR gate Two gates can be slowed down	2722 006 10001
FZH291/4.OR30	Quad OR gate Two gates can be slowed down	2722 006 09001
FZJ101/FF30	Single JK flip-flop Slave can be slowed down	2722 006 00001
FZJ111/FF31	Single JK flip-flop Master and slave can be slowed down	2722 006 00011
FZJ121/2.FF32	Dual JK master-slave flip- flop	2722 006 00021
FZJ131/4.FF33	Quad D-type latch flip-flop	2722 006 00031

SURVEY OF TYPES (continued)

type	description	catalogue number
FZJ141/FF34	Single synchronous decimal counter Has parallel-set and common reset inputs	2722 006 00041
FZJ151/FF35	Single synchronous 4-bit binary counter. Has parallel-set and common reset inputs	2722 006 00051
FZJ161/FF36	Single synchronous 4-bit shift register. Two gates can be slowed down	2722 006 00061
FZK101/OS30	Single monostable multivibrator Input can be slowed down	2722 006 03001
FZL101/ND30	Single BCD-decimal decoder numerical indicator tube driver	2722 006 06021
FZL111/SD30	BCD 7-segment decoder-driver with open collector outputs	2722 006 14001
FZL121/PA31	Short-circuit-proof power stage with open collector output	2722 032 00121
FZL131/PA32	Short-circuit-proof power stage with open collector output	2722 032 00131
FZL141/PA33	Short-circuit-proof power driver for transistor stages	2722 032 00141
2. LRD30	Dual lamp/relay driver Can be slowed down	2722 006 06011
PA30	Power amplifier Can be slowed down	2722 032 00091
TU30	Single timer unit	2722 006 05001

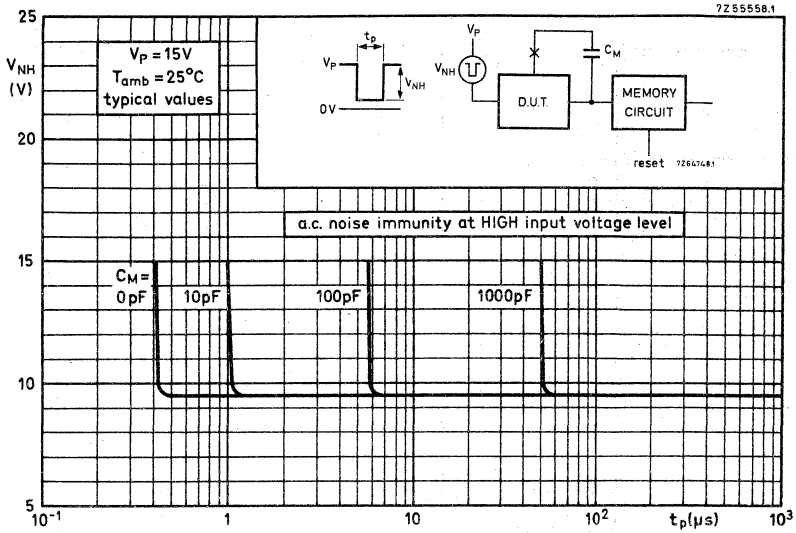
MAIN CHARACTERISTICS

Operating ambient temperature (range I)		0 to +70	°C
Storage temperature		-65 to +150	°C
Package outline		dual in-line	
Supply voltage : range I	12	+ 12 ¹ / ₂ % - 5 %	V 1)
	15	+ 13 % - 10 %	V 1)
range II			
Power consumption (per gate)	typ.	30	mW
(per flip-flop)	typ.	165	mW
Counting rate (flip-flops) can be slowed down	<	500	kHz
Fan-out (in gate loads): NAND gates and flip-flops	N _{aL}	10	
	POWER-NAND gates	N _{aL}	30
	for all units	N _{aH}	100
Propagation delay : (gates)	typ.	150	ns 2)
	(flip-flops)	typ.	430 ns 2)
Output short circuit duration non-repetitive value	t _{QSC}	max. 1	s 3)
D. C. noise margin	typ.	5	V
A. C. noise threshold		see curves next page	
(With an external capacitor the response time of a function can be slowed down, resulting in an increased a. c. noise threshold.)			

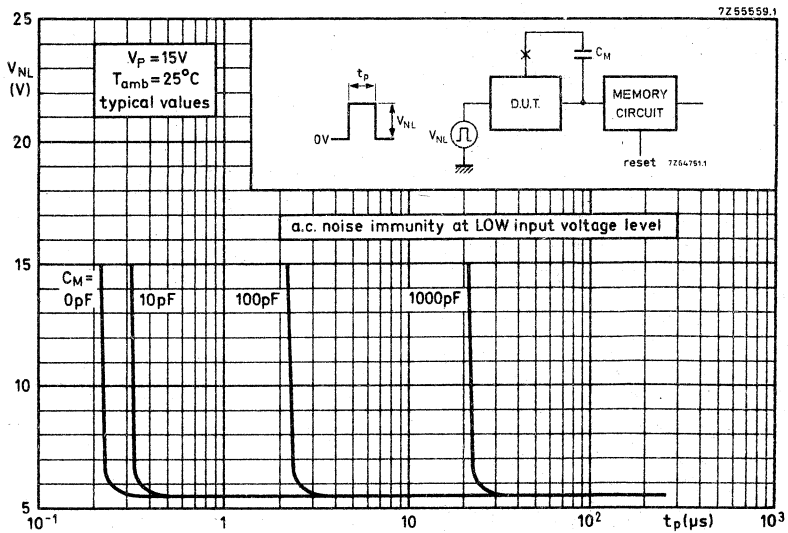
1) Voltage steps within the specified supply limits are allowed.

2) Can be increased to raise a. c. noise threshold.

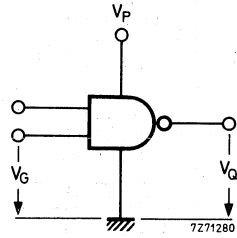
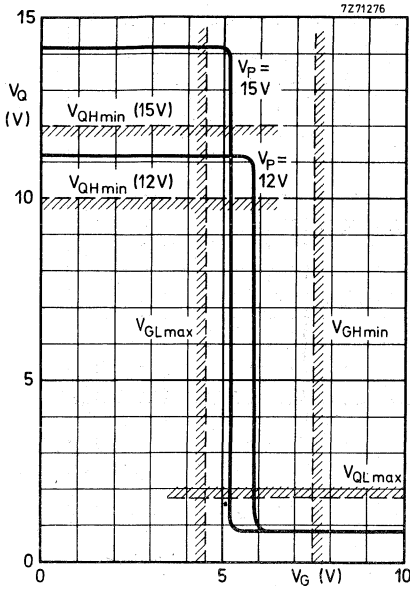
3) Only one output may be shorted at a time.



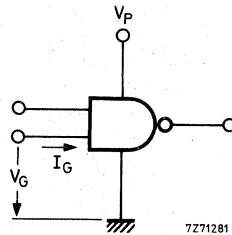
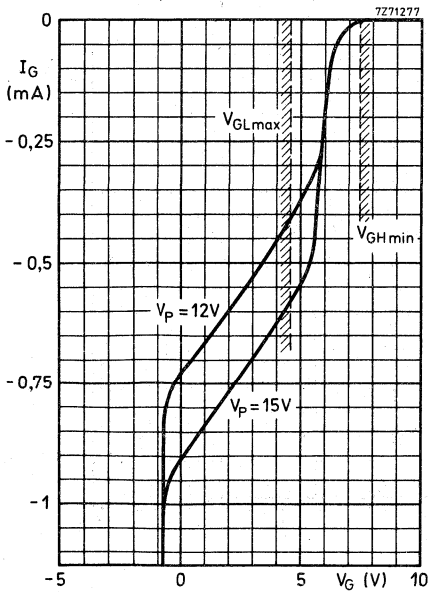
Typical curves for HIGH-input voltage level.



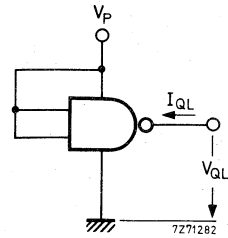
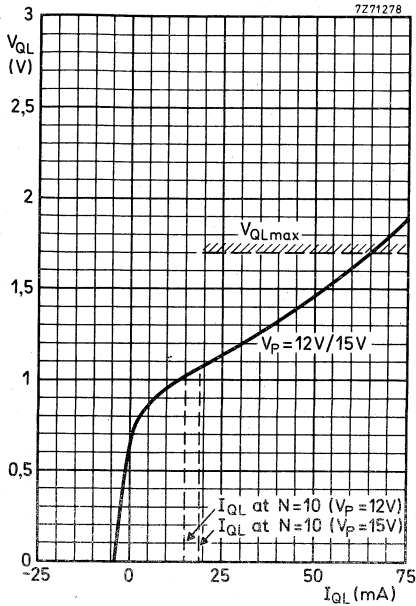
Typical curves for LOW-input voltage level.



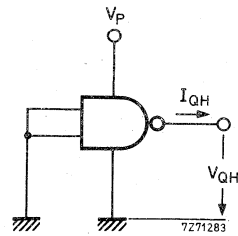
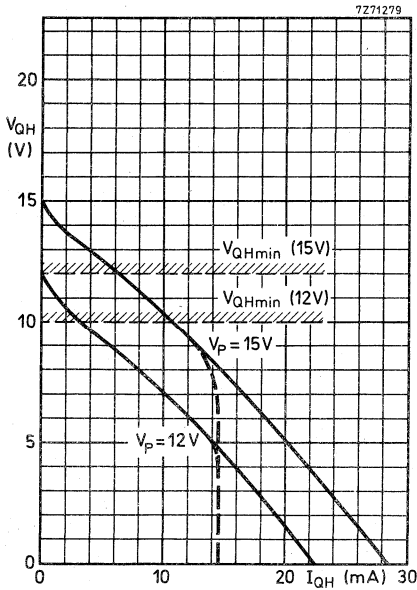
Typical transfer function of NAND gates at $V_P = 12\text{ V}$ and $V_P = 15\text{ V}$.



Typical input characteristic of NAND gates.



Typical output characteristic of the LOW-state outputs at $V_P = 12V, 15V$.



Typical output characteristic of the HIGH-state
 — FZH101 to FZH171, FZJ101 and FZJ111
 - - - FZH191 to FZH291, FZJ121 to FZJ161,
 and FZK101.

LOADING TABLE ($T_{amb} = 0$ to $+70$ °C; $V_P = 15$ V)

type	function	input (D.U.)		output (D.U.)	
		terminal	required	terminal	available
FZH101/4. NAND32	Quad 2-input NAND	G1 - G8	1	Q1 - Q4	10
FZH111/4. NAND30	Quad 2-input NAND	G1 - G8	1	Q1 - Q4	10
FZH121/2. NAND30	Dual 5-input NAND	G1 - G10	1	Q1 ; Q2	10
FZH131/2. NAND31	Dual 5-input NAND	G1 - G10	1	Q1 ; Q2	10
FZH141/2. NAND32	Dual 5-input power NAND	G1 - G10	1	Q1 ; Q2	30
FZH151/2. AOR30	Dual AND-AND-OR	G2, G3, G9, G10 other gates	1, 5	Q1 ; Q2	16
FZH161/4. LI31	Quad logic interface HNIL to 5 V logic	G2 - G5 G1, G6	1 2	Q1 - Q4	$V_{QL} \leq 0,4$ V $I_{QL} = 20$ mA $V_P = 13,5$ V
FZH171/2. NAND33	Dual 4-input NAND	G1 - G8	1	Q1 ; Q2	10
FZH181/4. LI30	Quad logic interface 5 V to HNIL	G1 - G8	1	Q1 - Q4	27
FZH191/3. NAND33	Triple 3-input NAND	G1 - G9	1	Q1 - Q3	10
FZH201/6. IN30	Sextuple inverter with strobe input	G1 - G6	1	Q1 - Q6	10
FZH211/4. NAND34	Quad 2-input NAND	G1 - G8	1	Q1 - Q4	10
FZH231/2. NAND35	Dual 5-input NAND	G1 - G10	1	Q1 ; Q2	10
FZH241/2. AST30	Dual 4-input NAND Schmitt trigger	G1 - G8	1	Q1 ; Q2	10
FZH251/4. AND30	Quad 2-input AND	G1 - G8	1	Q1 - Q4	10
FZH261/2. N-4. I30	Dual NAND/Quad inverter	G1 - G8	1	Q1 - Q6	10
FZH271/4. EO30	Quad EXCLUSIVE-OR	G1 - G8	1	Q1 - Q4	10

LOADING TABLE (continued)

type	function	input (D.U.)		output (D.U.)	
		terminal	required	terminal	available
FZH281/4, NOR30	Quad NOR	G1-C8	1	Q1-Q4	10
FZH291/4, OR30	Quad OR	G1-C8	1	Q1-Q4	10
FZJ101/FF30	Single JK master-slave flip-flop	J1;J2;K1;K2 T	1	Q1;Q2	10
FZJ111/FF31	Single JK master-slave flip-flop	S1;S2 J1;J2;K	1, 5 1	Q1;Q2	10
FZJ121/2, FF32	Dual JK master-slave flip-flop	S1;S2 J1;J2;K1;K2 T1;T2	1, 5 1	Q1-Q4	10
FZJ131/4, FF33	Quad D-type latch flip-flop	S1-S4 D1-D4 T1;T2	1, 5 2	Q1-Q8	10
FZJ141/FF34	Single synchronous decimal counter	all inputs	4	QA;QB;QC;QD	10
FZJ151/FF35	Single synchronous 4-bit binary counter	all inputs	1	QA;QB;QC;QD	10
FZJ161/FF36	Single synchronous 4-bit shift register	C5 input all other inputs	4	QA;QB;QC;QD	10
FZK101/OS30	Monostable multivibrator	G1-C4	1	Q	10
FZL101/ND30	Single BCD-decimal decoder N.I.T. driver	I1;I2;I4;I8	1	Q0-Q9	10

I_{QH} = 50 mA } input comb.
V_{QH} = 70 V } 0 to 9
I_{QH} = 5 mA } input comb.
V_{QH} = 60 V } 10 to 15



LOADING TABLE (continued)

type	function	input (D. U.)		output (D. U.)	
		terminal	required	terminal	available
2. LR30	Dual lamp/relay driver	G1:C2 E1:E2	3 3 (max 15 Si-diodes)	Q1:Q2	$I_{QL} \leq 200 \text{ mA}$ $V_{Pmax} = 17 \text{ V}$
PA30	Power amplifier	G	$I_{GL} = 5,1 \text{ mA}$; $V_{GL} = 1,7 \text{ V}$	Q	$I_{QL} = 2 \text{ A}$ $V_{QL} = 1,3 \text{ V}$
TU	Timer unit	G	$I_{GL} = 0,95 \text{ mA}$ $V_{GL} = 1,7 \text{ V}$ $V_P = 11,4 \text{ V}$ } $I_{GL} = 1,6 \text{ mA}$ $V_{GL} = 1,7 \text{ V}$ $V_P = 17 \text{ V}$ }	Q	22

NOTE

The figures quoted above for the fan-out in Drive Units (D. U.) are calculated for worst-case conditions: input Drive Units are simply added together to find the output Drive Units that the driving stage should be capable of supplying. To interface with other sorts of circuit, Drive Units can be interpreted as having the values shown below. These values are not applicable to the table.

LOW level:

- 1 input D.U. : 1,8 mA at 0 to 1,7 V
- 1 output D.U. : 1,5 mA at 1,7 V

HIGH level:

- input voltage = between 10 V and V_P
- output voltage = between $0,75 \times V_P$ and V_P

LETTER SYMBOLS

1. General

The voltages and currents are related to the terminals to which they are applied or at which they appear. Each terminal is indicated by a letter relating to the function of the device or the function of the pertinent signal.

In order to avoid confusion by any ambiguity in logical conventions, signal levels are indicated by H (= HIGH, for the more positive potential) and L (= LOW, for the less positive potential). Where circuit functions or logical equations are involved, the logical convention is mentioned specifically (for positive logic: H = 1, and for negative logic: H = 0).

2. Terminal designations

CE = condition enable for output QE

CQ = slow-down terminal

CT = condition enable trigger at input T

D = D input of D-type latch flip-flops

E = expander input (if necessary, this letter may be followed by a subscript, e.g. E₁ or E₂ or by one of the input letters, such as EG = gate expander input)

G = gate input

J, K = J, K input of JK flip-flops

N = negative supply

P = positive supply

Q = output

QE = output enable

R = direct Reset input

S = direct Set input

T = trigger (or toggle) input

ϕ = common supply return and voltage reference

3. Subscript sequence for voltages and currents

First subscript : terminal designation letter.

Second subscript : H (for HIGH) or L (for LOW), if applicable.

Third subscript : min or max, if applicable.

Examples : VP, IQL, V_{QHmin}, I_{PH} (in the latter case H denotes that the output level is HIGH).

4. Polarity of current and voltage

A current is defined as positive when its conventional direction of flow is into the device.

Unless otherwise specified, a voltage is measured with respect to the reference terminal (ϕ). Its polarity is defined as positive when the potential is higher than that of the reference terminal.

5. Time designations

If required for reasons of unambiguity, the related terminals may be included in the designations given below (e.g. t_{fQ1}).

t_f = fall time (transition from HIGH to LOW, see Fig. 1)

t_{hold} = hold time

t_H = signal HIGH duration (Fig. 1)

t_L = signal LOW duration (Fig. 1)

t_{pd} = average propagation delay time, defined as $\frac{t_{pdr} + t_{pdf}}{2}$

t_{pdf} = fall propagation delay time (output voltage falling, see Fig. 2)

t_{pdr} = rise propagation delay time (output voltage rising, see Fig. 2)

t_r = rise time (transition from LOW to HIGH, see Fig. 1)

t_{rec} = recovery time

t_{sc} = duration of short circuit (from relevant terminal to common return terminal)

t_{su} = set-up time

V_{pd} = reference voltage level for propagation delay measurement

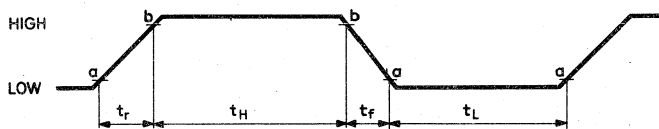


Fig. 1

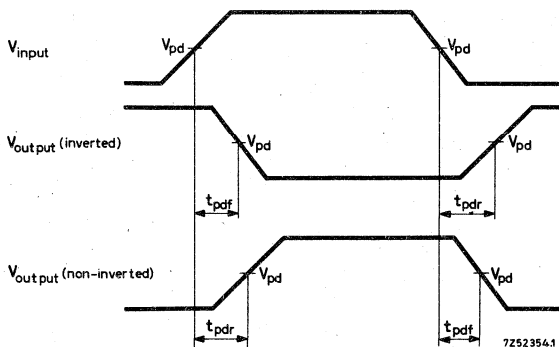
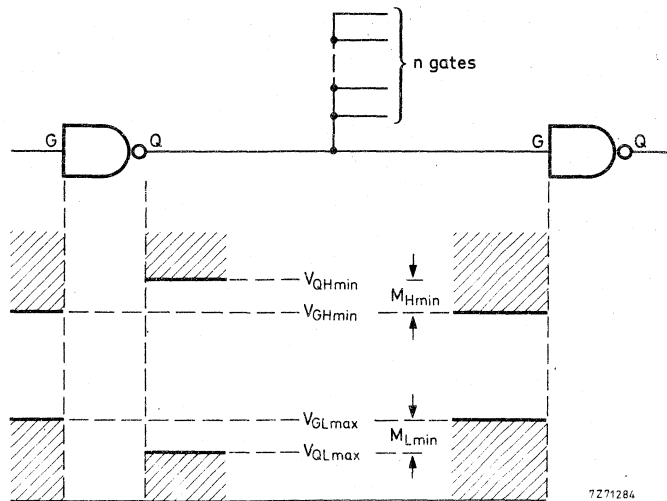


Fig. 2

6. Other designations

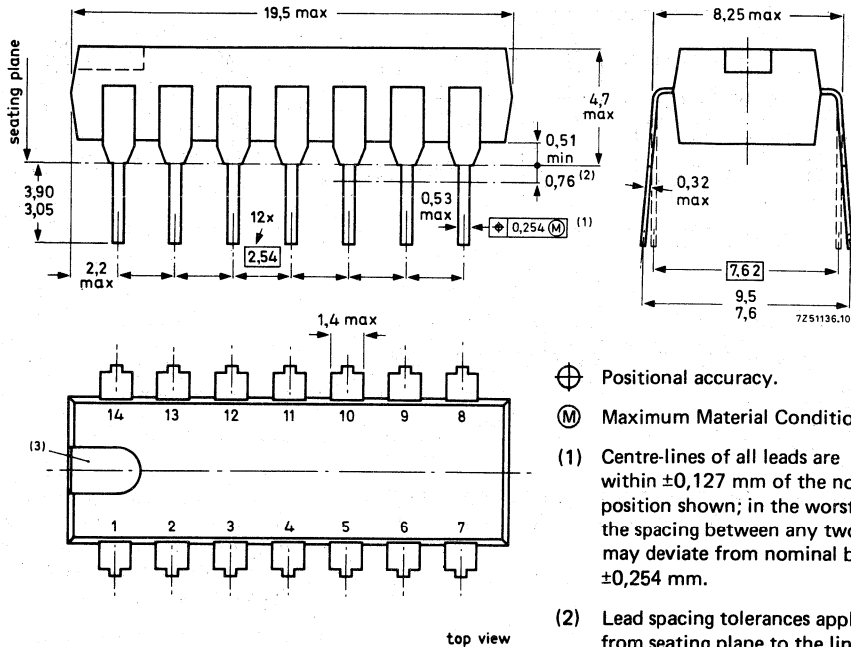
- i. c. = internally connected
Terminals with this indication should be left open. Otherwise correct working cannot be ensured; the device may even be damaged
- I_p = supply current
The logic state of the device indicated by H of L is normally referred to the output level, unless otherwise specified
- I_{pmax} = supply current
Maximum d. c. value under defined conditions
- M = d. c. noise margin



- M_L = d. c. noise margin, signal level LOW
(defined as: $M_L = V_{GLmax} - V_{QLmax}$ under defined loading, temperature and supply voltage conditions)
- M_H = d. c. noise margin, signal level HIGH
(calculated from: $M_H = V_{QHmin} - V_{GHmin}$ under defined loading, temperature and supply voltage conditions)
- N_{aL} = available d. c. fan-out (defined as: $N_{aL} = \frac{I_{QLmax}}{-I_{GLmax}}$ under defined temperature and supply voltage conditions)
- N_{aH} = available d. c. fan-out (defined as: $N_{aH} = \frac{-I_{QHmax}}{I_{GHmax}}$ under defined temperature and supply voltage conditions)
- P_H;P_L = power consumption, defined as the product of the supply current(s) and of the corresponding supply voltage(s). The logical state of the device, indicated by a letter subscript H or L, is normally referred to the output level, unless otherwise specified

- P_{av} = average power consumption at 50% duty cycle, unless otherwise specified. It is defined as: $P_{av} = V_P \cdot \frac{I_{PH} + I_{PL}}{2}$
- P_{tot} = power dissipation, defined as the total power dissipated by the device. It is the sum of the products of all currents and voltages at each of the input, output and supply terminals, their polarities being taken into account. The logical state of the device indicated by a letter subscript H or L is normally referred to the output level, unless otherwise specified
- T_{amb} = operating ambient temperature, i.e. the temperature of the free air in which the normally operating device is placed without external heat conduction, unless otherwise specified
- T_{stg} = storage temperature, i.e. the temperature of the ambient medium in which the non-operating device is stored
- V_{GLmax} = input voltage LOW at terminal G. With the specified level applied to the input of an inverting gate the output level will not be lower than the specified value V_{QHmin} at given I_{QH} .
- V_{GHmin} = input voltage HIGH at terminal G. With the specified level applied to the input of an inverting gate the output level will not exceed the specified value V_{QLmax} at given I_{QL} .
- V_H = hysteresis ($V_H = V_{TP} - V_{TN}$)
- V_{TP} = positive-going threshold voltage
- V_{TN} = negative-going threshold voltage
- ΔV_Q = change of output voltage caused by a specified change of output current

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27S, T, V)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

(3) Index may be horizontal as shown, or vertical.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).

If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

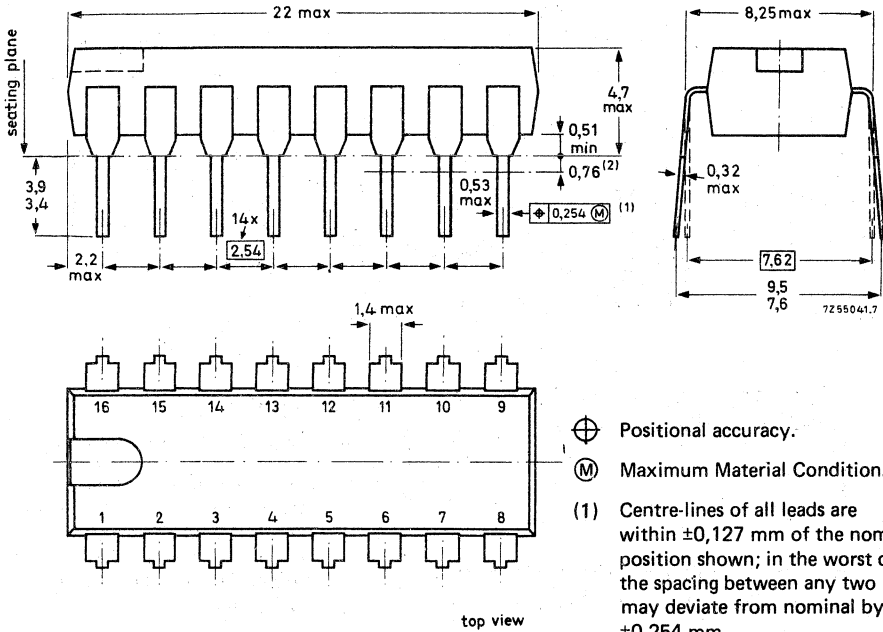
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38)



Dimensions in mm

- ⊕ Positional accuracy.
- Ⓜ Maximum Material Condition.

- (1) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by $\pm 0,254$ mm.
- (2) Lead spacing tolerances apply from seating plane to the line indicated.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

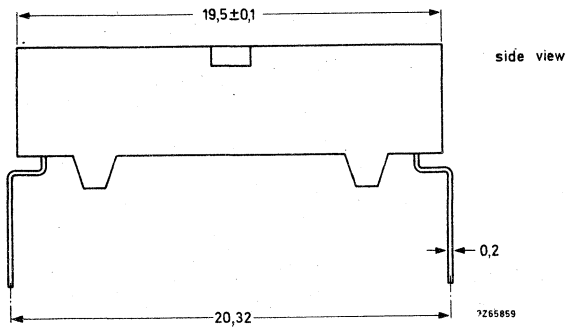
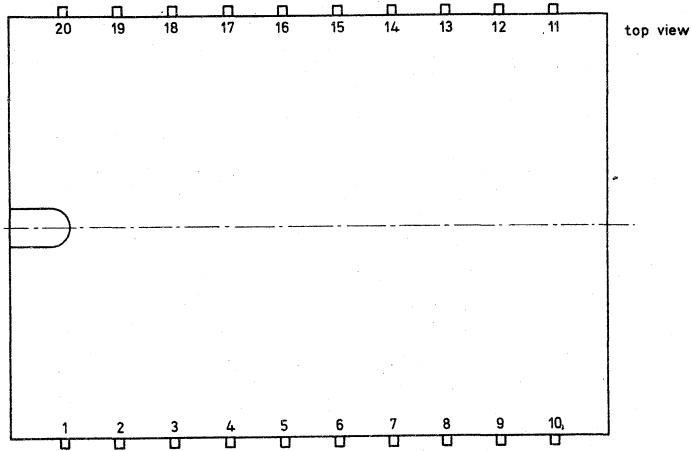
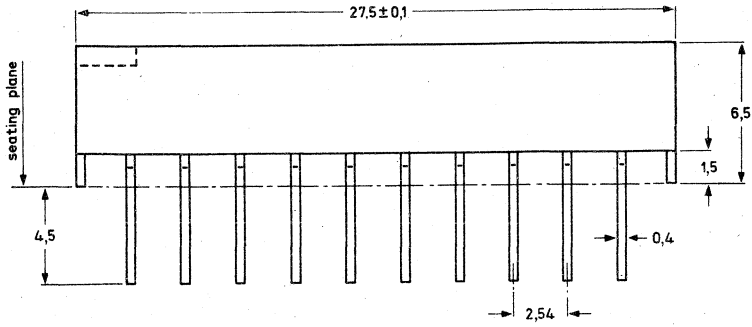
The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

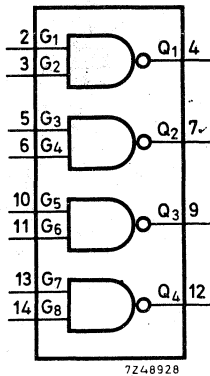
20 LEAD DUAL IN-LINE



The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

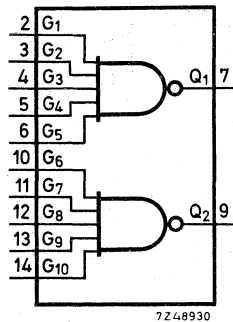
QUADRUPLE 2-INPUT NAND GATE

DUAL 5-INPUT NAND GATE



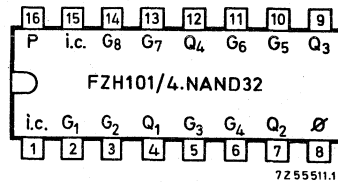
7Z48928

FZH101/4.NAND32

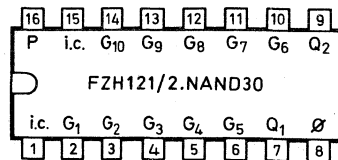


7Z48930

FZH121/2.NAND30



7255511.1



7255513.1

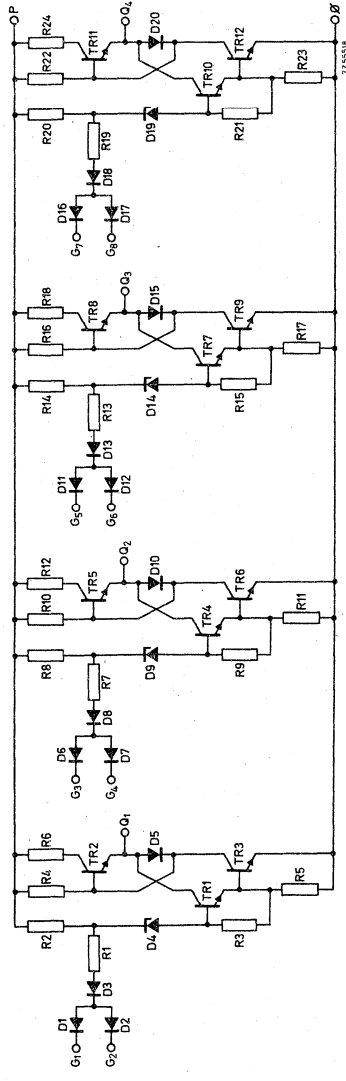
QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12 V
(range II)	V_P	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4, 5$ V)	t_{pd}	typ.	170 ns
Available d.c. fan-out } LOW state ($T_{amb} = 0$ to +70 °C)	N_{aL}	max.	10
D.C. noise margin at $T_{amb} = 25$ °C			
range I: $V_P = 12$ V	$M_L = M_H$	typ.	5 V
range II: $V_P = 15$ V	M_L	typ.	5 V
	M_H	typ.	8 V
Power consumption per gate at $T_{amb} = 25$ °C			
(50% duty cycle) range I: $V_P = 12$ V	P_{av}	typ.	16 mW
range II: $V_P = 15$ V	P_{av}	typ.	27 mW

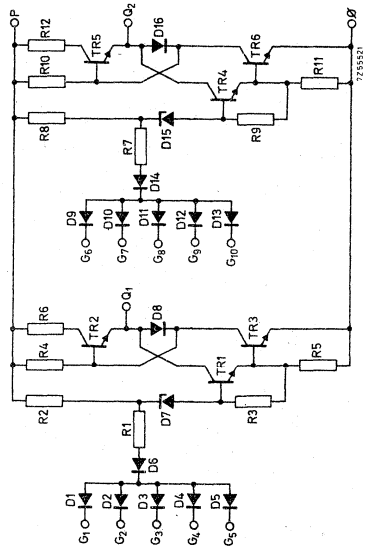
The FZH101/4.NAND32 and FZH121/2.NAND30 consists of a number of independent NAND gates without slow-down capability.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAMS
FZH101/4.NAND32

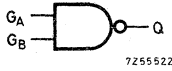


FZH121/2.NAND30



LOGIC FUNCTION

FZH101/4.NAND32

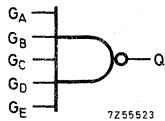


$$Q = \overline{G_A \cdot G_B} \text{ (positive logic)}$$

Function tables

G _A	G _B	Q
L	X	H
X	L	H
H	H	L

FZH121/2.NAND30



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E} \text{ (positive logic)}$$

G _A	G _B	G _C	G _D	G _E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V _P	max.	18 V
Output voltage	V _Q	max.	V _P
Input voltage	V _G	max.	18 V
Input current at V _P = 17 V	-I _{GL}	max.	25 mA
Voltage difference between any two inputs		max	18 V
Storage temperature	T _{stg}		-65 to +150 °C
Operating ambient temperature	T _{amb}		0 to +70 °C
Output short-circuit duration	t _{Qsc}	max.	1 s ¹⁾

¹⁾ Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70	°C
Uniform system supply voltage (range I)	V_P	11,4 to 13,5	V
	V_P	13,5 to 17	V
Available d.c. fan-out	N_{aL}	max. 10	
	N_{aH}	max. 100	
D.C. noise margin; range I at V_{Pmin}	M_L	min. 2,8	V
	M_H	min. 2,5	V
range II at V_{Pmin}	M_L	min. 2,8	V
	M_H	min. 4,5	V
Supply current per gate	range I ; output HIGH	I_{Pav}	typ. 0,9 mA
		I_{Pav}	typ. 1,7 mA
	output LOW	I_{Pav}	typ. 1,2 mA
		I_{Pav}	typ. 2,3 mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max. 31	mW
	P_{tot}	max. 52	mW
at range II; V_{Pmax}			
Thermal resistance from system to ambient	R_{th}	max. 150	°C/W



CHARACTERISTICS Test conditions: at range I ($V_P = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{GH}	7,5	-	-	V	11,4 $\left\{ \begin{array}{l} V_{QL} \leq 1,7\text{ V} \\ I_{QL} = 15\text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5 $\left\{ \begin{array}{l} V_{QH} \geq 10\text{ V} \\ -I_{QH} = 15\text{ mA} \end{array} \right.$
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5 $\left\{ \begin{array}{l} V_{GL} = 4,5\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4 $\left\{ \begin{array}{l} V_{GH} = 7,5\text{ V} \\ I_{QL} = 15\text{ mA} \end{array} \right.$
D.C. noise margin: HIGH LOW	M_H	2,5	5,0	-	V	11,4
	M_L	2,8	5,0	-	V	11,4
<u>Currents (per gate)</u>						
Input HIGH	I_{GH}	-	-	1,0	μA	13,5 $\left\{ \begin{array}{l} V_{GH} = 13,5\text{ V} \\ \text{other inputs } 0\text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5 $\left\{ \begin{array}{l} V_{GL} = 1,7\text{ V} \\ \text{other inputs } 13,5\text{ V} \end{array} \right.$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5 $\left\{ \begin{array}{l} V_{GL} = 4,5\text{ V} \\ V_{QH} = 10\text{ V} \end{array} \right.$
Output LOW	I_{QL}	15	-	-	mA	11,4 $\left\{ \begin{array}{l} V_{GH} = 7,5\text{ V} \\ V_{QL} = 1,7\text{ V} \end{array} \right.$
Output short-circuited ²⁾	$-I_{Qsc}$	10	30	50	mA	13,5 $V_G = 0\text{ V}; V_Q = 0\text{ V}$
Supply data						
<u>Currents (per gate)</u>						
at V_{QH}	I_P	-	0,9	1,6	mA	13,5 $V_G = 0\text{ V}$
at V_{QL}	I_P	-	1,7	3,0	mA	13,5 $V_G = 13,5\text{ V}$
Dynamic data						
<u>Times</u>						
Propagation delay:						
fall time	t_{pdf}	90	175	310	ns	12
rise time	t_{pdr}	90	175	310	ns	12
output rise time	t_r	200	340	570	ns	12
output fall time	t_f	70	120	210	ns	12
$C_L = 10\text{ pF}; N = 1$						
$T_{amb} = 25\text{ }^\circ\text{C}$						
$V_{pd} = 4,5\text{ V}$						

¹⁾ All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

²⁾ Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_P = 15 \text{ V}$); $T_{amb} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

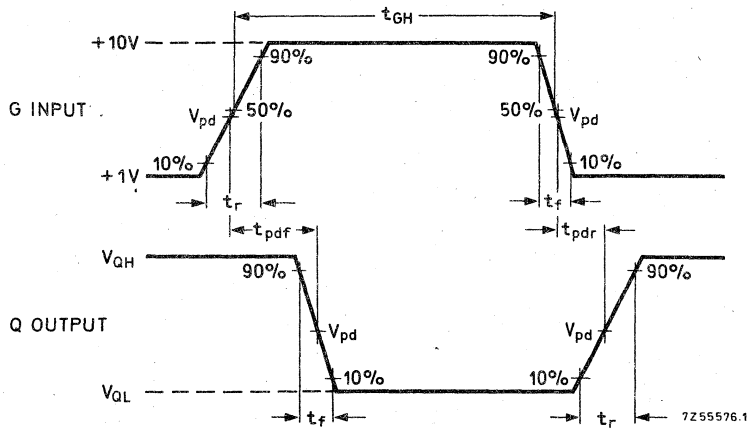
	Sym- bol	min. typ. ¹⁾ max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{GH}	7,5	-	-	V	13,5 { $V_{QL} \leq 1,7 \text{ V}$ $I_{QL} = 18 \text{ mA}$
Input LOW	V_{GL}	-	-	4,5	V	13,5 { $V_{QH} \geq 12 \text{ V}$ and 17 { $-I_{QH} = 0,1 \text{ mA}$
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 { $V_{GL} = 4,5 \text{ V}$ and 17 { $-I_{QH} = 0,1 \text{ mA}$
Output LOW	V_{QL}	-	1,0	1,7	V	13,5 { $V_{GH} = 7,5 \text{ V}$ $I_{QL} = 18 \text{ mA}$
D.C. noise margin: HIGH LOW	M_H	4,5	8,0	-	V	13,5
	M_L	2,8	5,0	-	V	
<u>Currents (per gate)</u>						
Input HIGH	I_{GH}	-	-	1,0	μA	17 { $V_{GH} = 17 \text{ V}$ other inputs 0 V
Input LOW	$-I_{GL}$	-	1,0	1,8	mA	17 { $V_{GL} = 1,7 \text{ V}$ other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17 { $V_{GL} = 4,5 \text{ V}$ $V_{QH} = 12 \text{ V}$
Output LOW	$-I_{QL}$	18	-	-	mA	13,5 { $V_{GH} = 7,5 \text{ V}$ $V_{QL} = 1,7 \text{ V}$
Output short-circuited ²⁾	$-I_{Qsc}$	15	37	60	mA	17 $V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
<u>Supply data</u>						
<u>Currents (per gate)</u>						
at V_{QH}	I_p	-	1,2	2,1	mA	17 $V_G = 0 \text{ V}$
at V_{QL}	I_p	-	2,3	4,0	mA	17 $V_G = 17 \text{ V}$
<u>Dynamic data</u>						
<u>Times</u>						
Propagation delay:						
fall time	t_{pdf}	-	140	-	ns	15 { $C_L = 10 \text{ pF}; N = 1$ $T_{amb} = 25 \text{ }^\circ\text{C}$
rise time	t_{pdr}	-	195	-	ns	
output rise time	t_r	-	410	-	ns	15 { $V_{pd} = 4,5 \text{ V}$
output fall time	t_f	-	75	-	ns	

1) All typical values under test conditions : $T_{amb} = 25 \text{ }^\circ\text{C}$ and $V_P = 15 \text{ V}$.

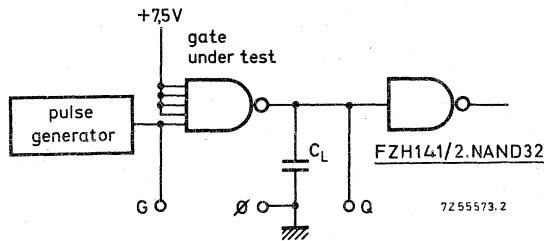
2) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): $t_R = 350 \text{ ns}$ $V_{pd} = +4,5 \text{ V}$
 $t_f = 120 \text{ ns}$
 $t_{GH} = 1 \mu\text{s}$

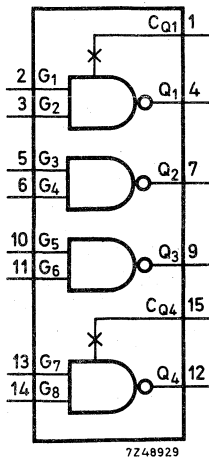


Measuring conditions: $V_P = +12 \text{ V}; +15 \text{ V}$
 $C_L = 10 \text{ pF}$ (including probe and jig capacitance)
 $T_{amb} = 25 \text{ }^\circ\text{C}$

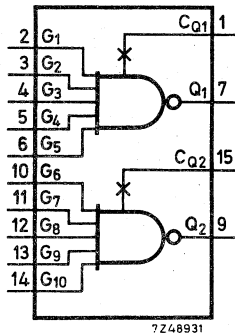
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

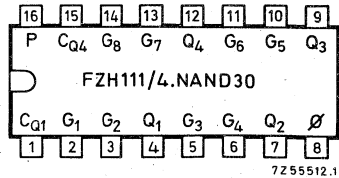
QUADRUPLE 2-INPUT NAND GATE
DUAL 5-INPUT NAND GATE
both having slow-down capability



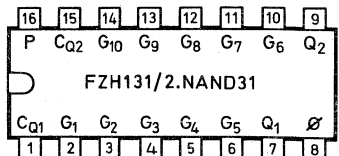
FZH111/4.NAND30



FZH131/2.NAND31



7255512.1



7255514.1

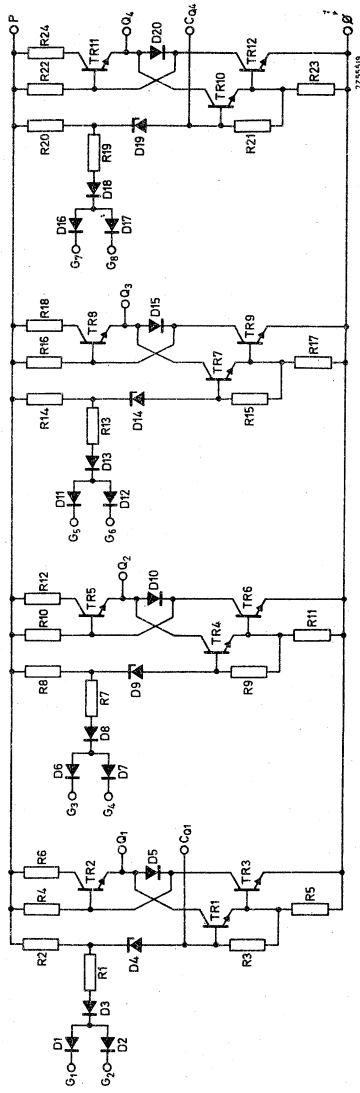
QUICK REFERENCE DATA

Supply voltage (range I)	V_p	nom.	12 V
(range II)	V_p	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4, 5$ V)	t_{pd}	typ.	170 ns
Available d. c. fan-out ($T_{amb} = 0$ to +70 °C)	N_{aL}	max.	10
D. C. noise margin at $T_{amb} = 25$ °C	$M_L = M_H$	range I ; $V_p = 12$ V	typ. 5 V
		range II ; $V_p = 15$ V	typ. 5 V
			typ. 8 V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_p = 12$ V	P_{av}	typ.	16 mW
	range II : $V_p = 15$ V	P_{av}	typ. 27 mW

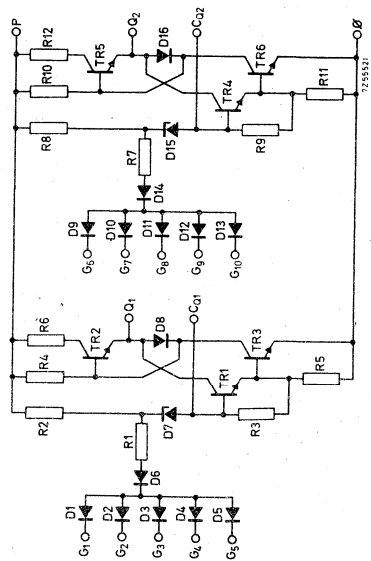
The FZH111/4.NAND30 and FZH131/2.NAND31 consist of a number of independent NAND gates at which two NAND gates per type have a special terminal (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAMS
FZH111/4.NAND30

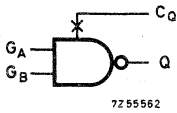


FZH131/2.NAND31



LOGIC FUNCTION

FZH111/4.NAND30

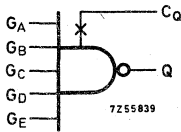


$$Q = \overline{G_A \cdot G_B} \text{ (positive logic)}$$

Function tables

G _A	G _B	Q
L	X	H
X	L	H
H	H	L

FZH131/2.NAND31



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E} \text{ (positive logic)}$$

G _A	G _B	G _C	G _D	G _E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V _P	max.	18 V
Output voltage	V _Q	max.	V _P
Input voltage	V _G	max.	18 V
Input current at V _P = 17 V	-I _{GL}	max.	25 mA
Voltage difference between any two inputs		max.	18 V
Storage temperature	T _{stg}		-65 to +150 °C
Operating ambient temperature	T _{amb}		0 to +70 °C
Output short-circuit duration	t _{Qsc}	max.	1 s ¹⁾
Slow-down input voltage	+V _{CQ}	max.	0,6 V
	-V _{CQ}	max.	1,0 V
Slow-down input current	+I _{CQ}	max.	2,0 mA
	-I _{CQ}	max.	10,0 mA

¹⁾ Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70 °C		
Uniform system supply voltage (range I)	V_P	11,4 to 13,5 V		
(range II)	V_P	13,5 to 17 V		
Available d. c. fan-out	N_{aL}	max. 10		
	N_{aH}	max. 100		
D. C. noise margin; range I at V_{Pmin}	M_L	min. 2,8 V		
	M_H	min. 2,5 V		
range II at V_{Pmin}	M_L	min. 2,8 V		
	M_H	min. 4,5 V		
Supply current per gate	} range I ; output HIGH	I_{Pav}	typ. 0,9 mA	
		} output LOW	I_{Pav}	typ. 1,7 mA
			} range II; output HIGH	I_{Pav}
		} output LOW		I_{Pav}
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max. 31 mW		
at range II ; V_{Pmax}	P_{tot}	max. 52 mW		
Thermal resistance from system to ambient	R_{th}	max. 150 °C/W		



CHARACTERISTICS Test conditions: at range I ($V_P = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{GH}	7,5	-	-	V	11,4 { $V_{QL} \leq 1,7\text{ V}$ $I_{QL} = 15\text{ mA}$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5 { $V_{QH} \geq 10\text{ V}$ $I_{QH} = 0,1\text{ mA}$
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5 { $V_{GL} = 4,5\text{ V}$ $I_{QH} = 0,1\text{ mA}$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4 { $V_{GH} = 7,5\text{ V}$ $I_{QL} = 15\text{ mA}$
D.C. noise margin: HIGH	M_H	2,5	5,0	-	V	11,4
LOW	M_L	2,8	5,0	-	V	11,4
<u>Currents (per gate)</u>						
Input HIGH	I_{GH}	-	-	1,0	μA	13,5 { $V_{GH} = 13,5\text{ V}$ other inputs 0 V
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5 { $V_{GL} = 1,7\text{ V}$ other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5 { $V_{GL} = 4,5\text{ V}$ $V_{QH} = 10\text{ V}$
Output LOW	I_{QL}	15	-	-	mA	11,4 { $V_{GH} = 7,5\text{ V}$ $V_{QL} = 1,7\text{ V}$
Output short-circuited ²⁾	$-I_{Qsc}$	10	30	50	mA	13,5 $V_G = 0\text{ V}; V_Q = 0\text{ V}$
Supply data						
<u>Currents (per gate)</u>						
at V_{QH}	I_P	-	0,9	1,6	mA	13,5 $V_G = 0\text{ V}$
at V_{QL}	I_P	-	1,7	3,0	mA	13,5 $V_G = 13,5\text{ V}$
Dynamic data						
<u>Times</u>						
Propagation delay						
fall time	t_{pdf}	90	175	310	ns	12
rise time	t_{pdr}	90	175	310	ns	12
output rise time	t_r	200	340	570	ns	12
output fall time	t_f	70	120	210	ns	12
$C_L = 10\text{ pF}; N = 1$ $T_{amb} = 25\text{ }^\circ\text{C}$ $V_{pd} = 4,5\text{ V}$						

1) All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

2) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_p = 15 \text{ V}$); $T_{amb} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

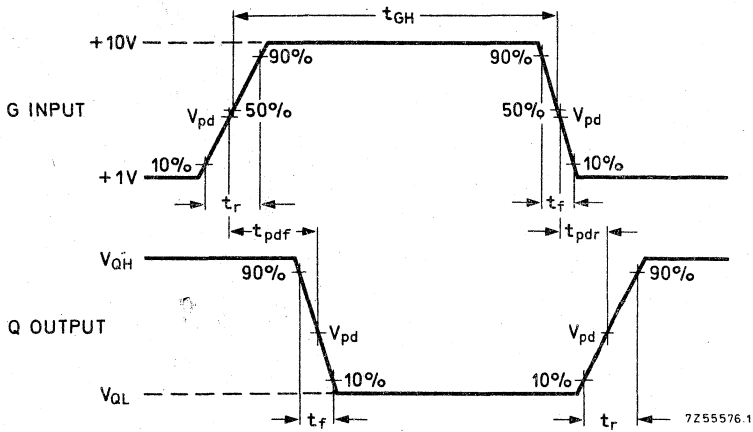
	Sym- bol	min. typ. ¹⁾ max.		Conditions and references		
				V _p (V)		
Static data						
<u>Voltages</u>						
Input HIGH	V _{GH}	7,5	- -	V	13,5	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
Input LOW	V _{GL}	-	-	4,5 V	13,5 and 17	$\left\{ \begin{array}{l} V_{QH} \geq 12 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output HIGH	V _{QH}	12,0	14,3	- V	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V _{QL}	-	1,0	1,7 V	13,5	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
D.C. noise margin: HIGH	M _H	4,5	8,0	- V	13,5	
LOW	M _L	2,8	5,0	- V	13,5	
<u>Currents (per gate)</u>						
Input HIGH	I _{GH}	-	-	1,0 μA	17	$\left\{ \begin{array}{l} V_{GH} = 17 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	-I _{GL}	-	1,0	1,8 mA	17	$\left\{ \begin{array}{l} V_{GL} = 1,7 \text{ V} \\ \text{other inputs } 17 \text{ V} \end{array} \right.$
Output HIGH	-I _{QH}	0,1	-	- mA	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 12 \text{ V} \end{array} \right.$
Output LOW	I _{QL}	18	-	- mA	13,5	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ V_{QL} = 1,7 \text{ V} \end{array} \right.$
Output short-circuited ²⁾	-I _{Qsc}	15	37	60 mA	17	$V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
Supply data						
<u>Currents (per gate)</u>						
at V _{QH}	I _p	-	1,2	2,1 mA	17	$V_G = 0 \text{ V}$
at V _{QL}	I _p	-	2,3	4,0 mA	17	$V_G = 17 \text{ V}$
Dynamic data						
<u>Times</u>						
<u>Propagation delay</u>						
fall time	t _{pdf}	-	140	- ns	15	$\left. \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{amb} = 25 \text{ }^\circ\text{C} \\ V_{dp} = 4,5 \text{ V} \end{array} \right\}$
rise time	t _{pdr}	-	195	- ns	15	
output rise time	t _r	-	410	- ns	15	
output fall time	t _f	-	75	- ns	15	

1) All typical values under test conditions: $T_{amb} = 25 \text{ }^\circ\text{C}$ and $V_p = 15 \text{ V}$.

2) Short-circuit duration max. 1 s.

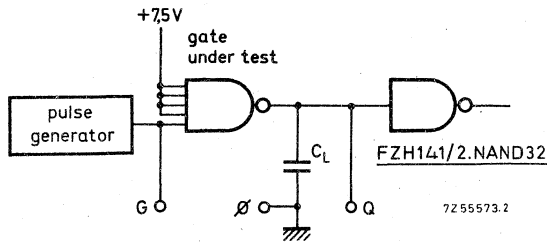
CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): $t_r = 350 \text{ ns}$
 $t_f = 120 \text{ ns}$
 $t_{GH} = 1 \mu\text{s}$

$V_{pd} = +4,5 \text{ V}$

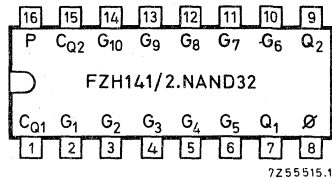
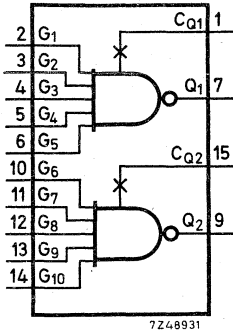


Measuring conditions: $V_P = +12 \text{ V}; +15 \text{ V}$
 $C_L = 10 \text{ pF}$ (including probe and jig capacitance)
 $T_{amb} = 25 \text{ }^\circ\text{C}$
Slow-down terminals are not connected

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL 5-INPUT POWER NAND GATE with slow-down capability



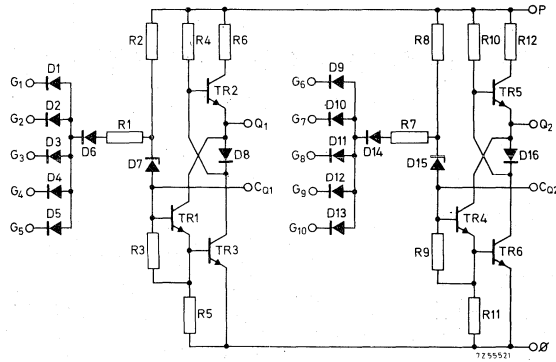
QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12 V
(range II)	V_P	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay (N = 1; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4, 5$ V)	t_{pd}	typ.	170 ns
Available d. c. fan-out ($T_{amb} = 0$ to +70 °C) } LOW state	N_{aL}	max.	30
D. C. noise margin at $T_{amb} = 25$ °C			
range I: $V_P = 12$ V	$M_L = M_H$	typ.	5 V
range II: $V_P = 15$ V	M_L M_H	typ.	5 V
		typ.	8 V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I: $V_P = 12$ V	P_{av}	typ.	16 mW
range II: $V_P = 15$ V	P_{av}	typ.	27 mW

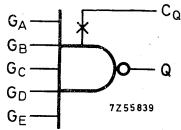
The FZH141/2.NAND32 is a dual 5-input power NAND gate with on each gate a special base connection (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$$

(positive logic)

Function table

GA	GB	GC	GD	GE	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Output voltage	V_Q	max.	V_P
Input voltage	V_G	max.	18 V
Input current at $V_P = 17$ V	$-I_{GL}$	max.	25 mA
Voltage difference between any two inputs		max.	18 V
Storage temperature	T_{stg}		-65 to +150 °C
Operating ambient temperature	T_{amb}		0 to +70 °C
Output short-circuit duration	t_{Qsc}	max.	1 s ¹⁾
Slow-down input voltage	$+V_{CQ}$	max.	0,6 V
	$-V_{CQ}$	max.	1,0 V
Slow-down input current	$+I_{CQ}$	max.	2,0 mA
	$-I_{CQ}$	max.	10,0 mA

¹⁾ Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70 °C
Uniform system supply voltage (range I) (range II)	V_P	11,4 to 13,5 V
	V_P	13,5 to 17 V
Available d. c. fan-out	N_{aL}	max. 30
	N_{aH}	max. 100
D. C. noise margin; range I at V_{Pmin}	M_L	min. 2,8 V
	M_H	min. 2,5 V
range II at V_{Pmin}	M_L	min. 2,8 V
	M_H	min. 4,5 V
Supply current per gate	range I; output HIGH	I_{Pav} typ. 0,9 mA
	output LOW	I_{Pav} typ. 1,7 mA
	range II; output HIGH	I_{Pav} typ. 1,2 mA
	output LOW	I_{Pav} typ. 2,3 mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max. 31 mW
	at range II ; V_{Pmax}	P_{tot} max. 52 mW
Thermal resistance from system to ambient	R_{th}	max. 150 °C/W



CHARACTERISTICS Test conditions: at range I ($V_p = 12\text{ V}$); $T_{\text{amb}} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references		
					V_p (V)		
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	11,4	$\left\{ \begin{array}{l} V_{QL} \leq 1,7\text{ V} \\ I_{QL} = 45\text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5	
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,3	1,7	V	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5\text{ V} \\ I_{QL} = 45\text{ mA} \end{array} \right.$
D. C. noise margin: HIGH LOW	M_H	2,5	5,0	-	V	11,4	
	M_L	2,8	5,0	-	V	11,4	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	13,5	$\left\{ \begin{array}{l} V_{GH} = 13,5\text{ V} \\ \text{other inputs } 0\text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5	$\left\{ \begin{array}{l} V_{GL} = 1,7\text{ V} \\ \text{other inputs } 13,5\text{ V} \end{array} \right.$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5\text{ V} \\ V_{QH} = 10\text{ V} \end{array} \right.$
Output LOW	I_{QL}	45	-	-	mA	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5\text{ V} \\ V_{QL} = 1,7\text{ V} \\ V_G = 0\text{ V}; V_Q = 0\text{ V} \end{array} \right.$
Output short-circuited ²⁾	$-I_{Qsc}$	10	30	50	mA	13,5	
<u>Supply data</u>							
<u>Currents (per gate)</u>							
at V_{QH}	I_p	-	0,9	1,6	mA	13,5	$\left\{ \begin{array}{l} V_G = 0\text{ V} \\ V_G = 13,5\text{ V} \end{array} \right.$
at V_{QL}	I_p	-	1,7	3,0	mA	13,5	
<u>Dynamic data</u>							
<u>Times</u>							
Propagation delay fall time rise time	t_{pdf}	90	175	310	ns	12	$\left\{ \begin{array}{l} C_L = 10\text{ pF}; N = 1 \\ T_{\text{amb}} = 25\text{ }^\circ\text{C} \\ V_{pd} = 4,5\text{ V} \end{array} \right.$
	t_{pdr}	90	175	310	ns	12	
output rise time output fall time	t_r	200	340	570	ns	12	
	t_f	70	120	210	ns	12	

1) All typical values under test conditions: $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ and $V_p = 12\text{ V}$.

2) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_p = 15$ V); $T_{amb} = 0$ to $+70$ °C

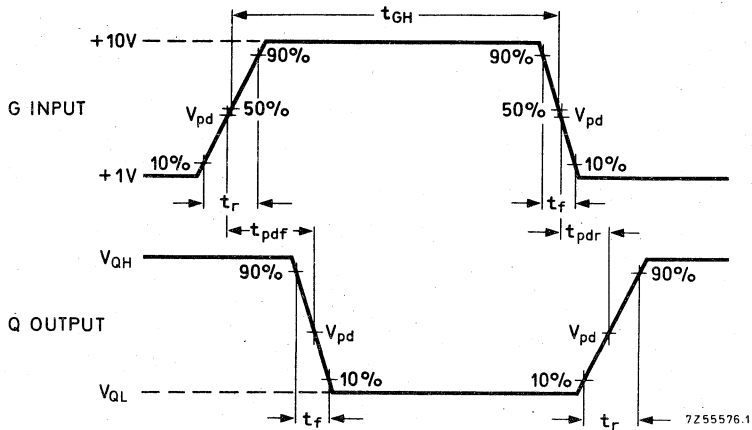
	Sym- bol	min. typ. 1) max.		Conditions and references		
				V_p (V)		
Static data						
<u>Voltages</u>						
Input HIGH	V_{GH}	7,5	-	- V	13,5	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 54 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5 V	13,5 and 17	
Output HIGH	V_{QH}	12,0	14,3	- V	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,4	1,7 V	13,5	
D. C. noise margin: HIGH	M_H	4,5	8,0	- V	13,5	
	M_L	2,8	5,0	- V	13,5	
<u>Currents (per gate)</u>						
Input HIGH	I_{GH}	-	-	1,0 μ A	17	$\left\{ \begin{array}{l} V_{GH} = 17 \text{ V} \\ \text{other inputs } 0 \text{ V} \\ V_{GL} = 1,7 \text{ V} \\ \text{other inputs } 17 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	-	1,8 mA	17	
Output HIGH	$-I_{QH}$	0,1	-	- mA	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 12 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	54	-	- mA	13,5	
Output short-circuited ²⁾	$-I_{Qsc}$	15	37	60 mA	17	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ V_{QL} = 1,7 \text{ V} \\ V_G = 0 \text{ V}; V_Q = 0 \text{ V} \end{array} \right.$
Supply data						
<u>Currents (per gate)</u>						
at V_{QH}	I_p	-	1,2	2,1 mA	17	$V_G = 0 \text{ V}$
at V_{QL}	I_p	-	2,3	4,0 mA	17	
Dynamic data						
<u>Times</u>						
Propagation delay fall time	t_{pdf}	-	140	- ns	15	$\left. \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{amb} = 25 \text{ }^\circ\text{C} \\ V_{dp} = 4,5 \text{ V} \end{array} \right\}$
		-	195	- ns	15	
output rise time	t_r	-	410	- ns	15	
output fall time	t_f	-	75	- ns	15	

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_p = 15$ V.

2) Short-circuit duration max. 1 s.

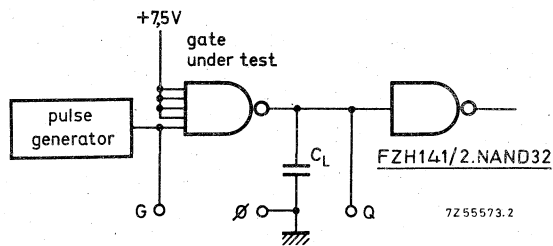
CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): t_r = 350 ns
 t_f = 120 ns
 t_{GH} = 1 μs

V_{pd} = +4,5 V

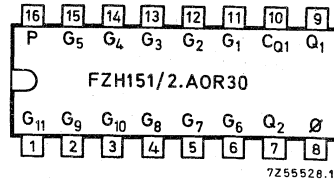
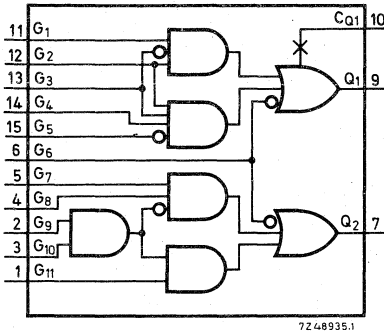


Measuring conditions: V_p = +12 V; +15 V
 C_L = 10 pF (including probe and jig capacitance)
 T_{amb} = 25 °C
 Slow-down terminals are not connected

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL AND-AND-OR GATE with slow-down capability



QUICK REFERENCE DATA

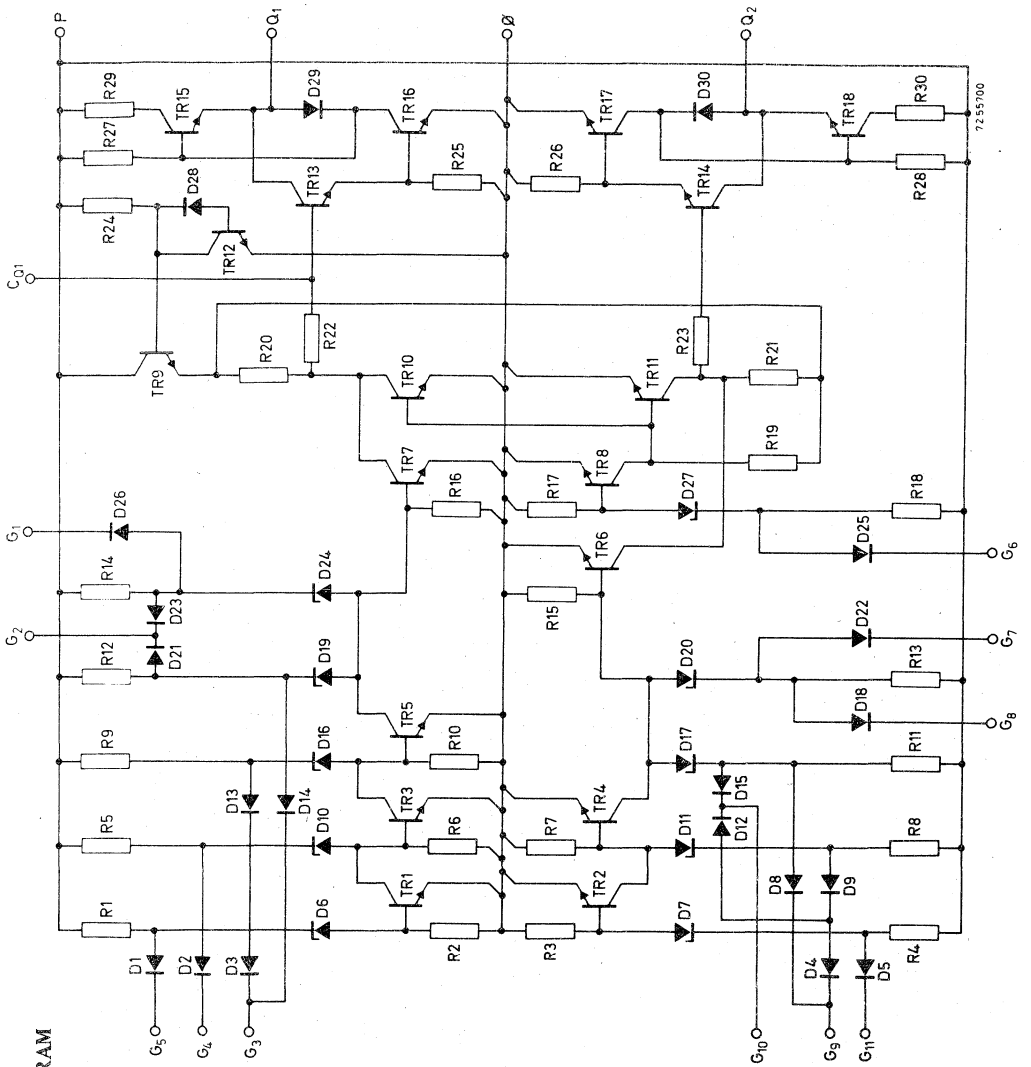
Supply voltage (range I)	V_P	nom.	12 V
(range II)	V_P	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4, 5$ V)	t_{pd}	typ.	380 ns
Available d. c. fan-out ($T_{amb} = 0$ to +70 °C) } LOW state	N_{aL}	max.	20 ¹⁾
	N_{aL}	max.	16 ²⁾
D. C. noise margin at $T_{amb} = 25$ °C			
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5 V
range II: $V_P = 15$ V	M_L	typ.	5 V
	M_H	typ.	8 V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	132 mW
range II: $V_P = 15$ V	P_{av}	typ.	225 mW

- 1) At FZH151/2.AOR30 load. }
 2) At HN1L gate load. } G_2, G_3, G_9 and G_{10} count for two inputs.

The FZH151/2.AOR30 consists of two combinations AND and OR gates with some common inputs to the AND gates and a common override input to the OR gates. One of the OR gates has a special terminal (C_{Q1}) to provide slow-down capability.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION

$$\left. \begin{aligned} Q_1 &= G_1 \cdot G_2 \cdot \overline{G_3} + G_2 \cdot G_3 \cdot G_4 \cdot \overline{G_5} + \overline{G_6} \\ Q_2 &= G_7 \cdot G_8 \cdot \overline{G_9} \cdot \overline{G_{10}} + G_9 \cdot G_{10} \cdot G_{11} + \overline{G_6} \end{aligned} \right\} \text{for positive logic}$$

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Output voltage	V_Q	max.	V_P
Input voltage	V_G	max.	18 V
Input current at $V_P = 17$ V	$-I_{GL}$	max.	25 mA
Voltage difference between any two inputs		max.	18 V
Slow-down input voltage	$+V_{CQ}$	max.	0,6 V
	$-V_{CQ}$	max.	1,0 V
Slow-down input current	$+I_{CQ}$	max.	2,0 mA
	$-I_{CQ}$	max.	10,0 mA
Storage temperature	T_{stg}		-65 to +150 °C
Operating ambient temperature	T_{amb}		0 to +70 °C
Output short-circuit duration	t_{Qsc}	max.	1 s ¹⁾

¹⁾ Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to 70	°C
Uniform system supply voltage (range I) (range II)	V_P	11, 4 to 13, 5	V
	V_P	13, 5 to 17	V
Available d. c. fan-out: at FZH151/2.AOR30 at HNIL gate load	N_{aL}	max. 20	*)
	N_{aL}	max. 16	
	N_{aH}	max. 100	
D. C. noise margin; range I at V_{Pmin} range II at V_{Pmin}	M_L	min. 2, 8	V
	M_H	min. 2, 5	V
	M_L	min. 2, 8	V
	M_H	min. 4, 5	V
Supply current per gate	range I ; output HIGH output LOW	I_{Pav}	typ. 14 mA
		I_{Pav}	typ. 8, 0 mA
	range II; output HIGH output LOW	I_{Pav}	typ. 18 mA
		I_{Pav}	typ. 12 mA
Power consumption per gate (50% duty cycle) at range I , V_{Pmax} at range II, V_{Pmax}	P_{tot}	max. 250	mW
	P_{tot}	max. 425	mW
Thermal resistance from system to ambient	R_{th}	max. 150	°C/W

*) G_2, G_3, G_9 and G_{10} count for two inputs.

CHARACTERISTICS Test conditions: at range I ($V_P = 12$ V); $T_{amb} = 0$ to $+70$ °C

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references		
					V_P (V)		
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	11,4	$\left\{ \begin{array}{l} V_{QL} = \max 1,7 \text{ V} \\ I_{QL} = 30 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	11,4	
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	
D.C. noise margin:HIGH	M_H	2,5	5,0	-	V		
	M_L	2,8	5,0	-	V		
<u>Currents</u>							
Input HIGH: $G_2; G_3; G_9; G_{10}$ at other G inputs	I_{GH}	-	-	2	μA	13,5	$\left\{ \begin{array}{l} V_{GH} = 13,5 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
	I_{GH}	-	-	1	μA		
Input LOW: $G_2; G_3; G_9; G_{10}$ at other G inputs	$-I_{GL}$	-	1,0	2,5	mA	13,5	$\left\{ \begin{array}{l} V_{GL} = 1,7 \text{ V} \\ \text{other inputs } 13,5 \text{ V} \end{array} \right.$
	$-I_{GL}$	-	0,5	1,25	mA		
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 10 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	30	-	-	mA	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ V_{QL} = 1,7 \text{ V} \end{array} \right.$
Output short-circuited 2)	$-I_{Qsc}$	10	30	50	mA	13,5	$V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
Supply data							
<u>Currents</u>							
at V_{QH}	I_P	-	14,0	22,0	mA	13,5	$V_G = 0 \text{ V}$
at V_{QL}	I_P	-	8,0	15,0	mA	13,5	$\left\{ \begin{array}{l} V_{G11} = V_{GL} \\ \text{other G inputs: } V_{GH} \end{array} \right.$

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_P = 12$ V.

2) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_P = 15$ V); $T_{amb} = 0$ to $+70$ °C

	Sym- bol	min. typ. 1) max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{GH}	7,5	-	-	V	13,5 { $V_{QL} = \text{max. } 1,7$ V $I_{QL} = 36$ mA
Input LOW	V_{GL}	-	-	4,5	V	13,5 { $V_{QH} = \text{min. } 12$ V $-I_{QH} = 0,1$ mA
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 { $V_{GL} = 4,5$ V $-I_{QH} = 0,1$ mA
Output LOW	V_{QL}	-	1,0	1,7	V	13,5 { $V_{GH} = 7,5$ V $I_{QL} = 36$ mA
D.C. noise margin:HIGH	M_H	4,5	8,0	-	V	13,5
LOW	M_L	2,8	5,0	-	V	13,5
<u>Currents</u>						
Input HIGH: $G_2; G_3; G_9; G_{10}$ at other G inputs	I_{GH}	-	-	2,0	μ A	17 { $V_{GH} = 17$ V other inputs 0 V
	I_{GH}	-	-	1,0	μ A	
Input LOW: $G_2; G_3; G_9; G_{10}$ at other G inputs	$-I_{GL}$	-	1,2	3,0	mA	17 { $V_{GL} = 1,7$ V other inputs 17 V
	$-I_{GL}$	-	0,6	1,5	mA	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 { $V_{GL} = 4,5$ V $V_{QH} = 12$ V
Output LOW	I_{QL}	30	-	-	mA	13,5 { $V_{GH} = 7,5$ V $V_{QL} = 1,7$ V
Output short-circuited 2)	$-I_{Qsc}$	15	37	60	mA	17 $V_G = 0$ V; $V_Q = 0$ V
Supply data						
<u>Currents</u>						
at V_{QH}	I_P	-	18	29	mA	17 $V_G = 0$ V
at V_{QL}	I_P	-	12	21	mA	17 { $V_{G11} = V_{GL}$ other G inputs: V_{GH}

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_P = 15$ V.

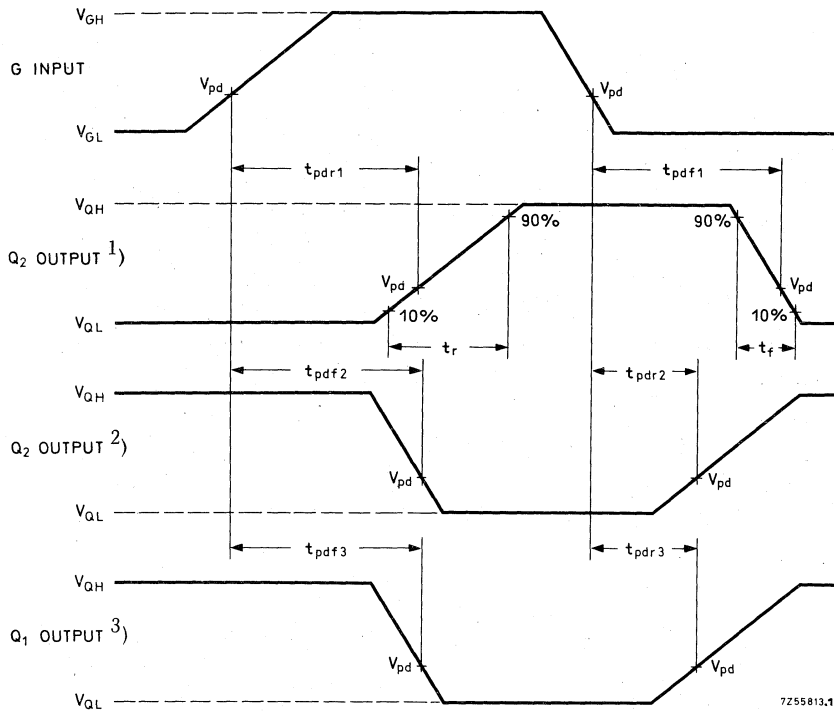
2) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

	Sym- bol	min. typ. 1) max.		Conditions and references	
				V _P (V)	
Dynamic data					
<u>Times</u>					
Propagation delay					
fall times at output Q	t _{pdf1}	- 230	- ns	12	} C _L = 10 pF N = 1 T _{amb} = 25 °C V _{pd} = 4,5 V
at output \bar{Q}	t _{pdf2}	- 300	- ns	12	
at input G ₅	t _{pdf3}	- 400	- ns	12	
rise times at output Q	t _{pdr1}	- 340	- ns	12	
at output \bar{Q}	t _{pdr2}	- 340	- ns	12	
at input G ₅	t _{pdr3}	- 270	- ns	12	
Output rise time	t _r	- 330	- ns	12	
Output fall time	t _f	- 200	- ns	12	

¹⁾ All typical values under test conditions: T_{amb} = 25 °C and V_P = 12 V.

CHARACTERISTICS (continued)



Waveforms illustrating measurement of t_{pdr} and t_{pdf}

1) If G input = G7, G8, G11.

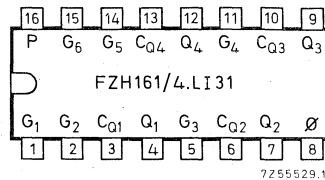
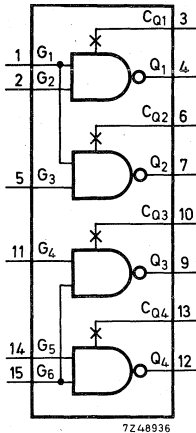
2) If G input = G6.

3) If G input = G5.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE LOGIC INTERFACE GATE

HNIL to 5 V logic; with slow-down capability



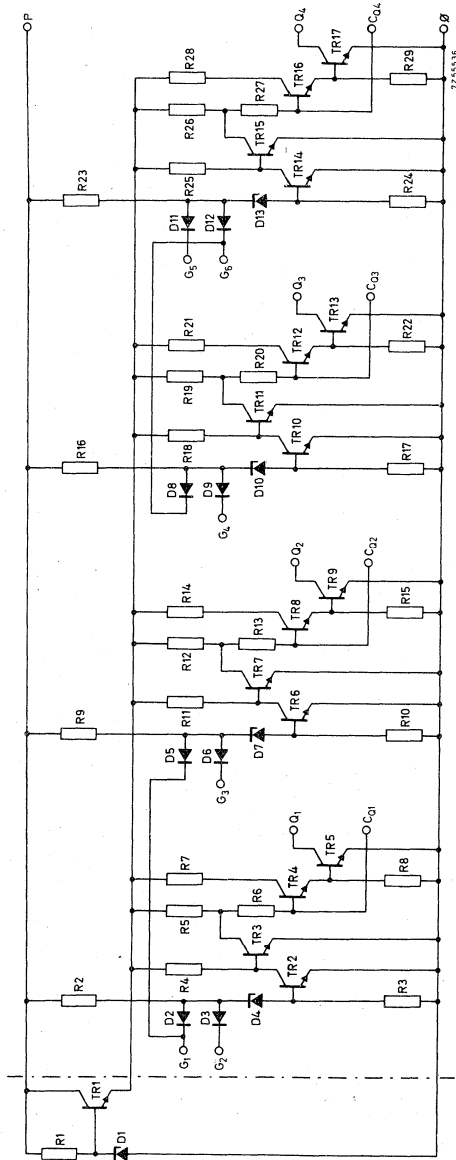
QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12 V
(range II)	V_P	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay			
$V_P = 12 V$; $N = 1$	} $V_Q = 12 V$	t_{pd1}	typ. 115 ns
$V_{pd} = 4,5 V$; $T_{amb} = 25 °C$		} $V_Q = 5 V$	t_{pd2}
D.C. noise margin at $T_{amb} = 25 °C$			
range I: $V_P = 12 V$	} $M_L = M_H$	$M_L = M_H$	typ. 5 V
range II: $V_P = 15 V$		M_L	typ. 5 V
		M_H	typ. 8 V
Power consumption per gate at $T_{amb} = 25 °C$			
(50% duty cycle) range I: $V_P = 12 V$	P_{av}	typ.	39 mW
range II: $V_P = 15 V$	P_{av}	typ.	55 mW

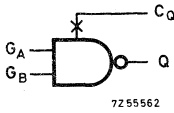
The FZH161/4.LI31 is a level converter with open-collector outputs for HNIL to TTL and consists of 4 gates and some common inputs. Each gate has slow-down capability.

PACKAGE OUTLINE 16 leads plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B}$$

(for positive logic)

Function table

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage (HIGH state)	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at $V_P = 17$ V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA
Storage temperature	T_{stg}		-65 to +150	°C
Operating ambient temperature	T_{amb}		0 to + 70	°C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70	$^{\circ}C$	
Uniform system supply voltage (range I)	V_P	11, 4 to 13, 5	V	
	(range II)	V_P	13, 5 to 17 V	
Available output current	I_{QL}	min. 20	mA	
	I_{QH}	max. 50	μA	
D. C. noise margin; range I at V_{Pmin}	M_L	min. 2, 8	V	
	M_H	min. 2, 5	V	
	range II at V_{Pmin}	M_L	min. 2, 8	V
		M_H	min. 4, 5	V
Supply current per gate	range I ; output HIGH	I_{Pav}	typ. 2, 5 mA	
		output LOW	I_{Pav}	typ. 4, 0 mA
	range II; output HIGH	I_{Pav}	typ. 2, 8 mA	
		output LOW	I_{Pav}	typ. 4, 5 mA
Power consumption per gate (50 % duty cycle) at range I ; V_{Pmax}	P_{tot}	max. 71	mW	
	at range II; V_{Pmax}	P_{tot}	max. 98 mW	
Average propagation delay	at $V_{pd1} = 4, 5 V$; ($V_Q = 12 V$)	t_{pd1}	max. 275 ns	
	at $V_{pd2} = 1, 5 V$; ($V_Q = 5 V$)	t_{pd2}	max. 275 ns	
Thermal resistance from system to ambient	R_{th}	max. 150	$^{\circ}C/W$	

CHARACTERISTICS Test conditions: at range I ($V_P = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$.

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{GH}	7,5	-	-	V	11,4 $\left\{ \begin{array}{l} V_{QL} = 0,4\text{ V} \\ I_{QL} = 20\text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	11,4 $\left\{ \begin{array}{l} V_{QH} = 13,5\text{ V} \\ I_{QH} = 40\text{ }\mu\text{A} \end{array} \right.$
Output LOW	V_{QL}	-	-	0,4	V	11,4 $\left\{ \begin{array}{l} V_{GH} = 7,5\text{ V} \\ I_{QL} = 20\text{ mA} \end{array} \right.$
D. C. noise margin: HIGH	M_H	2,5	5,0	-		11,4
	LOW M_L	2,8	5,0	-		11,4
<u>Currents (per gate)</u>						
Input HIGH; $G_2; G_3; G_4; G_5$ $G_1; G_6$	I_{GH}	-	-	1,0	μA	13,5 $\left\{ \begin{array}{l} V_{GH} = 13,5\text{ V} \\ \text{other inputs } 0\text{V} \end{array} \right.$
	I_{GH}	-	-	2,0	μA	
Input LOW; $G_2; G_3; G_4; G_5$ $G_1; G_6$	$-I_{GL}$	-	0,8	1,5	mA	13,5 $\left\{ \begin{array}{l} V_{GL} = 1,7\text{ V} \\ \text{other inputs } 13,5\text{V} \end{array} \right.$
	$-I_{GL}$	-	1,6	3,0	mA	
Output HIGH	I_{QH}	-	-	80	μA	11,4 $\left\{ \begin{array}{l} V_{QH} = 13,5\text{ V} \\ V_{GH} = 4,5\text{ V} \end{array} \right.$
Output LOW	I_{QL}	20	-	-	mA	11,4 $\left\{ \begin{array}{l} V_{QL} = 0,4\text{ V} \\ V_{GH} = 7,5\text{ V} \end{array} \right.$
Supply data						
<u>Currents (per gate)</u>						
at V_{QH}	I_P	-	2,5	4,5	mA	13,5 $\left\{ \begin{array}{l} V_G = 0\text{ V} \\ V_G = 13,5\text{ V} \end{array} \right.$
at V_{QL}	I_P	-	4,0	6,0	mA	13,5
Dynamic data						
<u>Times</u>						
Propagation delay						
fall time: $V_Q = 12\text{ V}$ $V_Q = 5\text{ V}$	t_{pdf1}	80	130	300	ns	$\left\{ \begin{array}{l} T_{amb} = 25\text{ }^\circ\text{C}; C_L = 15\text{ pF} \\ R_L = 760\text{ }\Omega \text{ at } V_Q = 12\text{ V} \\ R_L = 320\text{ }\Omega \text{ at } V_Q = 5\text{ V} \end{array} \right.$
	t_{pdf2}	80	120	300	ns	
rise time: $V_Q = 12\text{ V}$ $V_Q = 5\text{ V}$	t_{pdr1}	80	250	500	ns	
	t_{pdr2}	80	230	500	ns	

¹⁾ All typ. values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

CHARACTERISTICS Test conditions: at range II ($V_P = 15\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.	Conditions and references	
			V_P (V)	
Static data				
Input HIGH	V_{GH}	7,5 - - V	13,5	$\left\{ \begin{array}{l} V_{QL} = 0,4\text{ V} \\ I_{QL} = 20\text{ mA} \end{array} \right.$
Input LOW	V_{GL}	- - 4,5 V	13,5	$\left\{ \begin{array}{l} V_{QH} = 17\text{ V} \\ I_{QH} = 40\text{ }\mu\text{A} \end{array} \right.$
Output LOW	V_{QL}	- - 0,4 V	13,5	$\left\{ \begin{array}{l} V_{GH} = 7,5\text{ V} \\ I_{QL} = 20\text{ mA} \end{array} \right.$
D. C. noise margin: HIGH	M_H	4,5 8,0 - V	13,5	
	LOW M_L	2,8 5,0 - V	13,5	
<u>Currents (per gate)</u>				
Input HIGH: $G_2; G_3; G_4; G_5$ $G_1; G_6$	I_{GH}	- - 1,0 μA	17	$\left\{ \begin{array}{l} V_{GH} = 17\text{ V} \\ \text{other inputs } 0\text{ V} \end{array} \right.$
	I_{GH}	- - 2,0 μA		
Input LOW: $G_2; G_3; G_4; G_5$ $G_1; G_6$	$-I_{GL}$	- 1,0 1,8 mA	17	$\left\{ \begin{array}{l} V_{GL} = 1,7\text{ V} \\ \text{other inputs } 17\text{ V} \end{array} \right.$
	$-I_{GL}$	- 2,0 3,6 mA		
Output HIGH	I_{QH}	- - 80 μA	13,5	$\left\{ \begin{array}{l} V_{QH} = 17\text{ V} \\ V_{GL} = 4,5\text{ V} \end{array} \right.$
Output LOW	I_{QL}	20 - - mA	13,5	$\left\{ \begin{array}{l} V_{QL} = 0,4\text{ V} \\ V_{GL} = 7,5\text{ V} \end{array} \right.$
Supply data				
<u>Currents (per gate)</u>				
at V_{QH}	I_P	- 2,8 4,5 mA	17	$V_G = 0\text{ V}$
at V_{QL}	I_P	- 4,5 7,0 mA	17	$V_G = 17\text{ V}$

¹⁾ All typ. values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 15\text{ V}$.

CHARACTERISTICS (continued)Calculation of collector resistor R_Q

The collector resistor R_Q has to be calculated from voltages and input- and output currents of the gates.

$$R_{Q\max} = \frac{V_P - V_{QH} \quad (V)}{m \cdot I_{QH} + N \cdot I_{GH} \quad (\mu A)}$$

$$R_{Q\min} = \frac{V_P - V_{QL} \quad (V)}{I_{QL\max} - N \cdot I_{GL} \quad (mA)}$$

m = number of interconnected outputs

N = number of used inputs

V_P = supply voltage of TTL-inputs

V_{QH} = output voltage HIGH of TTL-circuit

V_{QL} = output voltage LOW of TTL-circuit

I_{GH} = input current HIGH of TTL-circuit

I_{GL} = input current LOW of TTL-circuit

For interfacing HNIL to TTL:

$$R_{Q\max} = \frac{5 - 2,4 \quad (V)}{m \cdot 80 + N \cdot 80 \quad (\mu A)}$$

$$R_{Q\min} = \frac{5 - 0,4 \quad (V)}{20 - N \cdot 1,6 \quad (mA)}$$

If FZH161/4. LI31 is used as wired-OR combination

for range I: $V_P = 12 V$

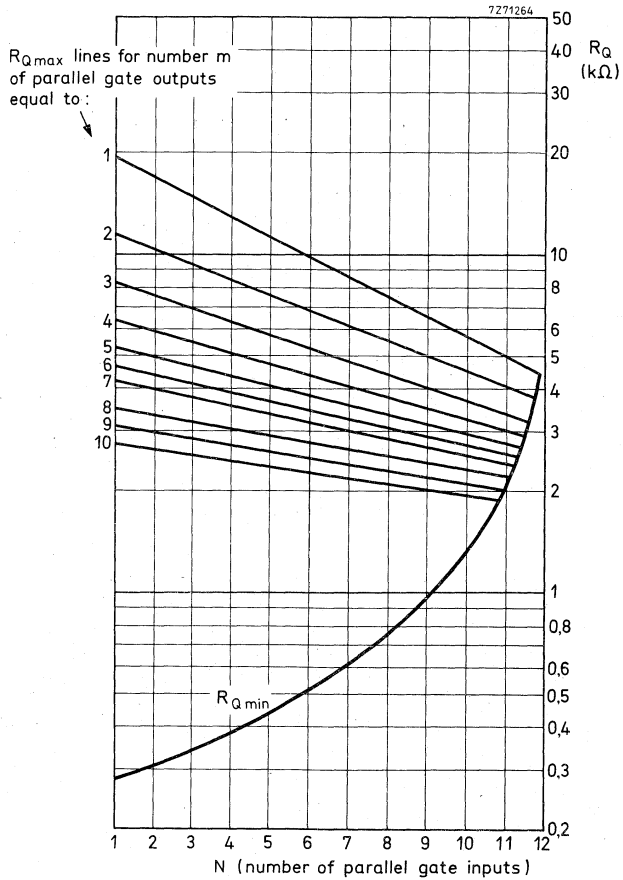
$$R_{Q\max} = \frac{12 - 10 \quad (V)}{m \cdot 80 + N \cdot 1 \quad (\mu A)}$$

$$R_{Q\min} = \frac{12 - 0,4 \quad (V)}{20 - N \cdot 1,5 \quad (mA)}$$

for range II: $V_P = 15 V$

$$R_{Q\max} = \frac{15 - 12 \quad (V)}{m \cdot 80 + N \cdot 1 \quad (\mu A)}$$

$$R_{Q\min} = \frac{15 - 0,4 \quad (V)}{20 - N \cdot 1,8 \quad (mA)}$$

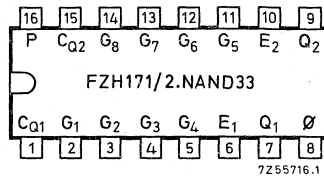
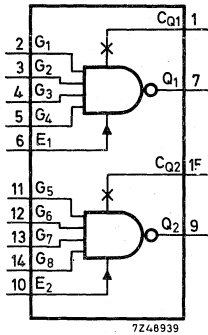


R_Q as a function of m and N loaded with TTL gates.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL 4-INPUT NAND GATE

with slow-down capability and expandable inputs



QUICK REFERENCE DATA

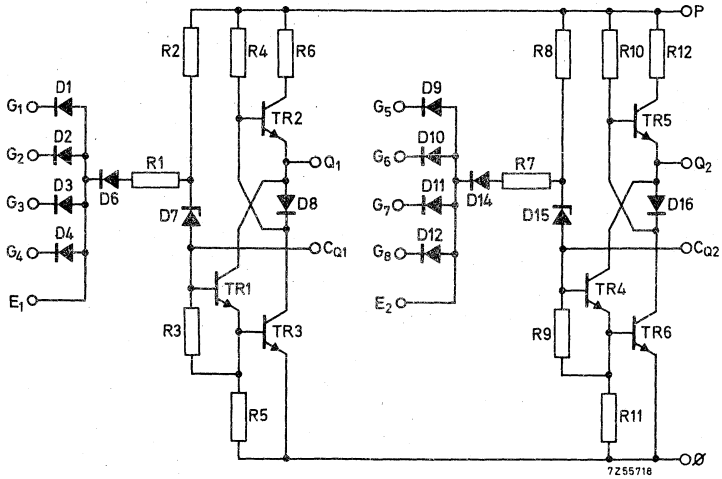
Supply voltage (range I)	V_p	nom.	12 V
(range II)	V_p	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4, 5$ V)	t_{pd}	typ.	170 ns
Available d.c. fan-out $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10
D.C. noise margin at $T_{amb} = 25$ °C			
range I: $V_p = 12$ V	$M_L = M_H$	typ.	5 V
range II: $V_p = 15$ V	M_L	typ.	5 V
	M_H	typ.	8 V
Power consumption per gate at $T_{amb} = 25$ °C			
(50% duty cycle) range I: $V_p = 12$ V	P_{av}	typ.	16 mW
range II: $V_p = 15$ V	P_{av}	typ.	27 mW

The FZH171/2.NAND33 consists of two independent NAND gates and each gate has a special terminal (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.

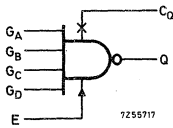
Non-used expander inputs E_1 and E_2 must be left floating.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot E^*}$$

(positive logic)

*) When provided with a diode

G_A	G_B	G_C	G_D	Q
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Output voltage	V_Q	max.	V_P
Input voltage	V_G	max.	18 V
Input current at $V_P = 17$ V	$-I_{GL}$	max.	25 mA
Voltage difference between any two inputs		max.	18 V
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$
Operating ambient temperature	T_{amb}	0 to +70	$^{\circ}C$
Output short-circuit duration	t_{Qsc}	max.	1 s ¹⁾
Slow-down input voltage	$+V_{CQ}$	max.	0,6 V
	$-V_{CQ}$	max.	1,0 V
Slow-down input current	$+I_{CQ}$	max.	2,0 mA
	$-I_{CQ}$	max.	10,0 mA
Expandable input voltage	V_E	min.	0 V
Expandable input current	$-I_E$	max.	25 mA

¹⁾ Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70	$^{\circ}C$
Uniform system supply voltage (range I) (range II)	V_P	11,4 to 13,5	V
	V_P	13,5 to 17	V
Available d. c. fan-out	N_{aL}	max.	10
	N_{aH}	max.	100
D. C. noise margin; range I at V_{Pmin}	M_L	min.	2,8 V
	M_H	min.	2,5 V
range II at V_{Pmin}	M_L	min.	2,8 V
	M_H	min.	4,5 V
Supply current per gate	range I; output HIGH output LOW	I_{Pav}	typ. 0,9 mA
		I_{Pav}	typ. 1,7 mA
	range II; output HIGH output LOW	I_{Pav}	typ. 1,2 mA
		I_{Pav}	typ. 2,3 mA
Power consumption per gate (50% duty cycle) at range I; V_{Pmax}	P_{tot}	max.	31 mW
	P_{tot}	max.	52 mW
at range II; V_{Pmax}			
Thermal resistance from system to ambient	R_{th}	max.	150 $^{\circ}C/W$

CHARACTERISTICS Test conditions: at range I ($V_P = 12 \text{ V}$); $T_{\text{amb}} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references		
					V_P (V)		
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	11,4	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 15 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5	
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ I_{QL} = 15 \text{ mA} \end{array} \right.$
D. C. noise margin: HIGH	M_H	2,5	5,0	-	V	11,4	
	LOW M_L	2,8	5,0	-	V	11,4	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	13,5	$\left\{ \begin{array}{l} V_{GH} = 13,5 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5	$\left\{ \begin{array}{l} V_{GL} = 1,7 \text{ V} \\ \text{other inputs } 13,5 \text{ V} \end{array} \right.$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 10 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	15	-	-	mA	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ V_{QL} = 1,7 \text{ V} \end{array} \right.$
Output short-circuited ²⁾	$-I_{Qsc}$	10	30	50	mA	13,5	$V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
Supply data							
<u>Currents (per gate)</u>							
at V_{QH}	I_P	-	0,9	1,6	mA	13,5	$V_G = 0 \text{ V}$
at V_{QL}	I_P	-	1,7	3,0	mA	13,5	$V_G = 13,5 \text{ V}$
Dynamic data							
<u>Times</u>							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	$\left. \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{\text{amb}} = 25 \text{ }^\circ\text{C} \\ V_{pd} = 4,5 \text{ V} \end{array} \right\}$
rise time	t_{pdr}	90	175	310	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

¹⁾ All typ. values under test conditions: $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ and $V_P = 12 \text{ V}$.

²⁾ Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_P = 15$ V); $T_{amb} = 0$ to $+70$ °C

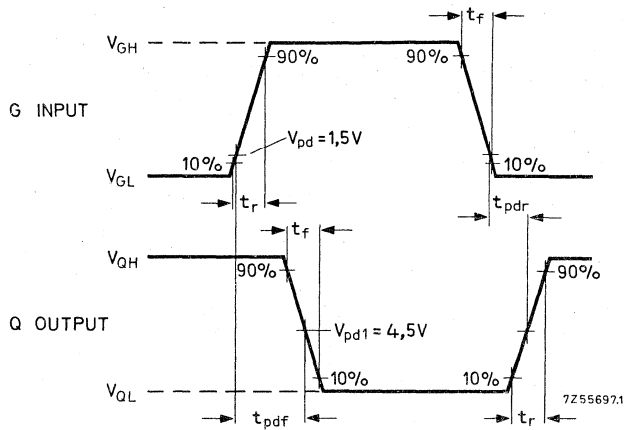
	Sym- bol	min. typ. ¹⁾ max.			Conditions and references		
					V_P (V)		
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	13,5	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	13,5 and 17	
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,0	1,7	V	13,5	
D. C. noise margin: HIGH LOW	M_H	4,5	8,0	-	V	13,5	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
	M_L	2,8	5,0	-	V	13,5	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	17	$\left\{ \begin{array}{l} V_{GH} = 17 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	1,0	1,8	mA	17	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 12 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	18	-	-	mA	13,5	
Output short-circuited ²⁾	$-I_{Qsc}$	15	37	60	mA	17	$V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
Supply data							
<u>Currents (per gate)</u>							
at V_{QH}	I_p	-	1,2	2,1	mA	17	$V_G = 0 \text{ V}$
at V_{QL}	I_p	-	2,3	4,0	mA	17	$V_G = 17 \text{ V}$
Dynamic data							
<u>Times</u>							
<u>Propagation delay</u>							
fall time	t_{pdf}	-	140	-	ns	15	$\left. \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{amb} = 25 \text{ }^\circ\text{C} \\ V_{pd} = 4,5 \text{ V} \end{array} \right\}$
rise time	t_{pdr}	-	195	-	ns	15	
output rise time	t_r	-	410	-	ns	15	
output fall time	t_f	-	75	-	ns	15	

¹⁾ All typical values under test conditions: $T_{amb} = 25$ °C and $V_P = 15$ V.

²⁾ Short-circuit duration max. 1 s.

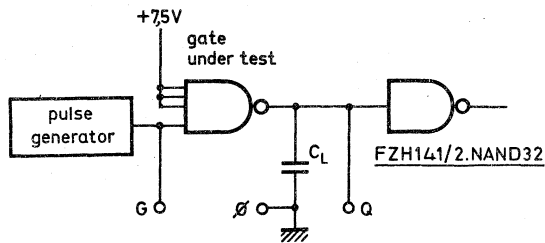
CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): $t_r = 350 \text{ ns}$
 $t_f = 120 \text{ ns}$
 $t_{GH} = 1 \mu\text{s}$

$V_{pd} = +4,5 \text{ V}$



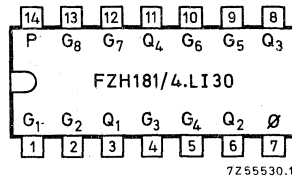
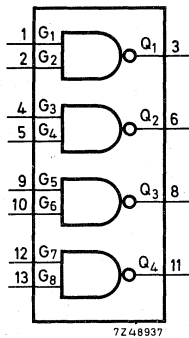
Measuring conditions: $V_p = +12 \text{ V}; +15 \text{ V}$
 $C_L = 10 \text{ pF}$ (including probe and jig capacitance)
 $T_{amb} = 25 \text{ }^\circ\text{C}$
 Slow-down terminals are not connected

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE LOGIC INTERFACE GATE

5 V logic to HNIL



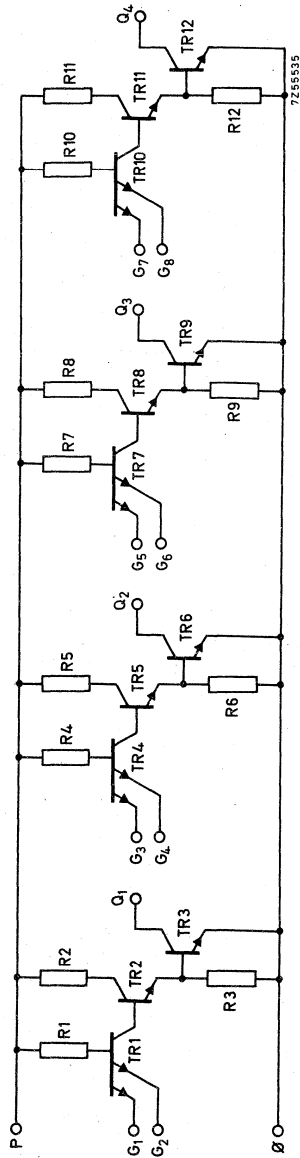
QUICK REFERENCE DATA

Supply voltage	V_P	$5 \pm 5\%$	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Available d. c. fan-out } ($T_{amb} = 0$ to +70 °C) } LOW state	N_{aL}	max.	27
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle)	P_{av}	typ.	24 mW

The FZH181/4. LI30 is a level converter with open-collector outputs for interfacing TTL to HNIL and consists of 4 gates.

PACKAGE OUTLINE 14 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B}$$

(for positive logic)

Function table

G_A	G_B	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	7 V
Output voltage	V_Q	max.	V_P ¹⁾
Input voltage	V_G	max.	5,5 V
Input current ($V_P = 5$ V)	$-I_{GL}$	max.	25 mA
Voltage difference between any two inputs		max.	5,5 V
Storage temperature	T_{stg}		-65 to +150 °C
Operating ambient temperature	T_{amb}		0 to +70 °C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70 °C
Uniform system supply voltage	V_P		4,75 to 5,25 V
Available d. c. fan-out	N_a	max.	27
D. C. noise margin	M	min.	0,4 V
Supply current per gate; output HIGH ($V_P = 5$ V; $V_G = 0$ V)	I_{Pav}	max.	2,0 mA
output LOW ($V_P = 5$ V; $V_G = 5$ V)	I_{Pav}	max.	12,0 mA
Power consumption per gate at V_{Pmax} (50% duty cycle)	P_{tot}	max.	37 mW
Thermal resistance from system to ambient	R_{th}	max.	150 °C/W

¹⁾ For HNIL.

CHARACTERISTICS Test conditions: $V_P = 5\text{ V}$; $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.		Conditions and references			
				V_P (V)			
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	2,0	- -	V	4,75	{ $V_{QL} = 1,0\text{ V}$ $I_{QL} = 50\text{ mA}$	
Input LOW	V_{GL}	-	-	0,8 V	4,75	{ $V_{QH} = 18,0\text{ V}$ $I_{QH} = 250\text{ }\mu\text{A}$	
Output LOW	V_{QL}	-	-	0,4 V	4,75	{ $V_{GH} = 2\text{ V}$ $I_{QL} = 16\text{ mA}$	
	V_{QL}	-	-	1,0 V	4,75	{ $V_{GH} = 2\text{ V}$ $I_{QL} = 50\text{ mA}$	
D.C. noise margin:	M_H	0,4	-	-	V		
	M_L	0,4	-	-	V		
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	40 μA	5,25	$V_{GH} = 2,4\text{ V}$	
Input LOW	$-I_{GL}$	-	-	1,6 mA	5,25	$V_{GL} = 0,4\text{ V}$	
Output HIGH	I_{QH}	-	-	250 μA	4,75	{ $V_{QH} = 18\text{ V}$ $V_{GL} = 0,8\text{ V}$	
Output LOW	I_{QL}	50	-	-	mA	4,75	{ $V_{GH} = 2\text{ V}$ $V_{QL} = 1,0\text{ V}$
<u>Supply data</u>							
<u>Currents (per gate)</u>							
at V_{QH}	I_P	-	1,0	2,0 mA	5	$V_{GL} = 0\text{ V}$	
at V_{QL}	I_P	-	8,5	12,0 mA	5	$V_{GH} = 5\text{ V}$	
<u>Dynamic data</u>							
<u>Times</u>							
<u>Propagation</u>							
fall time	t_{pdf}	-	20	60 ns	12	{ $V_Q = 12\text{ V}$; $R_L = 390\text{ }\Omega$	
rise time	t_{Pdr}	-	130	300 ns	12	{ $V_Q = 12\text{ V}$; $R_L = 3,9\text{ k}\Omega$	

¹⁾ All typ. values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

CHARACTERISTICS (continued)Calculation of collector resistor R_Q

The collector resistor R_Q has to be calculated from voltages and input - and output currents of the gates.

$$R_{Q\max} = \frac{V_P - V_{QH} \quad (V)}{m \cdot I_{QH} + N \cdot I_{GH} \quad (\mu A)} \quad R_{Q\min} = \frac{V_P - V_{QL} \quad (V)}{I_{QL\max} - N \cdot I_{GL} \quad (mA)}$$

- m = number of interconnected outputs
 N = number of used inputs
 V_P = supply voltage of HNIL inputs
 V_{QH} = output voltage HIGH of HNIL-circuit
 V_{QL} = output voltage LOW of HNIL-circuit
 I_{GH} = input current HIGH of HNIL-circuit
 I_{GL} = input current LOW of HNIL-circuit

For interfacing TTL to HNIL (range I; $V_P = 12 V$)

$$R_{Q\max} = \frac{12 - 10 \quad (V)}{m \cdot 250 + N \cdot 1 \quad (\mu A)} \quad R_{Q\min} = \frac{12 - 1,0 \quad (V)}{50 - N \cdot 1,5 \quad (mA)}$$

For interfacing TTL to HNIL (range II; $V_P = 15 V$)

$$R_{Q\max} = \frac{15 - 12 \quad (V)}{m \cdot 250 - N \cdot 1 \quad (\mu A)} \quad R_{Q\min} = \frac{15 - 1,0 \quad (V)}{50 - N \cdot 1,8 \quad (mA)}$$

If FZH181/4. LI30 is used as wired-OR combination

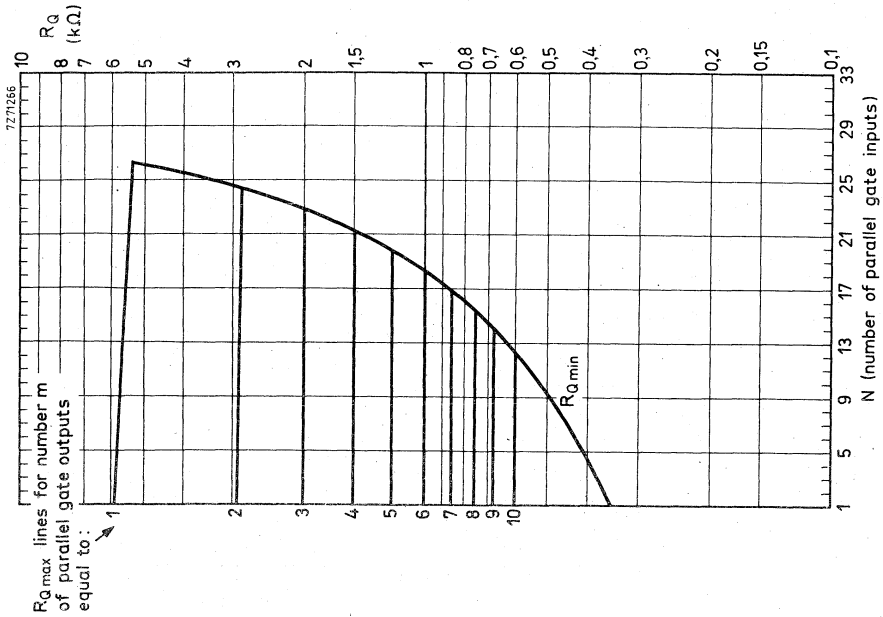
HIGH state

LOW state

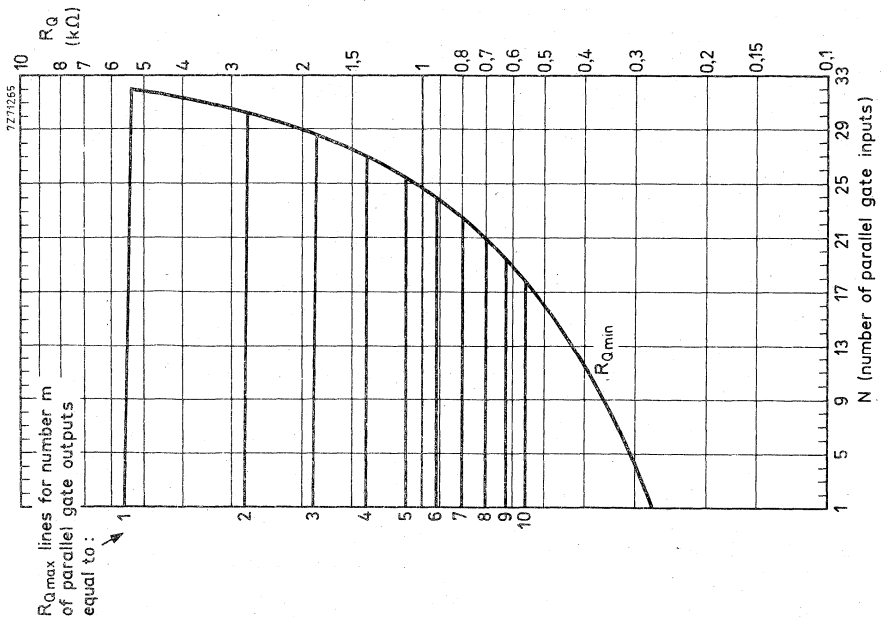
$$R_{Q\max} = \frac{V_P - 2,4 \quad (V)}{m \cdot 250 - N \cdot 40 \quad (\mu A)} \quad R_{Q\min} = \frac{V_P - 0,4 \quad (V)}{16 - N \cdot 1,6 \quad (mA)}$$

of which m = number of FZH181/4. LI30 OR combinations

N = number of used inputs



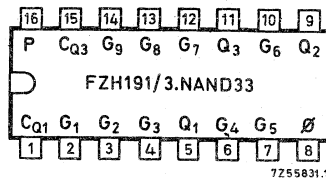
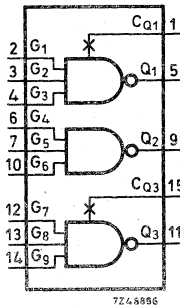
R_Q as a function of m and N at $V_p = 15$ V (range II).



R_Q as a function of m and N at $V_p = 12$ V (range I).

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

TRIPLE 3-INPUT NAND GATE with slow-down capability



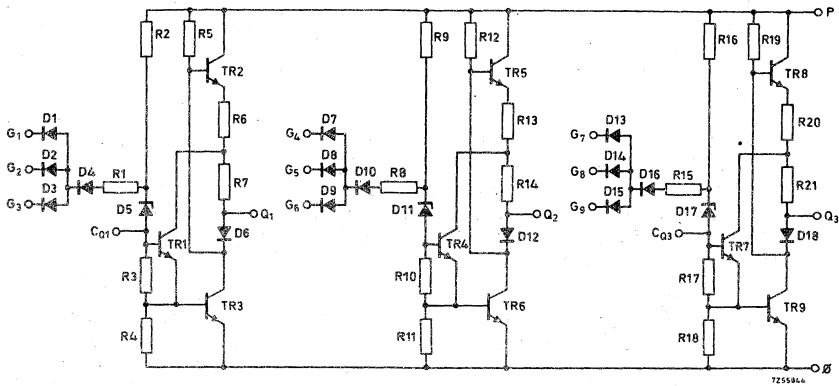
QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12 V
(range II)	V_P	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	170 ns
Available d.c. fan-out } $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10
D.C. noise margin at $T_{amb} = 25$ °C			
range I: $V_P = 12$ V	$M_L = M_H$	typ.	5 V
range II: $V_P = 15$ V	M_L	typ.	5 V
	M_H	typ.	8 V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I: $V_P = 12$ V	P_{av}	typ.	16 mW
range II: $V_P = 15$ V	P_{av}	typ.	27 mW

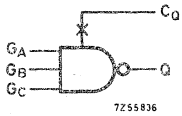
The FZH191/3.NAND33 consists of a number of independent NAND gates at which two NAND gates have a special terminal (C_Q). It is possible to connect a capacitor between the output (Q) and the corresponding slow-down terminal (C_Q) to increase the propagation delay.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B \cdot G_C}$$

(positive logic)

Function table

G_A	G_B	G_C	Q
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at $V_P = 17$ V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		-65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s ¹⁾
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V
(range II)	V_P		13,5 to 17	V
Available d. c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D. C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{Pmin}	M_L	min.	2,8	V
	M_H	min.	4,5	V
Supply current at range I ; output HIGH	I_{Pav}	typ.	0,9	mA
output LOW	I_{Pav}	typ.	1,7	mA
at range II ; output HIGH	I_{Pav}	typ.	1,2	mA
output LOW	I_{Pav}	typ.	2,3	mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	31	mW
at range II ; V_{Pmax}	P_{tot}	max.	52	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

¹⁾ Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I ($V_P = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.		Conditions and references			
				V_P (V)			
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	11,4	$\left\{ \begin{array}{l} V_{QL} \leq 1,7\text{ V} \\ I_{QL} = 15\text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5	$\left\{ \begin{array}{l} V_{QH} \geq 10\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{array} \right.$
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5\text{ V} \\ I_{QL} = 15\text{ mA} \end{array} \right.$
D.C. noise margin: HIGH	M_H	2,5	5,0	-	V	11,4	
LOW	M_L	2,8	5,0	-	V	11,4	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	13,5	$\left\{ \begin{array}{l} V_{GH} = 13,5\text{ V} \\ \text{other inputs } 0\text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5	$\left\{ \begin{array}{l} V_{GL} = 1,7\text{ V} \\ \text{other inputs } 13,5\text{ V} \end{array} \right.$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5\text{ V} \\ V_{QH} = 10\text{ V} \end{array} \right.$
Output LOW	I_{QL}	15	-	-	mA	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5\text{ V} \\ V_{QL} = 1,7\text{ V} \end{array} \right.$
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0\text{ V}; V_Q = 0\text{ V}$
Supply data							
<u>Currents (per gate)</u>							
at V_{QH}	I_P	-	0,9	1,6	mA	13,5	$V_G = 0\text{ V}$
at V_{QL}	I_P	-	1,7	3,0	mA	13,5	$V_G = 13,5\text{ V}$
Dynamic data							
<u>Times</u>							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	$\left. \begin{array}{l} C_L = 10\text{ pF}; N = 1 \\ T_{amb} = 25\text{ }^\circ\text{C} \\ V_{pd} = 4,5\text{ V} \end{array} \right\}$
rise time	t_{pdr}	90	175	310	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

¹⁾ All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

²⁾ Short-circuited duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_p = 15 \text{ V}$); $T_{\text{amb}} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

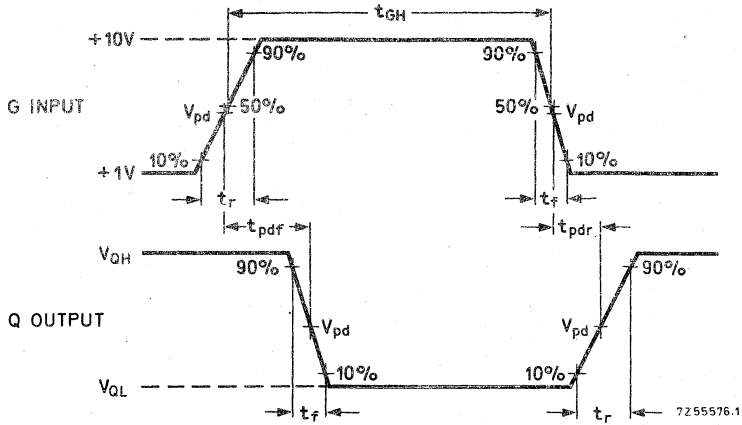
	Sym- bol	min. typ. ¹⁾ max.		Conditions and references			
				V_p (V)			
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	13,5	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	13,5 and 17	$\left\{ \begin{array}{l} V_{QH} \geq 12 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,0	1,7	V	13,5	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
D.C. noise margin: HIGH	M_H	4,5	8,0	-	V	13,5	
LOW	M_L	2,8	5,0	-	V	13,5	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	17	$\left\{ \begin{array}{l} V_{GH} = 17 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	1,0	1,8	mA	17	$\left\{ \begin{array}{l} V_{GL} = 1,7 \text{ V} \\ \text{other inputs } 17 \text{ V} \end{array} \right.$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 12 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	18	-	-	mA	13,5	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ V_{QL} = 1,7 \text{ V} \end{array} \right.$
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	17	$V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
Supply data							
<u>Currents (per gate)</u>							
at V_{QH}	I_p	-	1,2	2,1	mA	17	$V_G = 0 \text{ V}$
at V_{QL}	I_p	-	2,3	4,0	mA	17	$V_G = 17 \text{ V}$
Dynamic data							
<u>Times</u>							
Propagation delay							
fall time	t_{pdf}	-	140	-	ns	15	$\left\{ \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{\text{amb}} = 25 \text{ }^\circ\text{C} \\ V_{dp} = 4,5 \text{ V} \end{array} \right.$
rise time	t_{pdr}	-	195	-	ns	15	
output rise time	t_r	-	410	-	ns	15	
output fall time	t_f	-	75	-	ns	15	

¹⁾ All typical values under test conditions: $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ and $V_p = 15 \text{ V}$.

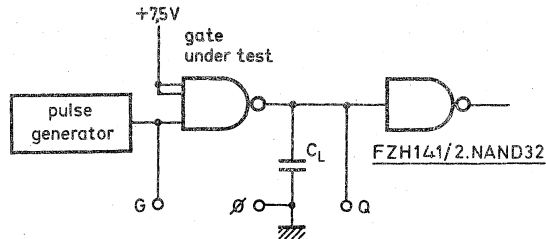
²⁾ Short-circuited duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): $t_r = 350 \text{ ns}$ $V_{pd} = +4,5 \text{ V}$
 $t_f = 120 \text{ ns}$
 $t_{GH} = 1 \mu\text{s}$

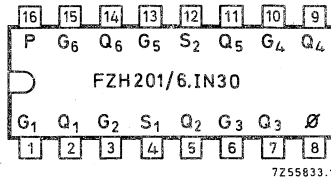
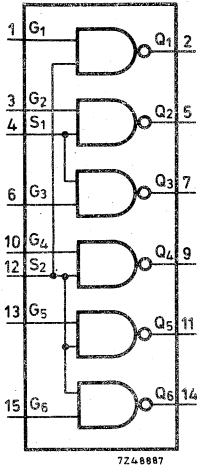


Measuring conditions: $V_p = +12 \text{ V}; +15 \text{ V}$
 $C_L = 10 \text{ pF}$ (including probe and jig capacitance)
 $T_{amb} = 25 \text{ }^\circ\text{C}$
 Slow-down terminals are not connected

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdr}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SEXTUPLE INVERTER WITH STROBE INPUT

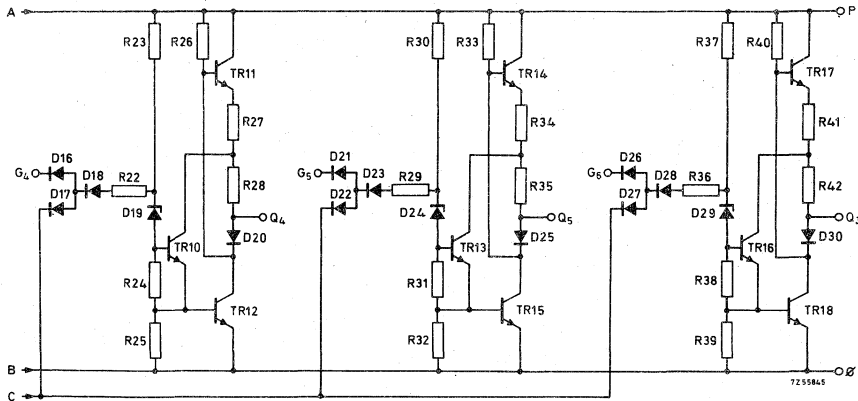
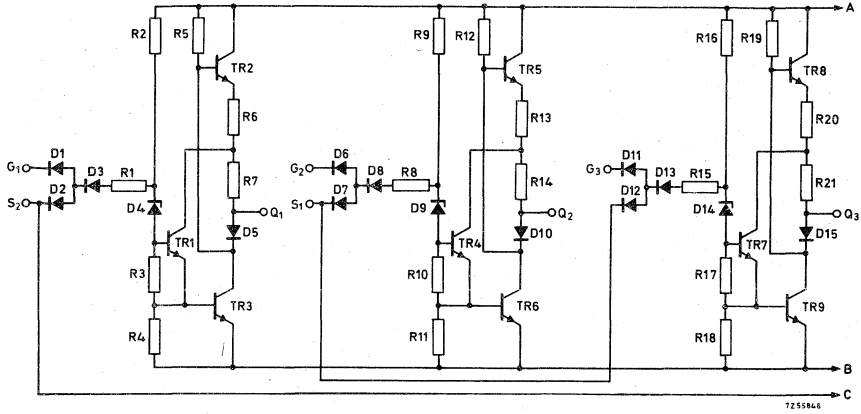


QUICK REFERENCE DATA			
Supply voltage (range I)	V_P	nom.	12 V
(range II)	V_P	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay time ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4, 5$ V)	t_{pd}	typ.	170 ns
Available d. c. fan-out } $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10
D. C. noise margin at $T_{amb} = 25$ °C			
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5 V
range II: $V_P = 15$ V		typ.	5 V
		typ.	8 V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	16 mW
range II: $V_P = 15$ V	P_{av}	typ.	27 mW

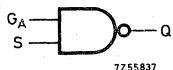
The FZH201/6.IN30 consists of a number of independent inverters without slow-down capability, but with a common strobe input.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A \cdot S} \text{ (positive logic)}$$

Function table

G_A	S	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at $V_P = 17$ V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}	-65 to +150		°C
Operating ambient temperature	T_{amb}	0 to +70		°C
Output short-circuit duration	t_{Qsc}	max.	1	s ¹⁾

¹⁾ Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70	$^{\circ}C$
Uniform system supply voltage (range I) (range II)	V_P	11,4 to 13,5	V
	V_P	13,5 to 17	V
Available d.c. fan-out	N_{aL}	max.	10
	N_{aH}	max.	100
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8 V
	M_H	min.	2,5 V
range II at V_{Pmin}	M_L	min.	2,8 V
	M_H	min.	4,5 V
Supply current per gate	range I ; output HIGH	I_{Pav}	typ. 0,9 mA
		I_{Pav}	typ. 1,7 mA
	range II; output HIGH	I_{Pav}	typ. 1,2 mA
		I_{Pav}	typ. 2,3 mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max.	31 mW
	P_{tot}	max.	52 mW
at range II; V_{Pmax}			
Thermal resistance from system to ambient	R_{th}	max.	150 $^{\circ}C/W$

CHARACTERISTICS Test conditions: at range I ($V_p = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references		
					V_p (V)		
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	11,4	$\begin{cases} V_{QL} \leq 1,7\text{ V} \\ I_{QL} = 15\text{ mA} \end{cases}$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5	$\begin{cases} V_{QH} \geq 10\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{cases}$
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	$\begin{cases} V_{GL} = 4,5\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{cases}$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	$\begin{cases} V_{GH} = 7,5\text{ V} \\ I_{QL} = 15\text{ mA} \end{cases}$
D.C. noise margin: HIGH LOW	M_H	2,5	5,0	-	V	11,4	
	M_L	2,8	5,0	-	V	11,4	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	13,5	$\begin{cases} V_{GH} = 13,5\text{ V} \\ \text{other inputs } 0\text{ V} \end{cases}$
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5	$\begin{cases} V_{GL} = 1,7\text{ V} \\ \text{other inputs } 13,5\text{ V} \end{cases}$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	$\begin{cases} V_{GL} = 4,5\text{ V} \\ V_{QH} = 10\text{ V} \end{cases}$
Output LOW	I_{QL}	15	-	-	mA	11,4	$\begin{cases} V_{GH} = 7,5\text{ V} \\ V_{QL} = 1,7\text{ V} \end{cases}$
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0\text{ V}; V_Q = 0\text{ V}$
Supply data							
<u>Currents (per gate)</u>							
at V_{QH}	I_p	-	0,9	1,6	mA	13,5	$V_G = 0\text{ V}$
at V_{QL}	I_p	-	1,7	3,0	mA	13,5	$V_G = 13,5\text{ V}$
Dynamic data							
<u>Times</u>							
Propagation delay:							
fall time	t_{pdf}	90	175	310	ns	12	$\begin{cases} C_L = 10\text{ pF}; N = 1 \\ T_{amb} = 25\text{ }^\circ\text{C} \\ V_{pd} = 4,5\text{ V} \end{cases}$
rise time	t_{pdr}	90	175	310	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

¹⁾ All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_p = 12\text{ V}$.

²⁾ Short-circuited duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_P = 15 \text{ V}$); $T_{amb} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

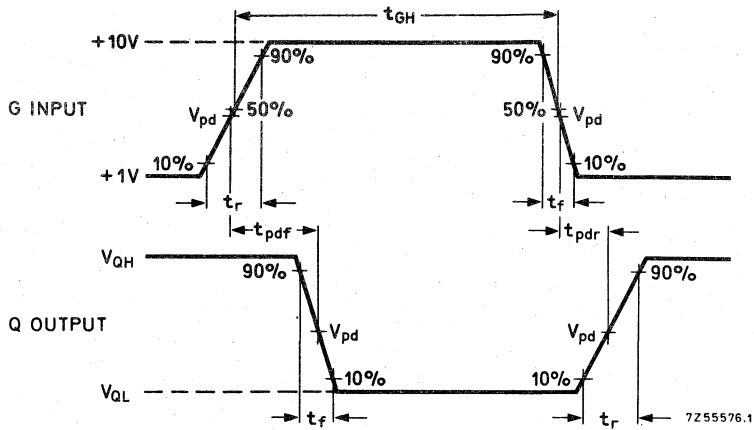
	Sym- bol	min. typ. ¹⁾ max.		Conditions and references			
				V_P (V)			
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	13,5	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	13,5 and 17	
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,0	1,7	V	13,5	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
D.C. noise margin: HIGH	M_H	4,5	8,0	-	V	13,5	
LOW	M_L	2,8	5,0	-	V	13,5	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	17	$\left\{ \begin{array}{l} V_{GH} = 17 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	1,0	1,8	mA	17	$\left\{ \begin{array}{l} V_{GL} = 1,7 \text{ V} \\ \text{other inputs } 17 \text{ V} \end{array} \right.$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 12 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	18	-	-	mA	13,5	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ V_{QL} = 1,7 \text{ V} \end{array} \right.$
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	17	$V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
Dynamic data							
<u>Currents (per gate)</u>							
at V_{QH}	I_P	-	1,2	2,1	mA	17	$V_G = 0 \text{ V}$
at V_{QL}	I_P	-	2,3	4,0	mA	17	$V_G = 17 \text{ V}$
Supply data							
<u>Times</u>							
Propagation delay:							
fall time	t_{pdf}	-	140	-	ns	15	$\left\{ \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{amb} = 25 \text{ }^\circ\text{C} \\ V_{pd} = 4,5 \text{ V} \end{array} \right.$
rise time	t_{pdr}	-	195	-	ns	15	
output rise time	t_r	-	410	-	ns	15	
output fall time	t_f	-	75	-	ns	15	

1) All typical values under test conditions: $T_{amb} = 25 \text{ }^\circ\text{C}$ and $V_P = 15 \text{ V}$.

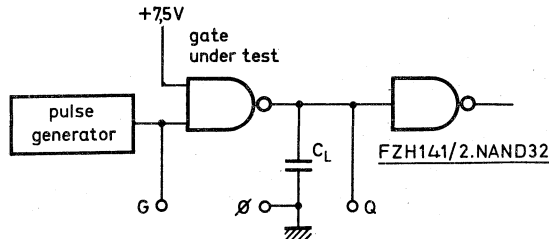
2) Short-circuited duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): $t_r = 350 \text{ ns}$ $V_{pD} = +4,5 \text{ V}$
 $t_f = 120 \text{ ns}$
 $t_{GH} = 1 \mu\text{s}$



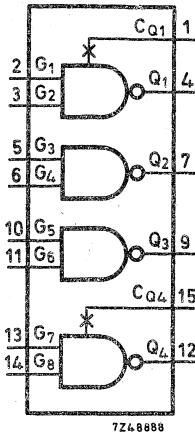
Measuring conditions: $V_p = +12 \text{ V}; +15 \text{ V}$
 $C_L = 10 \text{ pF}$ (including probe and jig capacitance)
 $T_{amb} = 25^\circ\text{C}$

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

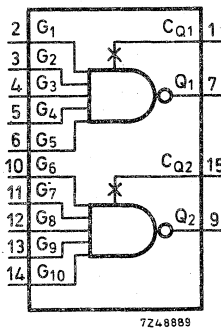
The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE 2-INPUT NAND GATE DUAL 5-INPUT NAND GATE

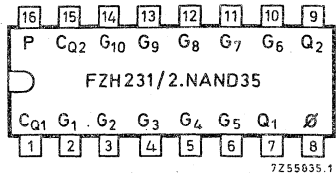
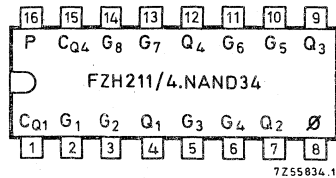
both having slow-down capability and open collector



FZH211/4.NAND34



FZH231/2.NAND35



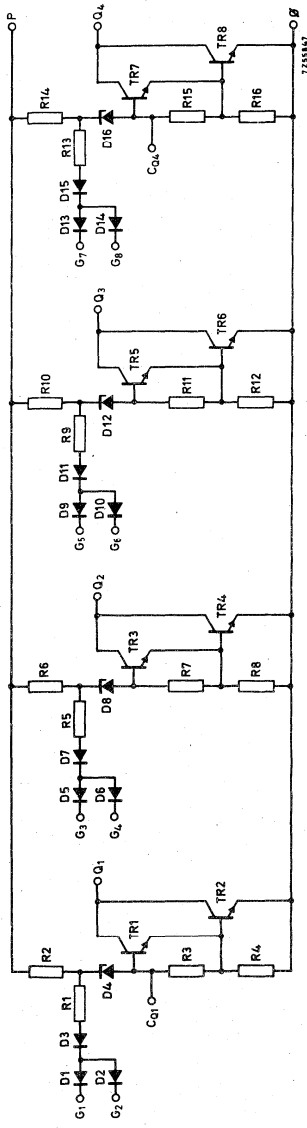
QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12 V
(range II)	V_P	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Available d.c. fan-out	N_{aL}	max.	10
$T_{amb} = 0 \text{ to } +70 \text{ °C}$			
D.C. noise margin at $T_{amb} = 25 \text{ °C}$			
range I: $V_P = 12 \text{ V}$	$M_L = M_H$	typ.	5 V
range II: $V_P = 15 \text{ V}$	M_L	typ.	5 V
	M_H	typ.	8 V
Power consumption per gate at $T_{amb} = 25 \text{ °C}$			
(50% duty cycle) range I: $V_P = 12 \text{ V}$	P_{av}	typ.	8,5 mW
range II: $V_P = 15 \text{ V}$	P_{av}	typ.	15 mW

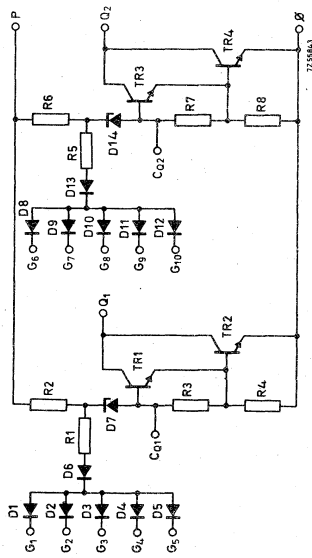
The FZH211/4.NAND34 and FZH231/2.NAND35 consist of a number of independent NAND gates with open collector and two gates of each circuit have a slow-down terminal. It is possible to connect a capacitor between the output Q and the corresponding slow-down terminal C_Q to increase the propagation delay.

The outputs of these gates may be interconnected to perform the AND-OR-NOT function.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).



CIRCUIT DIAGRAMS
FZH211/4.NAND34



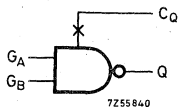
FZH231/2.NAND35

LOGIC FUNCTION

FUNCTION TABLES

1. Individual gate operation

FZH211/4.NAND34

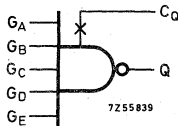


$$Q = \overline{G_A \cdot G_B}$$

(positive logic)

G _A	G _B	Q
L	X	H
X	L	H
H	H	L

FZH231/2.NAND35

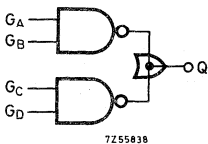


$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot G_E}$$

(positive logic)

G _A	G _B	G _C	G _D	G _E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
H	H	H	H	H	L

2. Wired-OR combination



$$Q = \overline{(G_A \cdot G_B) \cdot (G_C \cdot G_D)} = \overline{(G_A \cdot G_B) + (G_C \cdot G_D)}$$

(positive logic)

G _A	G _B	G _C	G _D	Q
L	X	L	X	H
L	X	X	L	H
X	L	X	L	H
X	L	L	X	H
H	H	X	X	L
X	X	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		-65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Input current at $V_P = 17$ V	$-I_{GL}$	max.	25	mA
Slow-down input voltage	$\left\{ \begin{array}{l} +V_{CQ} \\ -V_{CQ} \end{array} \right.$	max.	0,6	V
		max.	1,0	V
Slow-down input current	$\left\{ \begin{array}{l} +I_{CQ} \\ -I_{CQ} \end{array} \right.$	max.	2,0	mA
		max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C	
Uniform system supply voltage (range I)	V_P		11,4 to 13,5	V	
	(range II)	V_P	13,5 to 17	V	
Available d.c. fan-out	N_{aL}	max.	10		
D.C. noise margin; range I at V_{Pmin}	M_L	min.	2,8	V	
	M_H	min.	2,5	V	
	range II at V_{Pmin}	M_L	min.	2,8	V
		M_H	min.	4,5	V
Supply current per gate	range I; output HIGH	I_{Pav}	max.	2,1	mA
		output LOW	I_{Pav}	max.	1,2
	range II; output HIGH	I_{Pav}	max.	2,1	mA
		output LOW	I_{Pav}	max.	1,4
Power consumption per gate (50% duty cycle) at range I; V_{Pmax}	P_{tot}	max.	18	mW	
	at range II; V_{Pmax}	P_{tot}	max.	30	mW
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W	

CHARACTERISTICS Test conditions: at range I ($V_P = 12 \text{ V}$); $T_{\text{amb}} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.		Conditions and references			
				V_P (V)			
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	11,4	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 15 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5	
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ I_{QL} = 15 \text{ mA} \end{array} \right.$
D. C. noise margin: HIGH	M_H	2,5	5,0	-	V	11,4	
LOW	M_L	2,8	5,0	-	V	11,4	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	13,5	$\left\{ \begin{array}{l} V_{GH} = 13,5 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5	
Output HIGH	I_{QH}	-	-	80	μA	11,4	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 18 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	15	-	-	mA	11,4	
<u>Supply data</u>							
<u>Currents (per gate)</u>							
at V_{QH}	I_P	-	1,0	1,7	mA	13,5	$V_G = 0 \text{ V}$
at V_{QL}	I_P	-	0,4	1,0	mA	13,5	$V_G = 13,5 \text{ V}$

¹⁾ All typ. values under test conditions: $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ and $V_P = 12 \text{ V}$.

CHARACTERISTICS Test conditions: at range II ($V_P = 15\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references	
					V _P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V _{GH}	7,5	-	-	V	13,5 { V _{QL} ≤ 1,7 V I _{QL} = 18 mA
Input LOW	V _{GL}	-	-	4,5	V	13,5 and 17 { V _{QH} ≥ 12 V -I _{QH} = 0,1 mA
Output LOW	V _{QL}	-	1,0	1,7	V	13,5 { V _{GH} = 7,5 V I _{QL} = 18 mA
D. C. noise margin: HIGH	M _H	4,5	8,0	-	V	13,5
	LOW	M _L	2,8	5,0	-	
<u>Currents (per gate)</u>						
Input HIGH	I _{GH}	-	-	1,0	μA	17 { V _{GH} = 17 V other inputs 0 V
Input LOW	-I _{GL}	-	1,0	1,8	mA	17 { V _{GL} = 1,7 V other inputs 17 V
Output HIGH	I _{QH}	-	-	80	μA	13,5 { V _{GL} = 4,5 V V _{QH} = 18 V
Output LOW	I _{QL}	18	-	-	mA	13,5 { V _{GH} = 7,5 V V _{QL} = 1,7 V
Supply data						
<u>Currents (per gate)</u>						
at V _{QH}	I _P	-	1,3	2,1	mA	17 V _G = 0 V
at V _{QL}	I _P	-	0,7	1,4	mA	17 V _G = 17 V

¹⁾ All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 15\text{ V}$.

CHARACTERISTICS (continued)

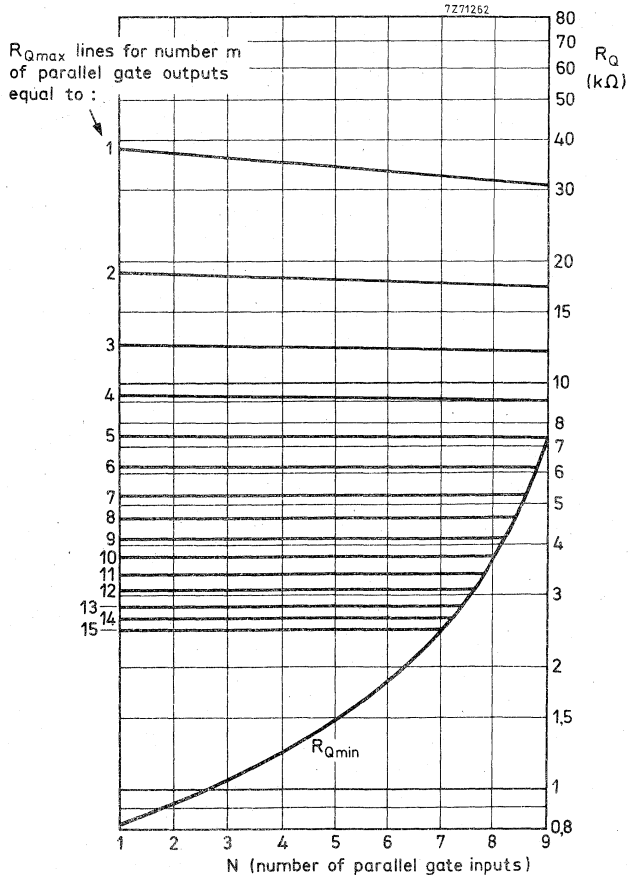
Calculation of collector resistor R_Q

The collector resistor R_Q has to be calculated from voltages and input- and output currents of the gates.

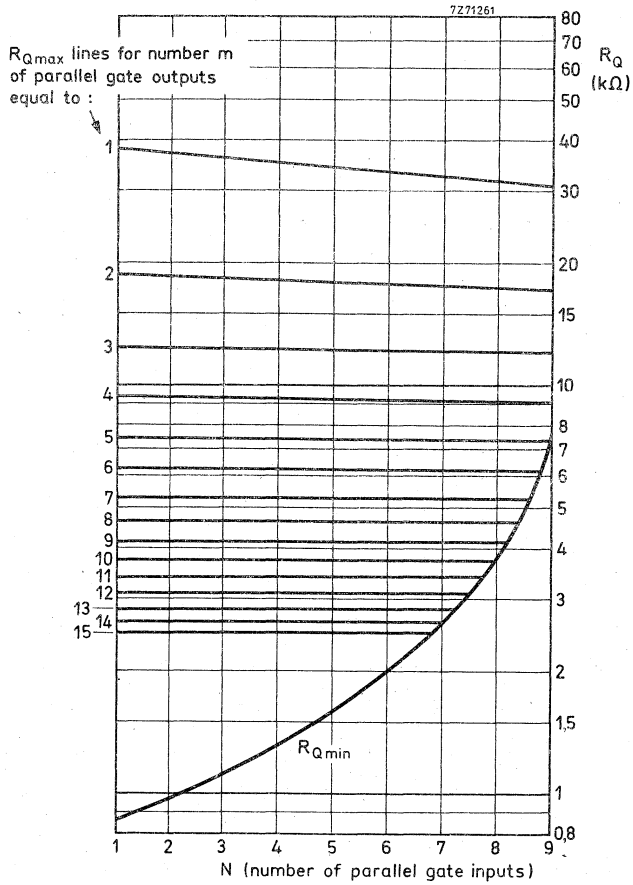
$$R_{Qmax} = \frac{V_P - V_{QH} \text{ (V)}}{m \cdot I_{QH} + N \cdot I_{GH} \text{ (\mu A)}}$$

$$R_{Qmin} = \frac{V_P - V_{QL} \text{ (V)}}{I_{QLmax} - N \cdot I_{GL} \text{ (mA)}}$$

- m = number of interconnected outputs
- N = number of used inputs
- V_P = supply voltage of HNIL inputs
- V_{QH} = output voltage HIGH of HNIL - circuit
- V_{QL} = output voltage LOW of HNIL - circuit



R_Q as a function of m and N at $V_P = 12 \text{ V}$ (range I).

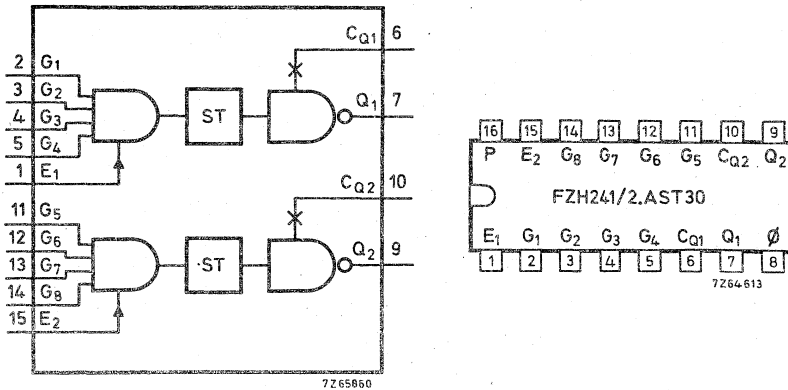


R_Q as a function of m and N at $V_P = 15$ V (range II).

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL 4-INPUT NAND SCHMITT TRIGGER

with slow-down capability and expandable inputs



QUICK REFERENCE DATA

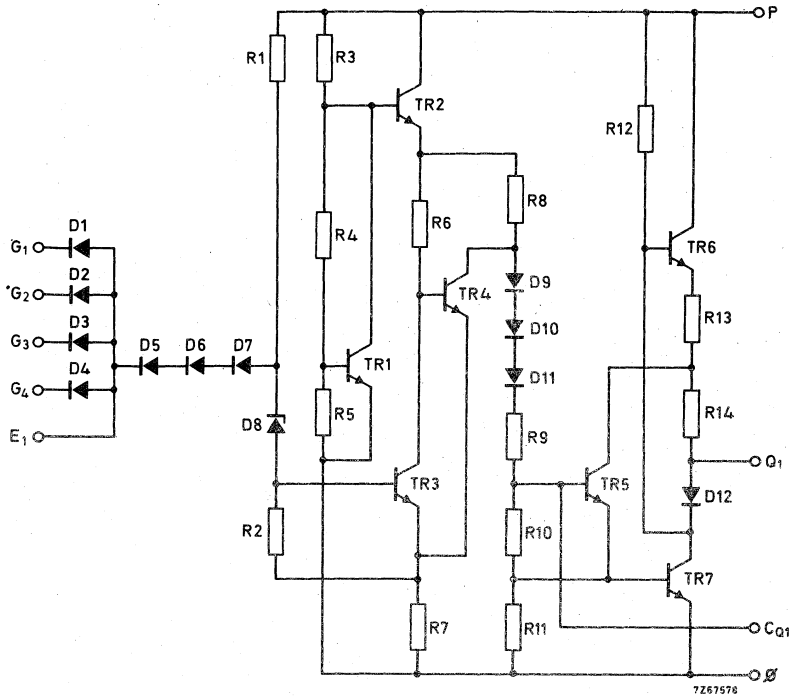
Supply voltage (range I)	V_P	nom.	12	V	
(range II)	V_P	nom.	15	V	
Operating ambient temperature	T_{amb}		0 to +70	°C	
Available d. c. fan-out $T_{amb} = 0 \text{ to } +70 \text{ } ^\circ\text{C}$	} LOW state	N_{aL}	max.	10	
D. C. noise margin at $T_{amb} = 25 \text{ } ^\circ\text{C}$					
range I : $V_P = 12 \text{ V}$	$M_L = M_H$	typ.	5	V	
range II : $V_P = 15 \text{ V}$	{	M_L	typ.	5	V
		M_H	typ.	8	V
Power consumption per gate at $T_{amb} = 25 \text{ } ^\circ\text{C}$					
(50% duty cycle) range I : $V_P = 12 \text{ V}$	P_{av}	typ.	48	mW	
range II : $V_P = 15 \text{ V}$	P_{av}	typ.	72	mW	

The FZH241/2.AST30 consists of two identical 4-input NAND SCHMITT triggers with slow-down capability and expandable inputs.

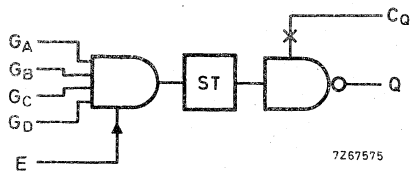
Each circuit functions as a 4-input NANDgate (without using the expandable input), but because of the SCHMITT action, the gate has different input threshold levels for positive- and negative-going signals. The hysteresis, which is the difference between the two threshold levels, is typically 900 mV.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



FUNCTION TABLE

G_A	G_B	G_C	G_D	E	Q
L	X	X	X	X	H
X	L	X	X	X	H
X	X	L	X	X	H
X	X	X	L	X	H
X	X	X	X	L	H
X	X	X	X	H	L

$$Q = \overline{G_A \cdot G_B \cdot G_C \cdot G_D \cdot E}$$

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at $V_P = 17$ V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		-65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s. ¹⁾
Slow-down input voltage	$\left\{ \begin{array}{l} +V_{CQ} \\ -V_{CQ} \end{array} \right.$	max.	0,6	V
		max.	1,0	V
Slow-down input current	$\left\{ \begin{array}{l} +I_{CQ} \\ -I_{CQ} \end{array} \right.$	max.	2,0	mA
		max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C	
Uniform system supply voltage (range I) (range II)	V_P		11,4 to 13,5	V	
	V_P		13,5 to 17	V	
Available d.c. fan-out; LOW state HIGH state	$\left\{ \begin{array}{l} N_{aL} \\ N_{aH} \end{array} \right.$	max.	10		
		max.	100		
D.C. noise margin; range I at V_{Pmin} range II at V_{Pmin}	$\left\{ \begin{array}{l} M_L \\ M_H \end{array} \right.$	min.	2,8	V	
		min.	2,5	V	
	$\left\{ \begin{array}{l} M_L \\ M_H \end{array} \right.$	min.	2,8	V	
		min.	4,5	V	
Supply current per gate	$\left\{ \begin{array}{l} \text{range I: output HIGH} \\ \text{output LOW} \end{array} \right.$	I_{Pav}	typ.	4,0	mA
		I_{Pav}	typ.	3,8	mA
	$\left\{ \begin{array}{l} \text{range II: output HIGH} \\ \text{output LOW} \end{array} \right.$	I_{Pav}	typ.	4,5	mA
		I_{Pav}	typ.	5,0	mA
Power consumption per gate (50% duty cycle) at range I; V_{Pmax} at range II; V_{Pmax}	P_{tot}	max.	85	mW	
	P_{tot}	max.	105	mW	
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W	

¹⁾ Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I ($V_P = 12\text{ V}$); $T_{\text{amb}} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references		
					V_P (V)		
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	8,0	-	-	V	11,4	$\left\{ \begin{array}{l} V_{QL} \leq 1,7\text{ V} \\ I_{QL} = 15\text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	5,0	V	11,4 and 13,5	$\left\{ \begin{array}{l} V_{QH} \geq 10\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{array} \right.$
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,0	1,7	V	11,4	$\left\{ \begin{array}{l} V_{GH} = 8,0\text{ V} \\ I_{QL} = 15\text{ mA} \end{array} \right.$
Positive-going threshold voltage	V_{TP}	-	7,1	-	V	12	
Negative-going threshold voltage	V_{TN}	-	6,2	-	V	12	
Hysteresis ²⁾	V_H	-	0,9	-	V	12	
D.C. noise margin: HIGH	M_H	2,5	5,0	-	V	11,4	
LOW	M_L	2,8	5,0	-	V	11,4	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	13,5	$\left\{ \begin{array}{l} V_{GH} = 13,5\text{ V} \\ \text{other inputs } 0\text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	-	1,5	mA	13,5	$\left\{ \begin{array}{l} V_{GL} = 1,7\text{ V} \\ \text{other inputs } 13,5\text{ V} \end{array} \right.$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 5,0\text{ V} \\ V_{QH} = 10\text{ V} \end{array} \right.$
Output LOW	I_{QL}	15	-	-	mA	11,4	$\left\{ \begin{array}{l} V_{GH} = 8,0\text{ V} \\ V_{QL} = 1,7\text{ V} \end{array} \right.$
Output short-circuited ³⁾	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0\text{ V}; V_Q = 0\text{ V}$
<u>Supply data</u>							
<u>Currents (per gate)</u>							
at V_{QH}	I_P	-	4,0	6,3	mA	13,5	$V_G = 0\text{ V}$
at V_{QL}	I_P	-	3,8	6,0	mA	13,5	$V_G = 13,5\text{ V}$

¹⁾ All typical values under test conditions: $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

²⁾ $V_H = V_{TP} - V_{TN}$.

³⁾ Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_P = 15$ V); $T_{amb} = 0$ to $+70$ °C

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references		
					V_P (V)		
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	8,0	-	-	V	13,5	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	5,0	V	13,5 and 17	$\left\{ \begin{array}{l} V_{QH} \geq 12 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,1	1,7	V	13,5	$\left\{ \begin{array}{l} V_{GH} = 8,0 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
Positive-going threshold voltage	V_{TP}	-	7,05	-	V	15	
Negative-going threshold voltage	V_{TN}	-	6,15	-	V	15	
Hysteresis ²⁾	V_H	-	0,9	-	V	15	
D.C. noise margin: HIGH	M_H	4,5	8,0	-	V	13,5	
LOW	M_L	2,8	5,0	-	V	13,5	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	17	$\left\{ \begin{array}{l} V_{GH} = 17 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	-	1,8	mA	17	$\left\{ \begin{array}{l} V_{GL} = 1,7 \text{ V} \\ \text{other inputs } 17 \text{ V} \end{array} \right.$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 5,0 \text{ V} \\ V_{QH} = 12 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	18	-	-	mA	13,5	$\left\{ \begin{array}{l} V_{GH} = 8,0 \text{ V} \\ V_{QL} = 1,7 \text{ V} \end{array} \right.$
Output short-circuited ³⁾	$-I_{Qsc}$	9	15	25	mA	17	$\left\{ \begin{array}{l} V_G = 0 \text{ V}; V_Q = 0 \text{ V} \end{array} \right.$
<u>Supply data</u>							
<u>Currents (per gate)</u>							
at V_{QH}	I_P	-	4,5	7,3	mA	17	$V_G = 0 \text{ V}$
at V_{QL}	I_P	-	5,0	8,0	mA	17	$V_G = 17 \text{ V}$

¹⁾ All typical values under test conditions: $T_{amb} = 25$ °C and $V_P = 15$ V.

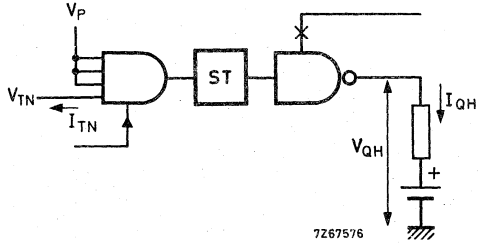
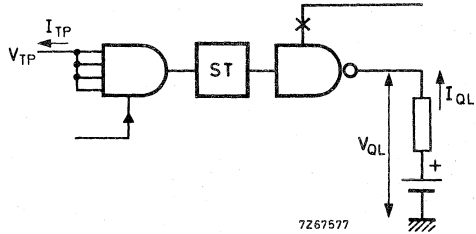
²⁾ $V_H = V_{TP} - V_{TN}$.

³⁾ Short-circuit duration max. 1 s.

CHARACTERISTICS

D.C. test circuit for V_{TP} , V_{TN} and V_H

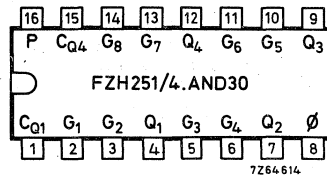
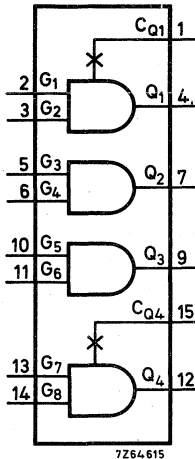
conditions: $V_P = 12\text{ V}$ (range I); ϕ to earth;
 $V_P = 15\text{ V}$ (range II); $T_{amb} = 25\text{ }^\circ\text{C}$



The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE 2-INPUT AND GATE

with slow-down capability



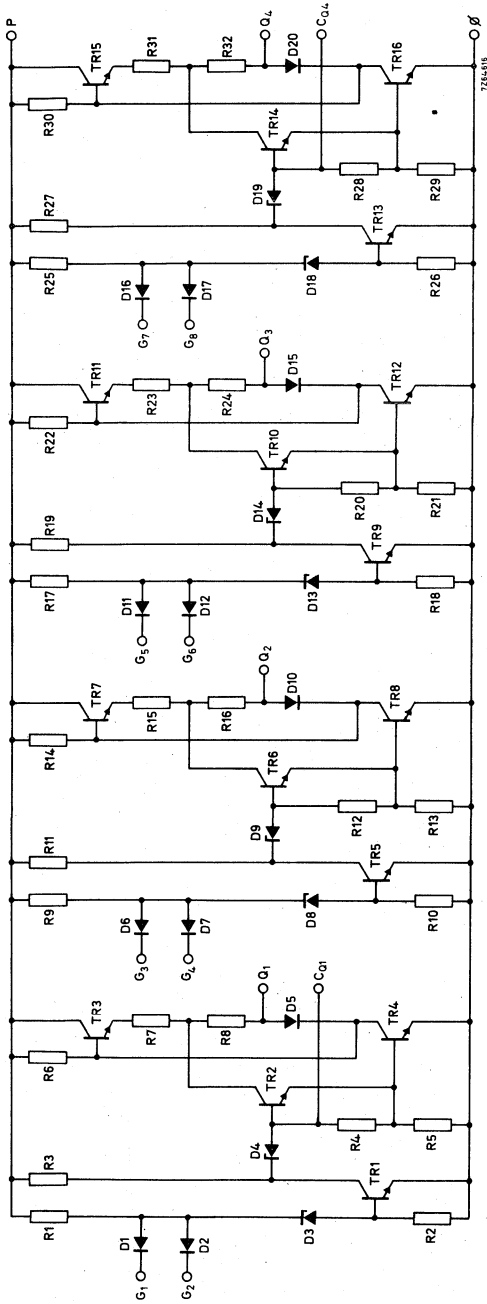
QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12 V
(range II)	V_P	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay N = 1; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V	t_{pd}	typ.	260 ns
Available d. c. fan-out $T_{amb} = 0$ to +70 °C	} LOW state	N_{aL}	max. 10
D. C. noise margin at $T_{amb} = 25$ °C			
range I: $V_P = 12$ V	} $M_L = M_H$	$M_L = M_H$	typ. 5 V
range II: $V_P = 15$ V		M_L	typ. 5 V
		M_H	typ. 8 V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I: $V_P = 12$ V	P_{av}	typ.	24 mW
range II: $V_P = 15$ V	P_{av}	typ.	42,8 mW

The FZH251/4.AND30 consists of four 2-input AND gates, two of which may be slowed down.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTIONS

Function table

GA	GB	Q
L	X	L
X	L	L
H	H	H



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$Q = G_A \cdot G_B$ (positive logic)

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at $V_P = 17$ V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		-65 to +150	$^{\circ}C$
Operating ambient temperature	T_{amb}		0 to +70	$^{\circ}C$
Output short-circuit duration	t_{Qsc}	max.	1	s ¹⁾
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	$^{\circ}C$	
Uniform system supply voltage (range I) (range II)	V_P		11,4 to 13,5	V	
	V_P		13,5 to 17	V	
Available d. c. fan-out	N_{aL}	max.	10		
	N_{aH}	max.	100		
D. C. noise margin; range I at V_{Pmin} range II at V_{Pmin}	M_L	min.	2,8	V	
	M_H	min.	2,5	V	
	M_L	min.	2,8	V	
	M_H	min.	4,5	V	
Supply current per gate	range I; output HIGH output LOW	I_{Pav}	typ.	1,6	mA
		I_{Pav}	typ.	2,4	mA
	range II; output HIGH output LOW	I_{Pav}	typ.	2,2	mA
		I_{Pav}	typ.	3,5	mA
Power consumption per gate (50% duty cycle) at range I; V_{Pmax} at range II; V_{Pmax}	P_{tot}	max.	51,5	mW	
	P_{tot}	max.	84	mW	
Thermal resistance from system to ambient	R_{th}	max.	150	$^{\circ}C/W$	

1) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I ($V_P = 12$ V); $T_{amb} = 0$ to $+70$ °C

	Sym- bol	min. typ. 1) max.		Conditions and references			
				V_P (V)			
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	11,4	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 15 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5	
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	
D. C. noise margin: HIGH	M_H	2,5	5,0	-	V	11,4	
	LOW M_L	2,8	5,0	-	V	11,4	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	13,5	$\left\{ \begin{array}{l} V_{GH} = 13,5 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 10 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	15	-	-	mA	11,4	
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
Supply data							
<u>Currents (per gate)</u>							
at V_{QL}	I_P	-	3	4,5	mA	13,5	$V_G = 0 \text{ V}$
Dynamic data							
<u>Times</u>							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	$\left. \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{amb} = 25 \text{ }^\circ\text{C} \\ V_{pd} = 4,5 \text{ V} \end{array} \right\}$
rise time	t_{pdr}	200	340	570	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_P = 12$ V.

2) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_p = 15$ V); $T_{amb} = 0$ to $+70$ °C

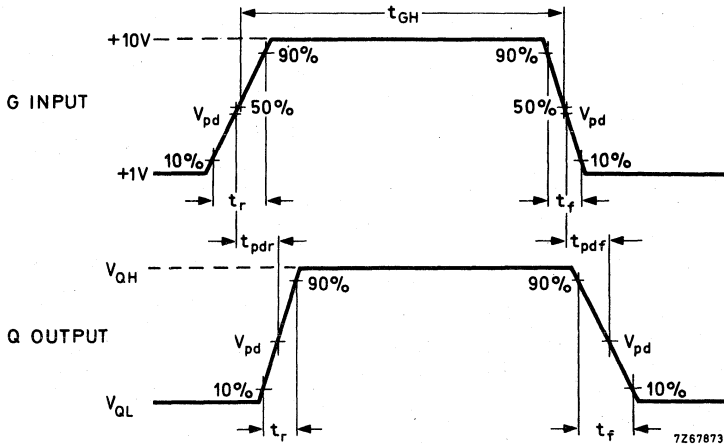
	Sym- bol	min. typ. ¹⁾ max.		Conditions and references			
				V_p (V)			
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	13,5	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	13,5 and 17	
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,0	1,7	V	13,5	
D. C. noise margin: HIGH LOW	M_H	4,5	8,0	-	V	13,5	
	M_L	2,8	5,0	-	V	13,5	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	17	$\left\{ \begin{array}{l} V_{GH} = 17 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	1,0	1,8	mA	17	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 12 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	18	-	-	mA	13,5	
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	17	
Supply data							
<u>Currents (per gate)</u>							
at V_{QL}	I_p	-	3,7	6	mA	17	$V_G = 0 \text{ V}$
Dynamic data							
<u>Times</u>							
Propagation delay fall time	t_{pdf}	-	t. b. f.	-	ns	15	$\left. \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{amb} = 25 \text{ }^\circ\text{C} \\ V_{pd} = 4,5 \text{ V} \end{array} \right\}$
	rise time	t_{pdr}	-	t. b. f.	-	ns	
output rise time	t_r	-	t. b. f.	-	ns	15	
	output all time	t_f	-	t. b. f.	-	ns	

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_p = 15$ V.

2) Short-circuit duration max. 1 s.

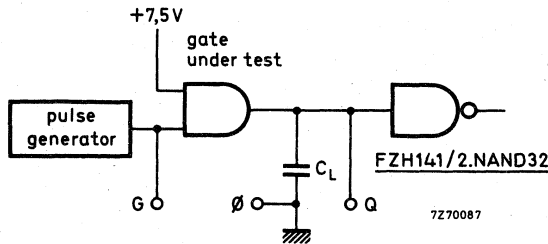
CHARACTERISTICS

Dynamic data



Pulse generator (G-input): $t_r = 350$ ns
 $t_f = 120$ ns
 $t_{GH} = 1 \mu s$

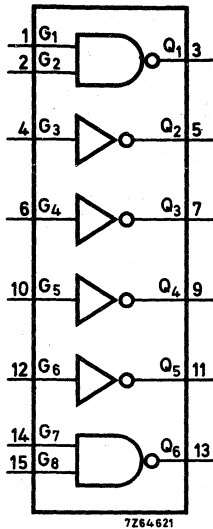
$V_{pd} = +4, 5$ V



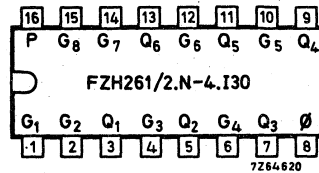
Measuring conditions: $V_p = +12$ V; +15 V
 $C_L = 10$ pF (including probe and jig capacitance)
 $T_{amb} = 25$ °C

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.



DUAL NAND GATE/ QUADRUPLE INVERTER



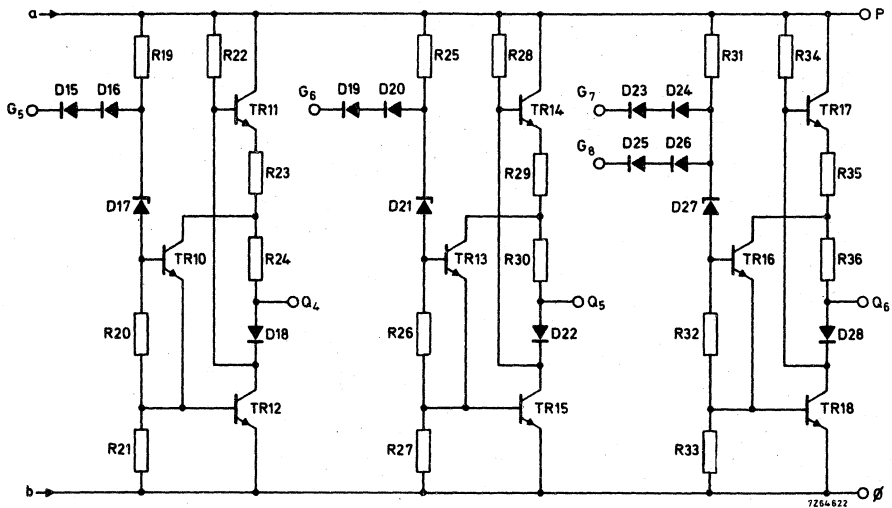
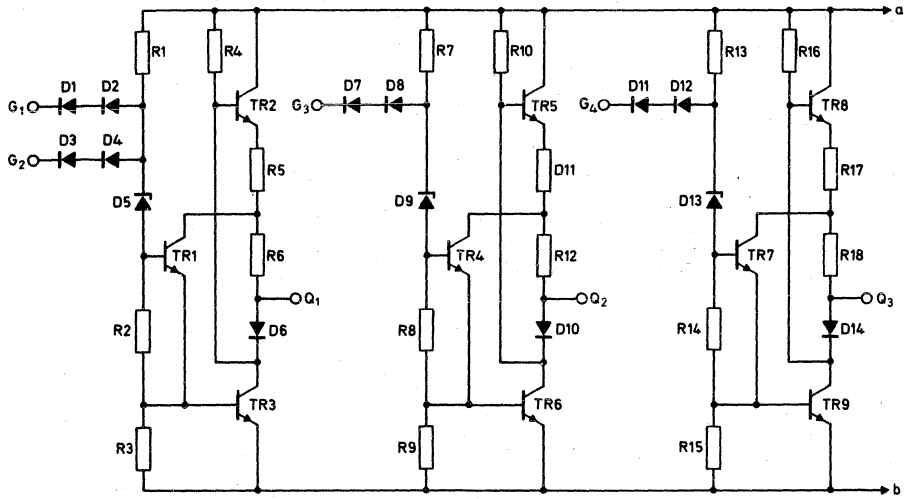
QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12 V	
(range II)	V_P	nom.	15 V	
Operating ambient temperature	T_{amb}		0 to +70 °C	
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4, 5$ V)	t_{pd}	typ.	175 ns	
Available d. c. fan-out $T_{amb} = 0$ to +70 °C	} LOW state N_{aL}	max.	10	
D. C. noise margin at $T_{amb} = 25$ °C				
range I: $V_P = 12$ V	} $M_L = M_H$	typ.	5 V	
range II: $V_P = 15$ V		M_L	typ.	5 V
		M_H	typ.	8 V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I: $V_P = 12$ V	P_{av}	typ.	16,2 mW	
range II: $V_P = 15$ V	P_{av}	typ.	28,5 mW	

The FZH261/2.N-4.I30 consists of two 2-input NAND gates and four inverters, none of which have the slow-down facility.

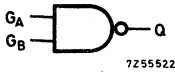
PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM

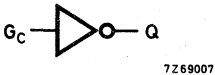


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LOGIC FUNCTION



$$Q = \overline{G_A \cdot G_B} \text{ (positive logic)}$$



$$Q = \overline{G_C} \text{ (positive logic)}$$

Function table

G _A	G _B	Q
L	X	H
X	L	H
H	H	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V _P	max.	18 V
Output voltage	V _Q	max.	V _P
Input voltage	V _G	max.	18 V
Input current at V _P = 17 V	-I _{GL}	max.	25 mA
Voltage difference between any two inputs		max.	18 V
Storage temperature	T _{stg}		-65 to +150 °C
Operating ambient temperature	T _{amb}		0 to +70 °C
Output short-circuit duration	t _{Qsc}	max.	1 s ¹⁾

¹⁾ Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	°C
Uniform system supply voltage (range I) (range II)	V_p		11,4 to 13,5	V
	V_p		13,5 to 17	V
Available d. c. fan-out	N_{aL}	max.	10	
	N_{aH}	max.	100	
D. C. noise margin; range I at V_{pmin}	M_L	min.	2,8	V
	M_H	min.	2,5	V
range II at V_{pmin}	M_L	min	2,8	V
	M_H	min	4,5	V
Supply current per gate	range I; output HIGH output LOW	I_{pav}	typ.	1,0 mA
		I_{pav}	typ.	1,7 mA
	range II; output HIGH output LOW	I_{pav}	typ.	1,4 mA
		I_{pav}	typ.	2,4 mA
Power consumption per gate (50% duty cycle) at range I ; V_{pmax}	P_{tot}	max.	34,3	mW
		at range II; V_{pmax}	max.	56
Thermal resistance from system to ambient	R_{th}	max.	150	°C/W

CHARACTERISTICS Test conditions: at range I ($V_p = 12$ V); $T_{amb} = 0$ to $+70$ °C

	Sym- bol	min. typ. 1) max.			Conditions and references		
					V_p (V)		
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	11,4	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 15 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5	
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ I_{QL} = 15 \text{ mA} \end{array} \right.$
D. C. noise margin: HIGH	M_H	2,5	5,0	-	V	11,4	
LOW	M_L	2,8	5,0	-	V	11,4	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	13,5	$\left\{ \begin{array}{l} V_{GH} = 13,5 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5	$\left\{ \begin{array}{l} V_{GL} = 1,7 \text{ V} \\ \text{other inputs } 13,5 \text{ V} \end{array} \right.$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 10 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	15	-	-	mA	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ V_{QL} = 1,7 \text{ V} \end{array} \right.$
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
Supply data							
<u>Currents (per gate)</u>							
at V_{QL}	I_p	-	1,7	3	mA	13,5	$V_G = 13,5 \text{ V}$
Dynamic data							
<u>Times</u>							
Propagation delay							$\left. \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{amb} = 25 \text{ }^\circ\text{C} \\ V_{pd} = 4,5 \text{ V} \end{array} \right\}$
fall time	t_{pdf}	90	175	310	ns	12	
rise time	t_{pdr}	90	175	310	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_p = 12$ V.

2) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_p = 15\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

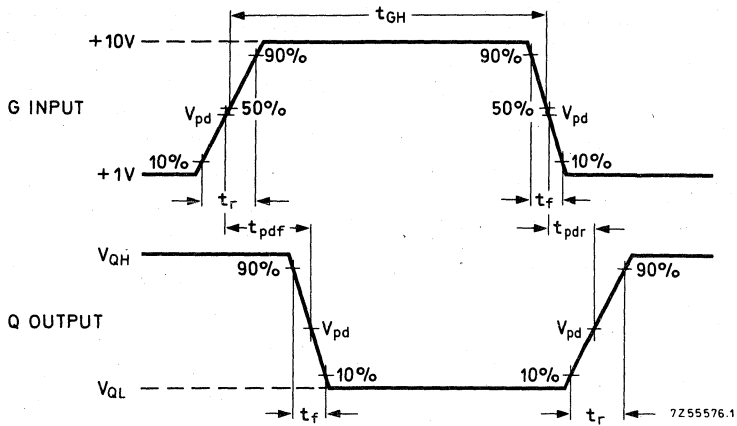
	Sym- bol	min. typ. 1) max.			Conditions and references	
					V_p (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{GH}	7,5	-	-	V	13,5 { $V_{QL} \leq 1,7\text{ V}$ $I_{QL} = 18\text{ mA}$
Input LOW	V_{GL}	-	-	4,5	V	13,5 and 17 { $V_{QH} \geq 12\text{ V}$ $-I_{QH} = 0,1\text{ mA}$
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 and 17 { $V_{GL} = 4,5\text{ V}$ $-I_{QH} = 0,1\text{ mA}$
Output LOW	V_{QL}	-	1,0	1,7	V	13,5 { $V_{GH} = 7,5\text{ V}$ $I_{QL} = 18\text{ mA}$
D.C. noise margin: HIGH LOW	M_H	4,5	8,0	-	V	13,5
	M_L	2,8	5,0	-	V	
<u>Currents (per gate)</u>						
Input HIGH	I_{GH}	-	-	1,0	μA	17 { $V_{GH} = 17\text{ V}$ other inputs 0 V
Input LOW	$-I_{GL}$	-	1,0	1,8	mA	17 { $V_{GL} = 1,7\text{ V}$ other inputs 17 V
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17 { $V_{GL} = 4,5\text{ V}$ $V_{QH} = 12\text{ V}$
Output LOW	I_{QL}	18	-	-	mA	13,5 { $V_{GH} = 7,5\text{ V}$ $V_{QL} = 1,7\text{ V}$
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	17 $V_G = 0\text{ V}; V_Q = 0\text{ V}$
Supply data						
<u>Currents (per gate)</u>						
at V_{QL}	I_p	-	2,4	4	mA	17 $V_G = 17\text{ V}$
Dynamic data						
<u>Times</u>						
Propagation delay fall time	t_{pdf}	-	t.b.f.	-	ns	15 } $C_L = 10\text{ pF}; N = 1$ $T_{amb} = 25\text{ }^\circ\text{C}$ $V_{pd} = 4,5\text{ V}$
	rise time	t_{pdr}	-	t.b.f.	-	
output rise time	t_r	-	t.b.f.	-	ns	
	output fall time	t_f	-	t.b.f.	-	

1) All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_p = 15\text{ V}$.

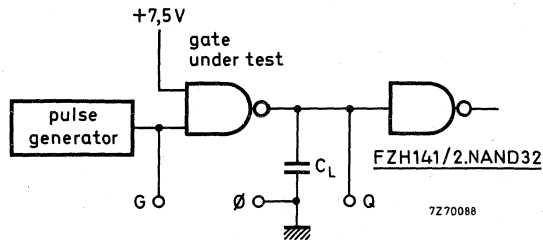
2) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): $t_r = 350 \text{ ns}$ $V_{pd} = +4,5 \text{ V}$
 $t_f = 120 \text{ ns}$
 $t_{GH} = 1 \mu\text{s}$



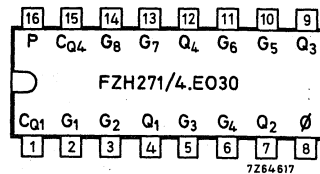
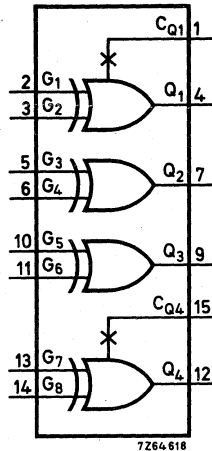
Measuring conditions: $V_p = +12 \text{ V}; +15 \text{ V}$
 $C_L = 10 \text{ pF}$ (including probe and jig capacitance)
 $T_{amb} = 25 \text{ }^\circ\text{C}$

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE EXCLUSIVE-OR GATE

with slow-down capability



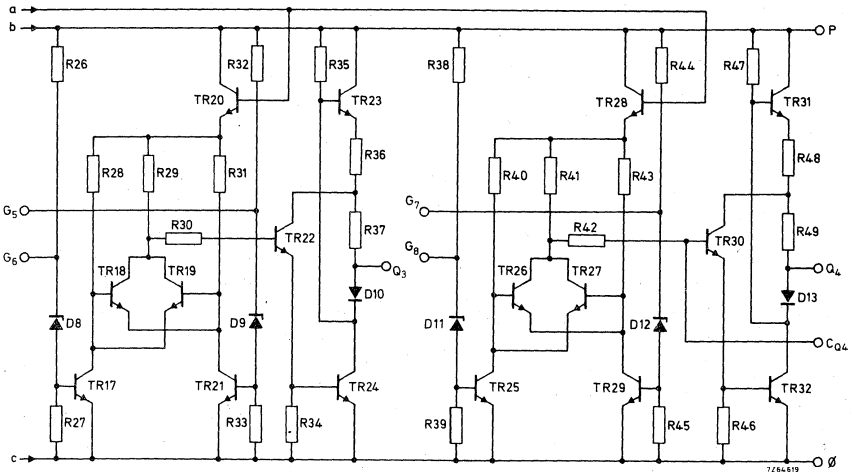
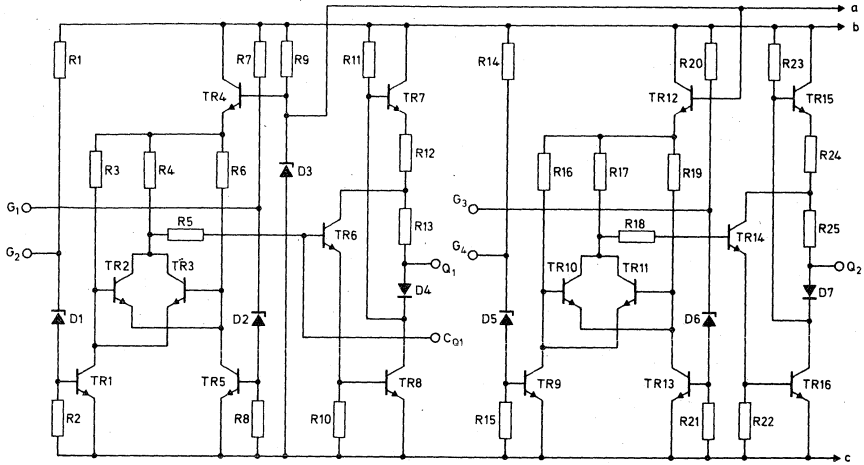
QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12 V
(range II)	V_P	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay			
$N = 1; C_L = 10 \text{ pF}; T_{amb} = 25 \text{ °C}; V_{pd} = 4, 5 \text{ V}$	t_{pd}	typ.	260 ns
Available d. c. fan-out			
$T_{amb} = 0 \text{ to } +70 \text{ °C}$	} LOW state	N_{aL}	max. 10
D. C. noise margin at $T_{amb} = 25 \text{ °C}$			
range I : $V_P = 12 \text{ V}$	} $M_L = M_H$	M_L	typ. 5 V
range II : $V_P = 15 \text{ V}$		M_L	typ. 5 V
		M_H	typ. 8 V
Power consumption per gate at $T_{amb} = 25 \text{ °C}$			
(50% duty cycle) range I : $V_P = 12 \text{ V}$	P_{av}	typ.	43,5 mW
range II : $V_P = 15 \text{ V}$	P_{av}	typ.	66,8 mW

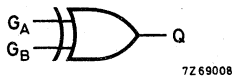
The FZH271/4.EO30 consists of four 2-input EXCLUSIVE-OR gates, two of which may be slowed down.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = G_A \cdot \bar{G}_B + \bar{G}_A \cdot G_B \text{ (positive logic)}$$

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

Function table

G_A	G_B	Q
L	L	L
H	L	H
L	H	H
H	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Input current at $V_P = 17$ V	$-I_{GL}$	max.	25	mA
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		-65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Output short-circuit duration	t_{Qsc}	max.	1	s ¹⁾
Slow-down input voltage	$+V_{CQ}$	max.	0,6	V
	$-V_{CQ}$	max.	1,0	V
Slow-down input current	$+I_{CQ}$	max.	2,0	mA
	$-I_{CQ}$	max.	10,0	mA

¹⁾ Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature		T_{amb}	0 to +70 °C
Uniform system supply voltage (range I)		V_P	11,4 to 13,5 V
	(range II)	V_P	13,5 to 17 V
Available d. c. fan-out		N_{aL}	max. 10
		N_{aH}	max. 100
D. C. noise margin; range I at V_{Pmin}		M_L	min. 2,8 V
		M_H	min. 2,5 V
range II at V_{Pmin}		M_L	min. 2,8 V
		M_H	min. 4,5 V
Supply current per gate	range I ; output HIGH	I_{Pav}	typ. 3,45 mA
		I_{Pav}	typ. 3,8 mA
	range II; output HIGH	I_{Pav}	typ. 4,1 mA
		I_{Pav}	typ. 4,8 mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}		P_{tot}	max. 76,8 mW
	at range II; V_{Pmax}	P_{tot}	max. 114,8 mW
Thermal resistance from system to ambient		R_{th}	max. 150 °C/W

CHARACTERISTICS Test conditions: at range I ($V_p = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. 1) max.			Conditions and references		
					V_p (V)		
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	11,4	$\left\{ \begin{array}{l} V_{QL} \leq 1,7\text{ V} \\ I_{QL} = 15\text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5	
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5\text{ V} \\ I_{QL} = 15\text{ mA} \end{array} \right.$
D.C. noise margin: HIGH LOW	M_H	2,5	5,0	-	V	11,4	
	M_L	2,8	5,0	-	V	11,4	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	13,5	$\left\{ \begin{array}{l} V_{GH} = 13,5\text{ V} \\ \text{other inputs } 0\text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5	$\left\{ \begin{array}{l} V_{GL} = 1,7\text{ V} \\ \text{other inputs } 13,5\text{ V} \end{array} \right.$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5\text{ V} \\ V_{QH} = 10\text{ V} \end{array} \right.$
Output LOW	I_{QL}	15	-	-	mA	11,4	$\left\{ \begin{array}{l} V_{GH} = 7,5\text{ V} \\ V_{QL} = 1,7\text{ V} \end{array} \right.$
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0\text{ V}; V_Q = 0\text{ V}$
Supply data							
<u>Currents (per gate)</u>							
at V_{QL}	I_p	-	3,8	6	mA	13,5	$V_G = 13,5\text{ V}$
Dynamic data							
<u>Times</u>							
Propagation delay							
fall time	t_{pdf}	90	175	310	ns	12	$\left. \begin{array}{l} C_L = 10\text{ pF}; N = 1 \\ T_{amb} = 25\text{ }^\circ\text{C} \\ V_{pd} = 4,5\text{ V} \end{array} \right\}$
rise time	t_{pdr}	200	340	570	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

1) All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_p = 12\text{ V}$.

2) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_P = 15 \text{ V}$); $T_{amb} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

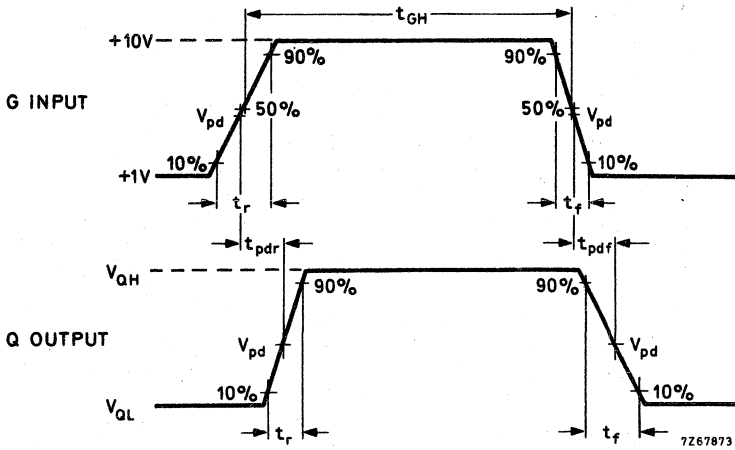
	Sym- bol	min. typ. 1) max.		Conditions and references			
				V_P (V)			
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	13,5	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	13,5 and 17	
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,0	1,7	V	13,5	
D.C. noise margin: HIGH	M_H	4,5	8,0	-	V	13,5	
	LOW	M_L	2,8	5,0	-	V	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	17	$\left\{ \begin{array}{l} V_{GH} = 17 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	1,0	1,8	mA	17	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 12 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	18	-	-	mA	13,5	
Output short-circuited 2)	$-I_{Qsc}$	9	15	25	mA	17	$V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
Supply data							
<u>Currents (per gate)</u>							
at V_{QL}	I_p	-	4,8	7,5	mA	17	$V_G = 17 \text{ V}$
Dynamic data							
<u>Times</u>							
Propagation delay							$\left. \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{amb} = 25 \text{ }^\circ\text{C} \\ V_{pd} = 4,5 \text{ V} \end{array} \right\}$
rise time	t_{pdr}	-	t.b.f.	-	ns	15	
output rise time	t_r	-	t.b.f.	-	ns	15	
output fall time	t_f	-	t.b.f.	-	ns	15	

1) All typical values under test conditions: $T_{amb} = 25 \text{ }^\circ\text{C}$ and $V_P = 15 \text{ V}$.

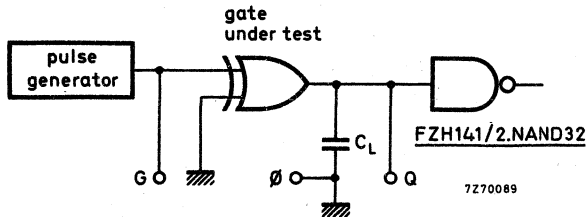
2) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): $t_r = 350 \text{ ns}$
 $t_f = 120 \text{ ns}$
 $t_{GH} = 1 \mu\text{s}$
 $V_{pd} = +4,5 \text{ V}$

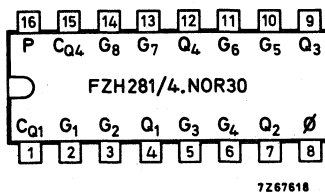
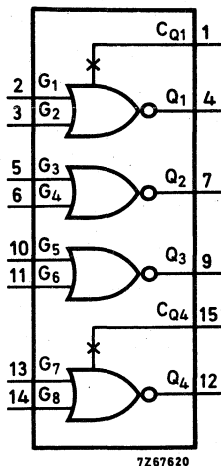


Measuring conditions: $V_p = +12 \text{ V}; +15 \text{ V}$
 $C_L = 10 \text{ pF}$ (including probe and jig capacitance)
 $T_{amb} = 25 \text{ }^\circ\text{C}$

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE NOR GATE with slow-down capability



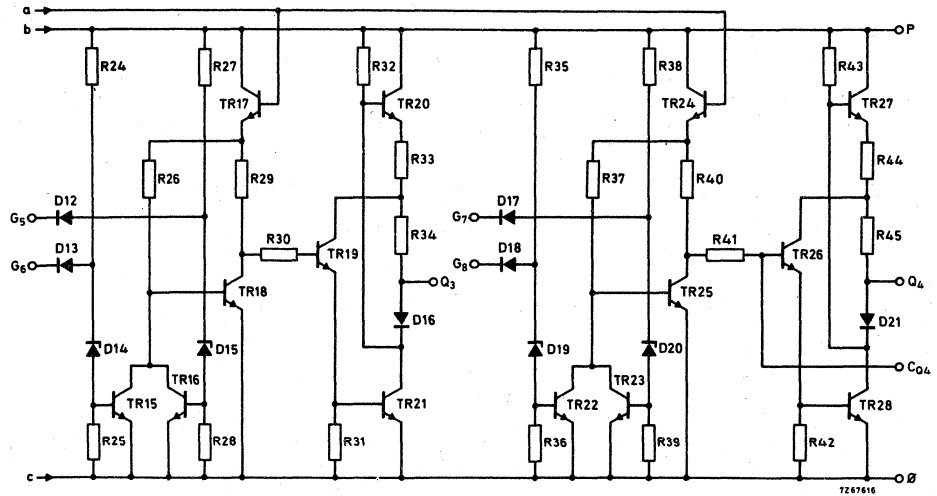
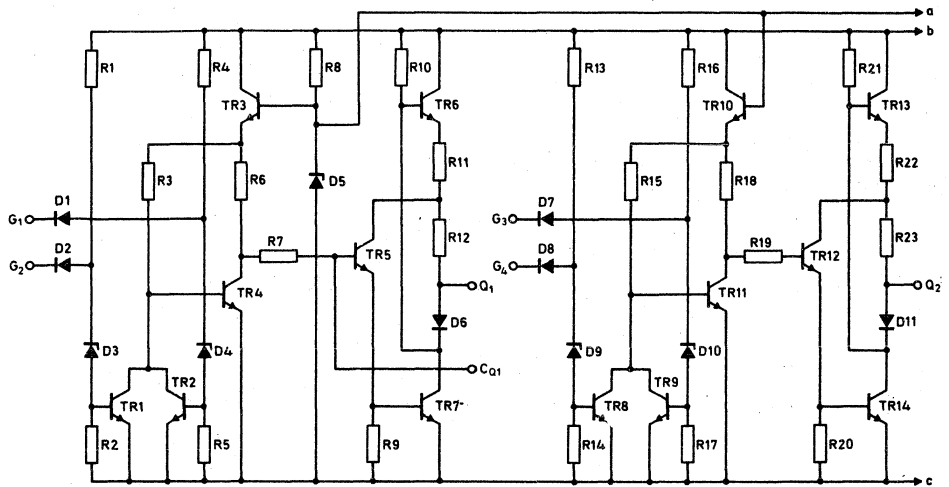
QUICK REFERENCE DATA

Supply voltage (range I)	V_p	nom.	12 V
(range II)	V_p	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	260 ns
Available d.c. fan-out $T_{amb} = 0$ to +70 °C	} LOW state	N_{aL}	max. 10
D.C. noise margin at $T_{amb} = 25$ °C			
range I: $V_p = 12$ V	}	$M_L = M_H$	typ. 5 V
range II: $V_p = 15$ V		M_L	typ. 5 V
		M_H	typ. 8 V
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I: $V_p = 12$ V	P_{av}	typ.	42 mW
range II: $V_p = 15$ V	P_{av}	typ.	63,8 mW

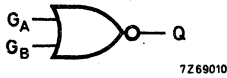
The FZH281/4.NOR30 consists of four 2-input NOR gates, two of which have the slow-down facility.

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC FUNCTION



$$Q = \overline{G_A + G_B} \text{ (positive logic)}$$

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

Function table

G _A	G _B	Q
L	L	H
H	X	L
X	H	L

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V _P	max.	18 V
Output voltage	V _Q	max.	V _P
Input voltage	V _G	max.	18 V
Input current at V _P = 17 V	-I _{GL}	max.	25 mA
Voltage difference between any two inputs		max.	18 V
Storage temperature	T _{stg}		-65 to +150 °C
Operating ambient temperature	T _{amb}		0 to +70 °C
Output short-circuit duration	t _{Qsc}	max.	1 s ¹⁾
Slow-down input voltage	+V _{CQ}	max.	0,6 V
	-V _{CQ}	max.	1,0 V
Slow-down input current	+I _{CQ}	max.	2,0 mA
	-I _{CQ}	max.	10,0 mA

¹⁾ Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70 °C	
Uniform system supply voltage (range I)	V_P	11,4 to 13,5 V	
(range II)	V_P	13,5 to 17 V	
Available d. c. fan-out	N_{aL}	max. 10	
	N_{aH}	max. 100	
D. C. noise margin; range I at V_{Pmin}	M_L	min. 2,8 V	
	M_H	min. 2,5 V	
range II at V_{Pmin}	M_L	min. 2,8 V	
	M_H	min. 4,5 V	
Supply current per gate	{ range I ; output HIGH output LOW range II; output HIGH output LOW	I_{pav}	typ. 3,3 mA
		I_{pav}	typ. 3,7 mA
		I_{pav}	typ. 3,8 mA
		I_{pav}	typ. 4,7 mA
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot}	max. 76,8 mW	
at range II; V_{Pmax}	P_{tot}	max. 114,8 mW	
Thermal resistance from system to ambient	R_{th}	max. 150 °C/W	

CHARACTERISTICS Test conditions: at range I ($V_p = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. 1) max.			Conditions and references	
					V_p (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{GH}	7,5	-	-	V	11,4 { $V_{QL} \leq 1,7\text{ V}$ $I_{QL} = 15\text{ mA}$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5 { $V_{QH} \geq 10\text{ V}$ $-I_{QH} = 0,1\text{ mA}$
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5 { $V_{GL} = 4,5\text{ V}$ $-I_{QH} = 0,1\text{ mA}$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4 { $V_{GH} = 7,5\text{ V}$ $I_{QL} = 15\text{ mA}$
D. C. noise margin: HIGH	M_H	2,5	5,0	-	V	11,4
LOW	M_L	2,8	5,0	-	V	11,4
<u>Currents (per gate)</u>						
Input HIGH	I_{GH}	-	-	1,0	μA	13,5 { $V_{GH} = 13,5\text{ V}$ other inputs 0 V
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5 { $V_{GL} = 1,7\text{ V}$ other inputs 13,5 V
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5 { $V_{GL} = 4,5\text{ V}$ $V_{QH} = 10\text{ V}$
Output LOW	I_{QL}	15	-	-	mA	11,4 { $V_{GH} = 7,5\text{ V}$ $V_{QL} = 1,7\text{ V}$
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	13,5 $V_G = 0\text{ V}; V_Q = 0\text{ V}$
Supply data						
<u>Currents (per gate)</u>						
at V_{QL}	I_p	-	3,7	6	mA	13,5 $V_G = 13,5\text{ V}$
Dynamic data						
<u>Times</u>						
Propagation delay						
fall time	t_{pdf}	200	340	570	ns	12 { $C_L = 10\text{ pF}; N = 1$ $T_{amb} = 25\text{ }^\circ\text{C}$ $V_{pd} = 4,5\text{ V}$
rise time	t_{pdr}	90	175	310	ns	
output rise time	t_r	200	340	570	ns	
output fall time	t_f	70	120	210	ns	

1) All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_p = 12\text{ V}$.

2) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_P = 15$ V); $T_{amb} = 0$ to $+70$ °C

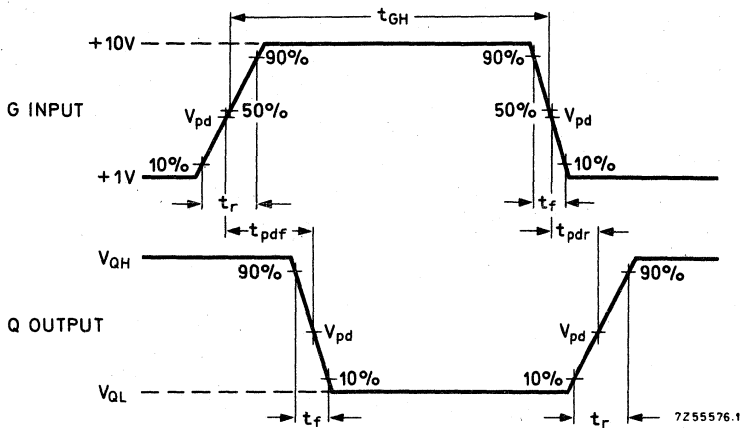
	Sym- bol	min. typ. ¹⁾ max.		Conditions and references			
				V_P (V)			
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	13,5	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	13,5 and 17	
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,0	1,7	V	13,5	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
D. C. noise margin: HIGH LOW	M_H	4,5	8,0	-	V	13,5	
	M_L	2,8	5,0	-	V	13,5	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	17	$\left\{ \begin{array}{l} V_{GH} = 17 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	1,0	1,8	mA	17	$\left\{ \begin{array}{l} V_{GL} = 1,7 \text{ V} \\ \text{other inputs } 17 \text{ V} \end{array} \right.$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 12 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	18	-	-	mA	13,5	$\left\{ \begin{array}{l} V_{GH} = 7,5 \text{ V} \\ V_{QL} = 1,7 \text{ V} \end{array} \right.$
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	17	$V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
Supply data							
<u>Currents (per gate)</u>							
at V_{QL}	I_P	-	4,7	7,5	mA	17	$V_G = 17 \text{ V}$
Dynamic data							
<u>Times</u>							
Propagation delay							
fall time	t_{pdf}	-	t. b. f.	-	ns	15	$\left. \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{amb} = 25 \text{ }^\circ\text{C} \\ V_{pd} = 4,5 \text{ V} \end{array} \right\}$
rise time	t_{pdr}	-	t. b. f.	-	ns	15	
output rise time	t_r	-	t. b. f.	-	ns	15	
output fall time	t_f	-	t. b. f.	-	ns	15	

¹⁾ All typical values under test conditions: $T_{amb} = 25$ °C and $V_P = 15$ V.

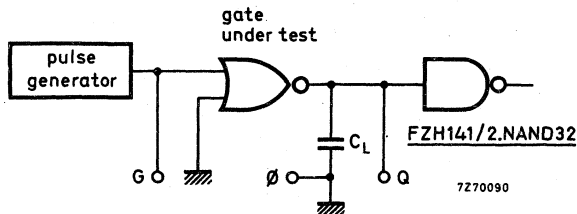
²⁾ Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): $t_r = 350 \text{ ns}$ $V_{pd} = +4,5 \text{ V}$
 $t_f = 120 \text{ ns}$
 $t_{GH} = 1 \mu\text{s}$

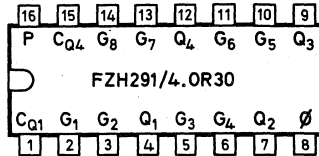
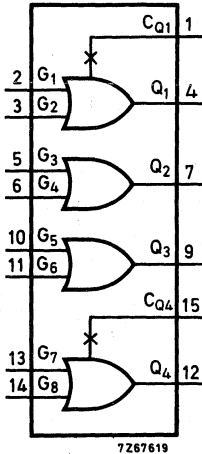


Measuring conditions: $V_p = +12 \text{ V}; +15 \text{ V}$
 $C_L = 10 \text{ pF}$ (including probe and jig capacitance)
 $T_{amb} = 25 \text{ }^\circ\text{C}$

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

QUADRUPLE OR GATE with slow-down capability

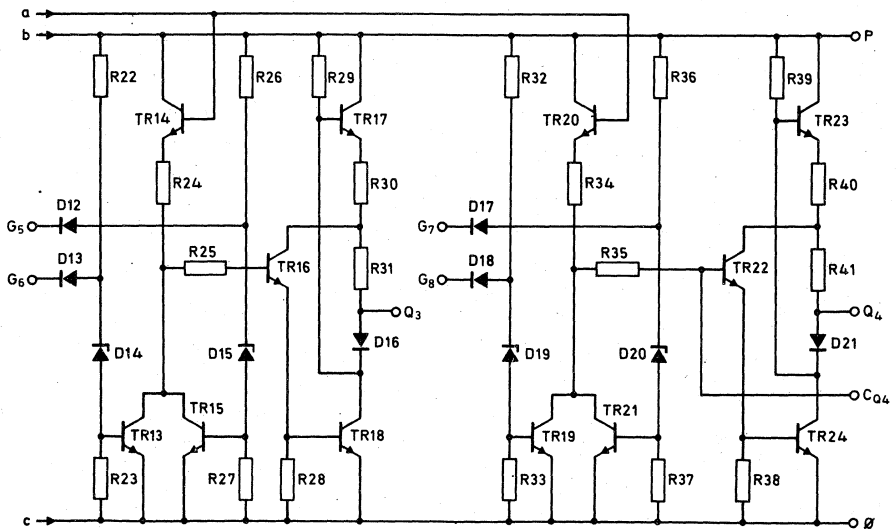
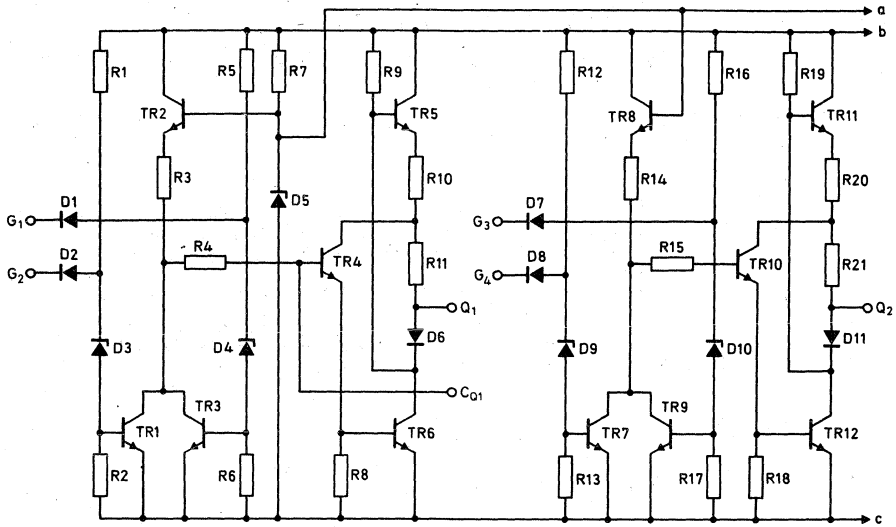


QUICK REFERENCE DATA			
Supply voltage (range I)	V_p	nom.	12 V
(range II)	V_p	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Average propagation delay ($N = 1$; $C_L = 10$ pF; $T_{amb} = 25$ °C; $V_{pd} = 4,5$ V)	t_{pd}	typ.	260 ns
Available d. c. fan-out $T_{amb} = 0$ to +70 °C	} LOW state	N_{aL}	max. 10
D. C. noise margin at $T_{amb} = 25$ °C			
range I : $V_p = 12$ V	$M_L = M_H$	typ.	5 V
range II: $V_p = 15$ V	} M_L	typ.	5 V
		M_H	typ.
Power consumption per gate at $T_{amb} = 25$ °C (50% duty cycle) range I : $V_p = 12$ V	P_{av}	typ.	35,1 mW
range II: $V_p = 15$ V	P_{av}	typ.	54 mW

The FZH291/4.OR30 consists of four 2-input OR gates, two of which may be slowed down.

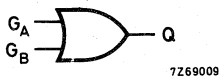
PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



7267615

LOGIC FUNCTION



$$Q = G_A + G_B \text{ (positive logic)}$$

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

Function table

G_A	G_B	Q
L	L	L
H	X	H
X	H	H

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Output voltage	V_Q	max.	V_P
Input voltage	V_G	max.	18 V
Input current at $V_P = 17$ V	$-I_{GL}$	max.	25 mA
Voltage difference between any two inputs		max.	18 V
Storage temperature	T_{stg}		-65 to +150 °C
Operating ambient temperature	T_{amb}		0 to +70 °C
Output short-circuit duration	t_{Qsc}	max.	1 s ¹⁾
Slow-down input voltage	$+V_{CQ}$	max.	0,6 V
	$-V_{CQ}$	max.	1,0 V
Slow-down input current	$+I_{CQ}$	max.	2,0 mA
	$-I_{CQ}$	max.	10,0 mA

¹⁾ Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70 °C	
Uniform system supply voltage (range I)	V_P	11, 4 to 13, 5 V	
(range II)	V_P	13, 5 to 17 V	
Available d. c. fan-out	N_{aL} max.	10	
	N_{aH} max.	100	
D. C. noise margin; range I at V_{Pmin}	M_L min.	2, 8 V	
	M_H min.	2, 5 V	
range II at V_{Pmin}	M_L min.	2, 8 V	
	M_H min.	4, 5 V	
Supply current per gate	range I ; output HIGH	I_{pav} typ.	2, 25 mA
		output LOW	I_{pav} typ.
	range II; output HIGH	I_{pav} typ.	2, 6 mA
		output LOW	I_{pav} typ.
Power consumption per gate (50% duty cycle) at range I ; V_{Pmax}	P_{tot} max.	64, 1 mW	
at range II; V_{Pmax}	P_{tot} max.	104, 1 mW	
Thermal resistance from system to ambient	R_{th} max.	150 °C/W	

CHARACTERISTICS Test conditions: at range I ($V_p = 12$ V); $T_{amb} = 0$ to $+70$ °C

	Sym- bol	min. typ. 1) max.			Conditions and references		
					V_p (V)		
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	11,4	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 15 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5	
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	
D.C. noise margin: HIGH LOW	M_H	2,5	5,0	-	V	11,4	
	M_L	2,8	5,0	-	V	11,4	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μ A	13,5	$\left\{ \begin{array}{l} V_{GH} = 13,5 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 10 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	15	-	-	mA	11,4	
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	13,5	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
<u>Currents (per gate)</u>							
at V_{QH}	I_p	-	3,6	5,8	mA	13,5	$V_G = 13,5$ V
Dynamic data							
<u>Times</u>							
Propagation delay							$\left\{ \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{amb} = 25 \text{ }^\circ\text{C} \\ V_{pd} = 4,5 \text{ V} \end{array} \right.$
fall time	t_{pdf}	90	175	310	ns	12	
rise time	t_{pdr}	200	340	570	ns	12	
output rise time	t_r	200	340	570	ns	12	
output fall time	t_f	70	120	210	ns	12	

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_p = 12$ V.

2) Short-circuit duration max. 1 s.

CHARACTERISTICS Test conditions: at range II ($V_p = 15$ V); $T_{amb} = 0$ to $+70$ °C

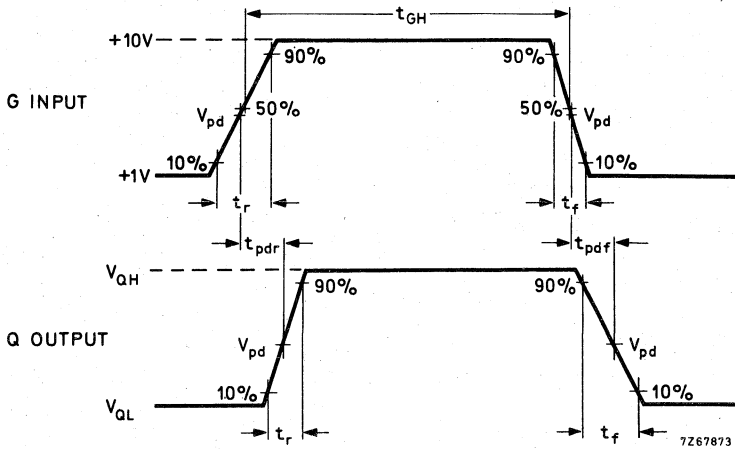
	Sym- bol	min. typ. ¹⁾ max.		Conditions and references			
				V_p (V)			
Static data							
<u>Voltages</u>							
Input HIGH	V_{GH}	7,5	-	-	V	13,5	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
Input LOW	V_{GL}	-	-	4,5	V	13,5 and 17	
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,0	1,7	V	13,5	
D. C. noise margin: HIGH	M_H	4,5	8,0	-	V	13,5	
LOW	M_L	2,8	5,0	-	V	13,5	
<u>Currents (per gate)</u>							
Input HIGH	I_{GH}	-	-	1,0	μA	17	$\left\{ \begin{array}{l} V_{GH} = 17 \text{ V} \\ \text{other inputs } 0 \text{ V} \end{array} \right.$
Input LOW	$-I_{GL}$	-	1,0	1,8	mA	17	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	$\left\{ \begin{array}{l} V_{GL} = 4,5 \text{ V} \\ V_{QH} = 12 \text{ V} \end{array} \right.$
Output LOW	I_{QL}	18	-	-	mA	13,5	
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25	mA	17	$V_G = 0$ V; $V_Q = 0$ V
Supply data							
<u>Currents (per gate)</u>							
at V_{QH}	I_p	-	4,6	7,3	mA	17	$V_G = 17$ V
Dynamic data							
<u>Times</u>							
Propagation delay							
fall time	t_{pdf}	-	t. b. f.	-	ns	15	$\left. \begin{array}{l} C_L = 10 \text{ pF}; N = 1 \\ T_{amb} = 25 \text{ }^\circ\text{C} \\ V_{pd} = 4,5 \text{ V} \end{array} \right\}$
rise time	t_{pdr}	-	t. b. f.	-	ns	15	
output rise time	t_r	-	t. b. f.	-	ns	15	
output fall time	t_f	-	t. b. f.	-	ns	15	

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_p = 15$ V.

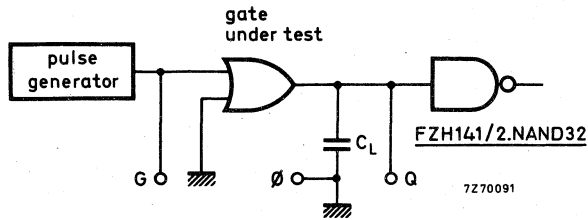
2) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): $t_r = 350 \text{ ns}$ $V_{pd} = +4, 5 \text{ V}$
 $t_f = 120 \text{ ns}$
 $t_{GH} = 1 \mu\text{s}$



Measuring conditions: $V_p = +12 \text{ V}; +15 \text{ V}$
 $C_L = 10 \text{ pF}$ (including probe and jig capacitance)
 $T_{amb} = 25 \text{ }^\circ\text{C}$

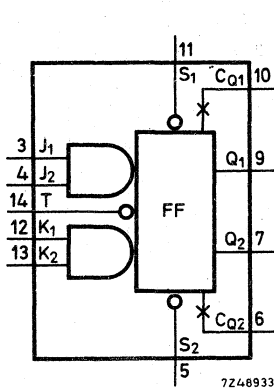
Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf}

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

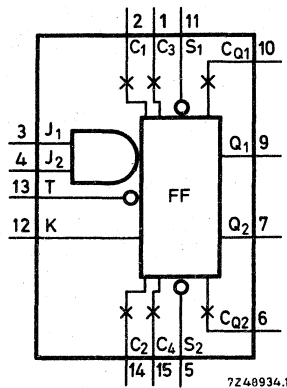
SINGLE JK MASTER-SLAVE FLIP-FLOPS

FZJ101/FF30: with slow-down capability on the slave

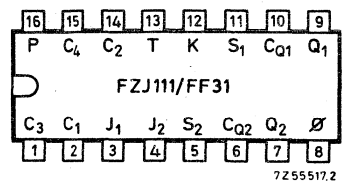
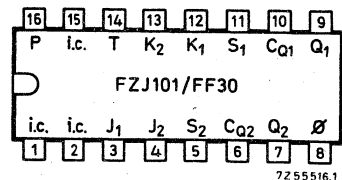
FZJ111/FF31: with slow-down capability on master and slave



FZJ101/FF30



FZJ111/FF31



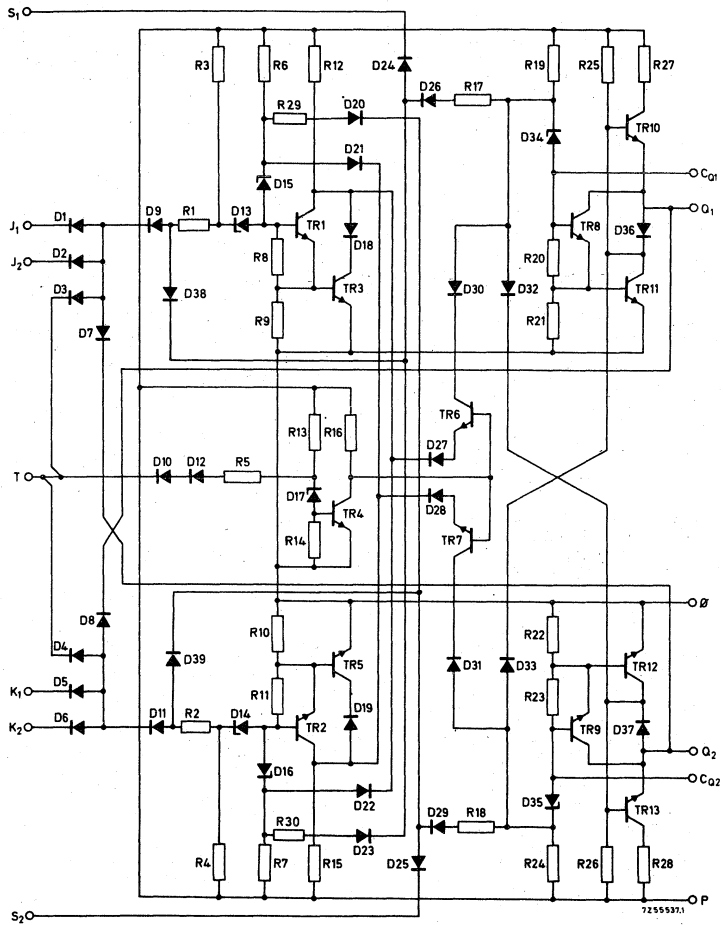
QUICK REFERENCE DATA

Supply voltage (range I)	V_p	nom.	12	V
(range II)	V_p	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d. c. fan-out ($T_{amb} = 0$ to +70 °C) } LOW state	N_{aL}	max.	10	
Operating frequency at $T_{amb} = 25$ °C duty cycle 50%; range I/II	f_c	typ.	0,5	MHz
Average supply current at $T_{amb} = 25$ °C				
$V_p = 13,5$ V	I_{pav}	typ.	8	mA
$V_p = 17$ V	I_{pav}	typ.	11	mA
D. C. noise margin at $T_{amb} = 25$ °C				
range I : $V_p = 12$ V	$M_L = M_H$	typ.	5	V
range II : $V_p = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V

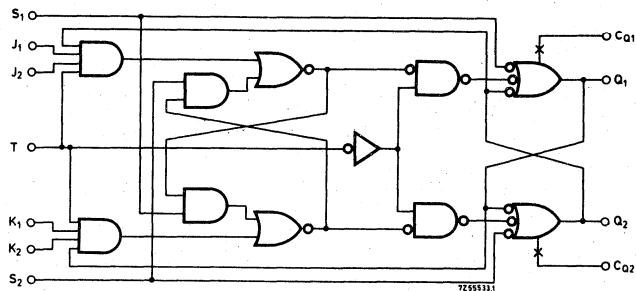
PACKAGE OUTLINE 16-lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM

FZJ101/FF30



LOGIC DIAGRAM



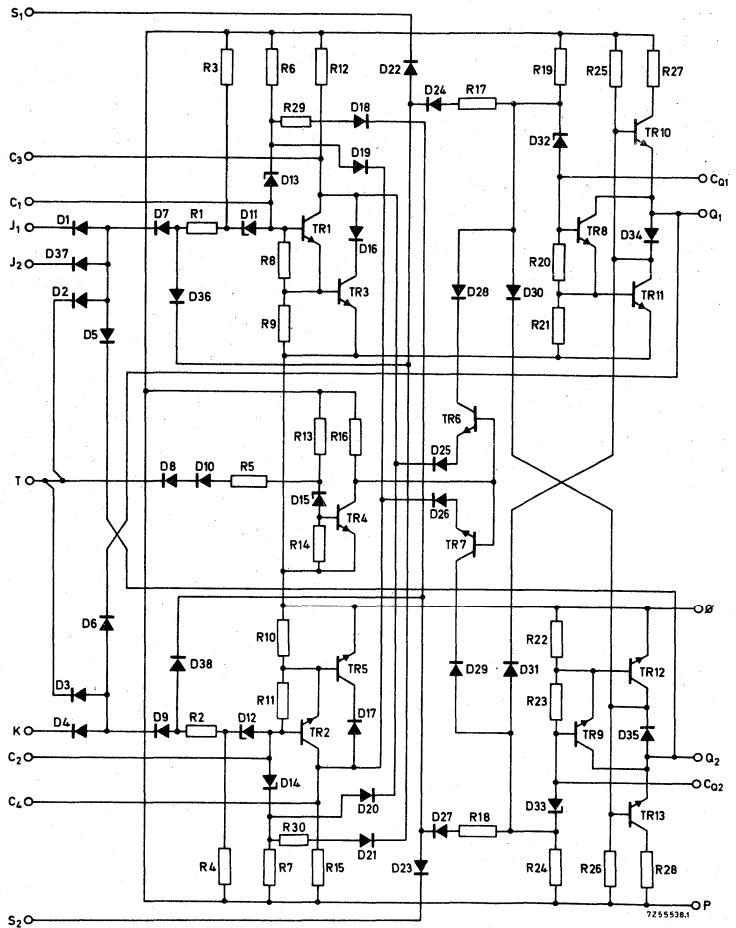
2722 006 00001
2722 006 00011

SINGLE JK MASTER-SLAVE FLIP-FLOPS

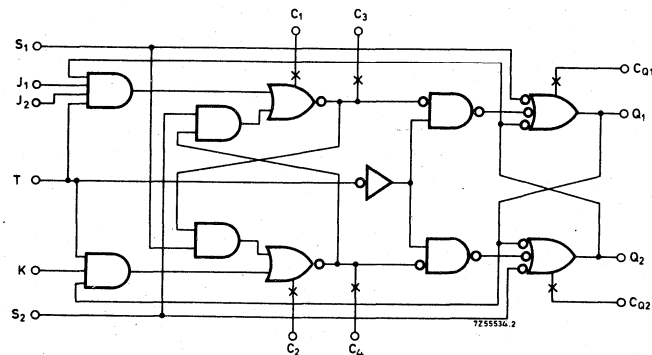
FZJ101/FF30
FZJ111/FF31

CIRCUIT DIAGRAM

FZJ111/FF31



LOGIC DIAGRAM



GENERAL DESCRIPTION

The FZJ101/FF30 consists of a single JK master-slave flip-flop with two J and K inputs and also has a slow-down capability on the slave of the flip-flop. So the reaction time of the slave to the negative-going clock-edge can be increased. This can be achieved by connecting external capacitors between the output terminals and their associated slow-down terminals.

The FZJ111/FF31 consists of a single JK master-slave flip-flop with two J inputs and one K input and has a slow-down capability both on the master and the slave of the flip-flop. For slowing down the slave see FZJ101/FF30.

The reaction time of the master to the positive-going clock-edge can be increased by connecting external capacitors between the slow-down terminals C₁, C₃ and C₂, C₄ respectively. Furthermore a minimum slope of the T-signal is required.

LOGIC FUNCTIONS

FZJ101/FF30

$$J = J_1 \cdot J_2$$

$$K = K_1 \cdot K_2$$

FZJ111/FF31

$$J = J_1 \cdot J_2$$

$$K = K$$

Function tables

t _n		t _{n+1}	
J	K	Q ₁	Q ₂
L	L	Q _{1n}	Q _{2n}
L	H	L	H
H	L	H	L
H	H	Q _{2n}	Q _{1n}
Q ₂ is opposite Q ₁			

The set inputs S₁ and S₂ override all the other inputs.

S ₁	S ₂	Q ₁	Q ₂
L	H	H	L
H	L	L	H
H	H	Q ₁	Q ₂ 1)
L	L	H	H 2)

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

- 1) Q₂ is opposite Q₁
- 2) If S₁ and S₂ return to HIGH simultaneously the Q-states will be indeterminate.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V _P	max.	18 V
Output voltage	V _Q	max.	12 V
Input voltage	V _J , V _K , V _T	max.	18 V
Input current at V _P = 17 V	-I _{IL}	max.	25 mA 1)
Storage temperature	T _{stg}	-65 to +150	°C
Operating ambient temperature	T _{amb}	0 to +70	°C

1) All inputs except slow-down inputs.

NOTE

The slow-down terminals indicated by crosses are for slow-down purposes only; they are not to be connected to any other terminal.

RATINGS (continued)

Output short-circuit duration	t_{Qsc}	max.	1	s	1)
Slow-down input voltage	$\left\{ \begin{array}{l} +V_{CQ} \\ -V_{CQ} \end{array} \right.$	max.	0,6	V	
		max.	1,0	V	
Slow-down input current	$\left\{ \begin{array}{l} +I_{CQ} \\ -I_{CQ} \end{array} \right.$	max.	2,0	V	
		max.	10,0	V	

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70	°C
Uniform system supply voltage (range I) (range II)	V_P	11,4 to 13,5	V
	V_P	13,5 to 17	V
Available d. c. fan-out	N_{aL}	max.	10
D. C. noise margin to all inputs: range I at V_{Pmin} range II at V_{Pmin}	$\left\{ \begin{array}{l} M_L \\ M_H \end{array} \right.$	min.	2,8 V
		min.	2,5 V
	$\left\{ \begin{array}{l} M_L \\ M_H \end{array} \right.$	min.	2,8 V
		min.	4,5 V
Average propagation delay time at $V_{pd} = 4,5$ V			
T → Q: at range I; $V_P = 12$ V at range II; $V_P = 15$ V	t_{pd}	max.	645 ns
		typ.	400 ns
S → Q: at range I; $V_P = 12$ V at range II; $V_P = 15$ V	t_{pd}	max.	455 ns
		typ.	265 ns
Maximum clock rate at $T_{amb} = 25$ °C duty cycle 50%; range I/II			
Supply current at range I: $V_P = 12$ V range II: $V_P = 15$ V	I_P	typ.	0,5 MHz
		min.	0,2 MHz
Supply current at range I: $V_P = 12$ V range II: $V_P = 15$ V	I_P	typ.	8 mA
		typ.	11 mA
Thermal resistance from system to ambient	R_{th}	max.	150 °C/W

1) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I ($V_P = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH: J, K, T, S	V_{IH}	7,5	-	- V	11,4	$\left\{ \begin{array}{l} V_{QL} \leq 1,7\text{ V} \\ I_{QL} = 15\text{ mA} \end{array} \right.$
Input LOW: J, K, S	V_{IL}	-	-	4,5 V	11,4	
T	V_{TL}	-	-	4,0 V	13,5	$\left\{ \begin{array}{l} V_{QH} \geq 10\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{array} \right.$
Output HIGH	V_{QH}	10	11,3	- V	11,4 and 13,5	
Output LOW	V_{QL}	-	0,9	1,7 V	11,4	$\left\{ \begin{array}{l} V_{IL} = 4,5\text{ V} \\ -I_{QH} = 0,1\text{ mA} \\ V_{IH} = 7,5\text{ V} \\ I_{QL} = 15\text{ mA} \end{array} \right.$
D. C. noise margin: HIGH	M_H	2,5	5,0	- V	11,4	
LOW	M_L	2,8	5,0	- V	11,4	
<u>Currents</u>						
Input HIGH: J, K, S	I_{IH}	-	-	1 μA	13,5	$\left\{ \begin{array}{l} V_{IH} = 13,5\text{ V} \\ \text{(other inputs } 0\text{V)} \end{array} \right.$
T	I_{TH}	-	-	3 μA		
Input LOW: J, K	$-I_{IL}$	-	0,8	1,5 mA	13,5	$\left\{ \begin{array}{l} V_{JL} = V_{KL} = 1,7\text{ V} \\ V_{TL} = 1,7\text{ V} \\ V_{SL} = 1,7\text{ V} \end{array} \right.$
T	$-I_{TL}$	-	1,6	3,0 mA	13,5	
S ²⁾	$-I_{SL}$	-	0,8	1,5 mA	13,5	
Output HIGH	$-I_{QH}$	0,1	-	- mA	11,4 and 13,5	$\left\{ \begin{array}{l} V_{QH} = 10\text{ V} \\ V_{QL} = 1,7\text{ V} \end{array} \right.$
Output LOW	I_{QL}	15	-	- mA	11,4	
Output short-circuited ³⁾	$-I_{Qsc}$	10	30	50 mA	13,5	$V_I = 0\text{V}; V_Q = 0\text{V}$
Supply data						
Supply current	I_P	-	8,0	- mA	13,5	

1) All typ. values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

2) For dynamic: $-I_{SL} = 1,5 \times$ specified values.

3) Short-circuited duration max. 1 s.

CHARACTERISTICS (continued)

Test conditions : at range I ($V_P = 12$ V); $T_{amb} = 0$ to $+70$ °C

	Sym- bol	min.	typ. 1)	max.		Conditions and references
Dynamic data						
<u>Times</u>						
Propagation delay:						
T → Q						
fall time	t_{pdf}	270	450	770	ns	$C_L = 10$ pF $N = 1$ $T_{amb} = 25$ °C $V_{pd} = 4,5$ V
rise time	t_{pdr}	160	290	520	ns	
S → Q						
fall time	t_{pdf}	180	330	580	ns	
rise time	t_{pdr}	70	165	330	ns	
output rise time	t_r	200	340	570	ns	
output fall time	t_f	70	120	210	ns	
Clock rate (duty cycle 50%)	f_c	0,2	0,5	-	MHz	
Input times						
T input	t_{TH}	0,6	-	-	µs	
	t_{TL}	0,6	-	-	µs	
S input	t_{SL}	1,0	-	-	µs	
J or K input						
hold time	t_{hold}	0	-	-	ns	
set-up time	t_{su}	0	-	-	ns	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

1) All typical values under test conditions : $T_{amb} = 25$ °C and $V_P = 12$ V.

CHARACTERISTICS (continued)

Test conditions: at range II ($V_p = 15$ V); $T_{amb} = 0$ to $+70$ °C

	Sym- bol	min. typ. 1) max.			Conditions and references		
					V_p (V)		
Static data							
<u>Voltages</u>							
Input HIGH: J, K, T, S	V_{IH}	7,5	-	-	V	13,5	$\left\{ \begin{array}{l} V_{QL} \leq 1,7 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
Input LOW: J, K, S	V_{IL}	-	-	4,5	V	13,5	
T	V_{TL}	-	-	4,0	V	17	$\left\{ \begin{array}{l} V_{QH} \leq 12 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right.$
Output HIGH	V_{QH}	12	14,3	-	V	13,5 and 17	
Output LOW	V_{QL}	-	1,0	1,7	V	13,5	$\left\{ \begin{array}{l} V_{IL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \\ V_{IH} = 7,5 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right.$
D. C. noise margin: HIGH	M_H	4,5	8,0	-	V	13,5	
LOW	M_L	2,8	5,0	-	V	13,5	
<u>Currents</u>							
Input HIGH: J, K, S	I_{IH}	-	-	1,0	μ A	17	$\left\{ \begin{array}{l} V_{IH} = 17 \text{ V} \\ \text{(other inputs 0 V)} \end{array} \right.$
T	I_{TH}	-	-	3,0	μ A	17	
Input LOW: J, K	$-I_{IL}$	-	1,0	1,8	mA	17	$\left\{ \begin{array}{l} V_{JL} = V_{KL} = 1,7 \text{ V} \\ V_{TL} = 1,7 \text{ V} \\ V_{SL} = 1,7 \text{ V} \end{array} \right.$
T	$-I_{TL}$	-	2,0	3,6	mA	17	
S 2)	$-I_{SL}$	-	1,0	1,8	mA	17	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 and 17	$\left. \begin{array}{l} \\ \end{array} \right\} V_{QH} = 12 \text{ V}$
Output LOW	I_{QL}	18	-	-	mA	13,5	
Output short-circuited	$-I_{Qsc}^3)$	15	37	60	mA	17	$V_I = 0 \text{ V}; V_Q = 0 \text{ V}$
Supply data							
Supply current	I_p	-	11	-	mA	17	

1) All typ. values under test conditions: $T_{amb} = 25$ °C and $V_p = 15$ V.

2) For dynamic: $-I_{SL} = 1,5$ x specified values.

3) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Test conditions : at range II ($V_P = 15 \text{ V}$); $T_{amb} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

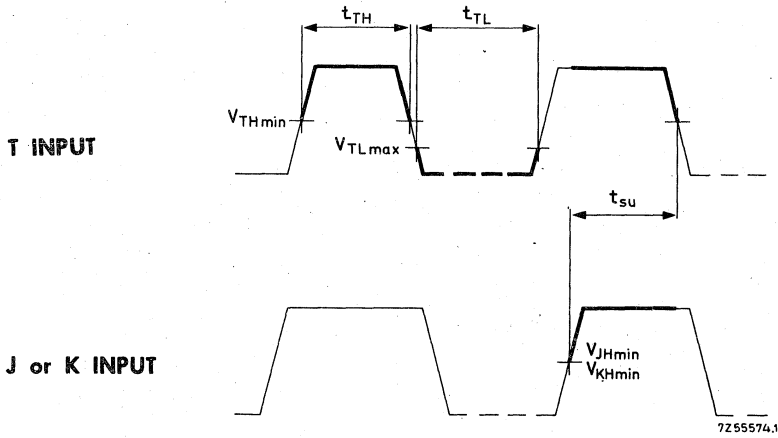
	Sym- bol	min. typ. 1) max.				Conditions and references
Dynamic data						
<u>Times</u>						
Propagation delay:						
T → Q						
fall time	t_{pdf}	-	470	-	ns	
rise time	t_{pdr}	-	330	-	ns	
S → Q						
fall time	t_{pdf}	-	340	-	ns	
rise time	t_{pdr}	-	195	-	ns	
output rise time	t_r	-	410	-	ns	
output fall time	t_f	-	75	-	ns	
Clock rate (duty cycle 50%)	f_c	-	0,5	-	MHz	
Input times						
T input	t_{TH}	0,6	-	-	μs	
	t_{TL}	0,6	-	-	μs	
S input	t_{SL}	1,0	-	-	μs	
J or K input						
hold time	t_{hold}	0	-	-	μs	
set-up time	t_{su}	0	-	-	μs	
T input slope	$(-dV/dt)_{Tmin}$			1	V/ μs	

$C_L = 10 \text{ pF}$
 $N = 1$
 $T_{amb} = 25 \text{ }^\circ\text{C}$
 $V_{pd} = 4,5 \text{ V}$

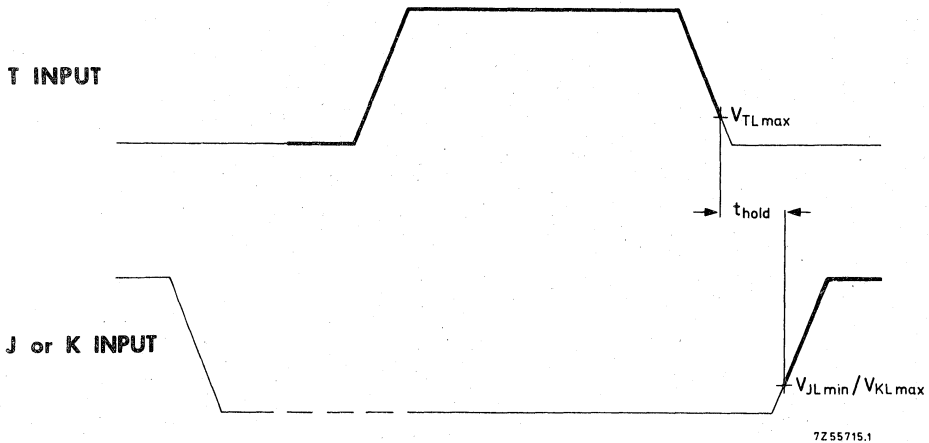
1) All typical values under test conditions : $T_{amb} = 25 \text{ }^\circ\text{C}$ and $V_P = 15 \text{ V}$.

CHARACTERISTICS (continued)

Dynamic data



Waveforms illustrating conditions for change of state

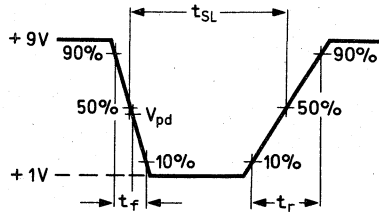


Waveforms illustrating conditions for no change of state

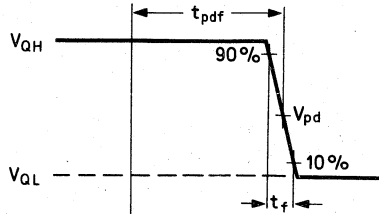
CHARACTERISTICS (continued)

Dynamic data

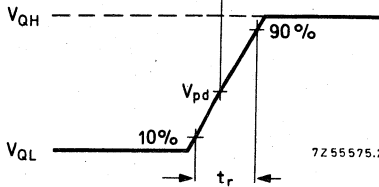
$S_2(S_1)$ INPUT



$Q_1(Q_2)$ OUTPUT

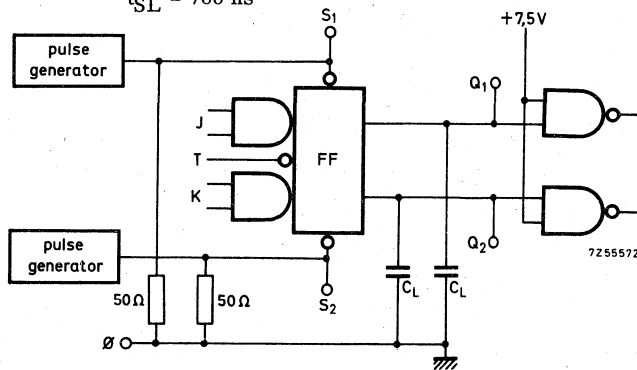


$Q_2(Q_1)$ OUTPUT



Pulse generator (S-input): $t_r = 350$ ns
 $t_f = 120$ ns
 $t_{SL} = 700$ ns

$V_{pd} = +4, 5$ V



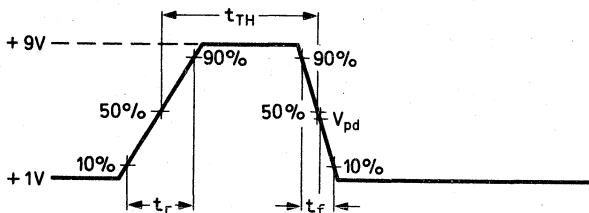
Measuring conditions: $V_p = +12$ V; $+15$ V
 $C_L = 10$ pF (including probe and jig capacitance)
 $T_{amb} = 25$ °C
Slow-down terminals are not connected
All other inputs are floating.

Waveforms illustrating conditions for set inputs. Set input signals are not supplied simultaneously.

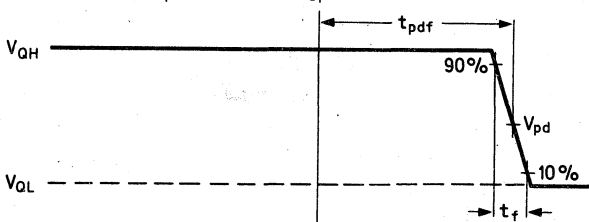
CHARACTERISTICS (continued)

Dynamic data

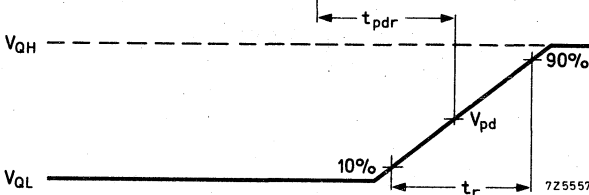
T INPUT



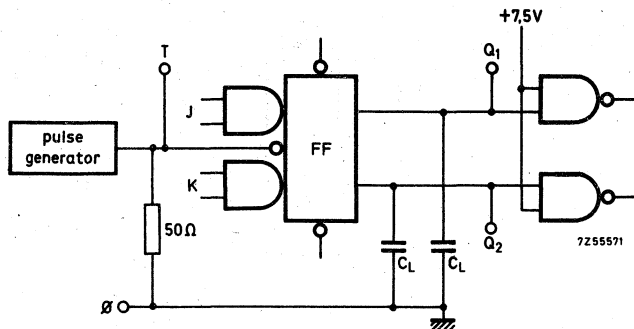
Q₁(Q₂) OUTPUT



Q₂(Q₁) OUTPUT



Pulse generator (T-input): $t_r = 350$ ns
 $t_f = 120$ ns
 $t_{TH} = 400$ ns
 $V_{pd} = +4, 5$ V

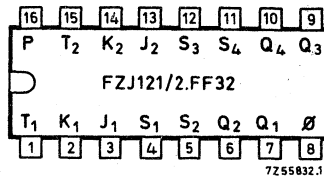
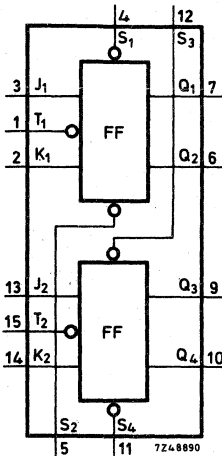


Measuring conditions: $V_p = +12$ V; +15 V
 $C_L = 10$ pF (including probe and jig capacitance)
 $T_{amb} = 25$ °C
Slow-down terminals are not connected
All other inputs are floating.

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf} .

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL JK MASTER-SLAVE FLIP-FLOP



QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d. c. fan-out	N_{aL}	max.	10	LOW state
$T_{amb} = 0$ to +70 °C				
Operating frequency at $T_{amb} = 25$ °C duty cycle 50%: range I/II	f_c	typ.	0,5	MHz
Average supply current at $T_{amb} = 25$ °C	I_{Pav}	typ.	15	mA
	I_{Pav}	typ.	20	mA
D. C. noise margin at $T_{amb} = 25$ °C	$M_L = M_H$	typ.	5	V
			5	V
			8	V
range I : $V_P = 12$ V				
range II : $V_P = 15$ V				

PACKAGE OUTLINE 16-lead plastic dual in-line (see general section).

GENERAL DESCRIPTION

The FZJ121/2.FF32 comprises two independent JK flip-flops, operating on the master-slave principle. Operation depends on voltage levels only, e.g. rise and fall times of all input signals including the trigger signals are immaterial.

The set and reset inputs (overriding any other input) are active at LOW level. There are no slow-down terminals.

Typical applications include counters and shift registers.

FUNCTION TABLES

t_n		t_{n+1}
J ₁	K ₁	Q ₁
J ₂	K ₂	Q ₃
L	L	Q _n
L	H	L
H	L	\overline{H}
H	H	$\overline{Q_n}$
Q ₂ is opposite Q ₁		
Q ₄ is opposite Q ₃		

S ₁	S ₂	Q ₁	Q ₂
S ₃	S ₄	Q ₃	Q ₄
L	H	H	L
H	L	L	H
H	H	Q ₁ (Q ₃)	Q ₂ (Q ₄) ¹⁾
L	L	X	X ²⁾

1) Q₂(Q₄) is opposite Q₁(Q₃)
 2) If S₁ (S₃) and S₂ (S₄) return to HIGH simultaneously the Q-states will be indeterminate.

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V _P	max.	18	V
Output voltage	V _Q	max.	V _P	
Input voltage	V _J , V _K , V _T	max.	18	V
Input current at V _P = 17 V	-I _{IL}	max.	25	mA
Storage temperature	T _{stg}		-65 to +150	°C
Operating ambient temperature	T _{amb}		0 to +70	°C
Output short-circuit duration	t _{Qsc}	max.	1	s ¹⁾

¹⁾ Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70	$^{\circ}C$
Uniform system supply voltage (range I) (range II)	V_P	11,4 to 13,5	V
	V_P	13,5 to 17	V
Available d.c. fan-out	N_{aL}	max. 10	
D.C. noise margin to all inputs: range I at V_{Pmin} range II at V_{Pmin}	{ M_L	min. 2,8	V
		min. 2,5	V
	{ M_H	min. 2,8	V
		min. 4,5	V
Supply current at range I : $V_P = 12$ V range II : $V_P = 15$ V	I_P	typ. 15	mA
	I_P	typ. 20	mA
Thermal resistance from system to ambient	R_{th}	max. 150	$^{\circ}C/W$



CHARACTERISTICS Test conditions: at range I ($V_P = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min.	typ. ¹⁾	max.	Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH: T J; K S	V_{TH}	6,5	-	-	V	} $V_{QL} \leq 1,7\text{ V}$ $I_{QL} = 15\text{ mA}$
	V_{IH}	8,0	-	-	V	
	V_{SH}	7,5	-	-	V	
Input LOW: T J; K S	V_{TL}	-	-	4,0	V	} $V_{QH} \geq 10\text{ V}$ and $-I_{QH} = 0,1\text{ mA}$
	V_{IL}	-	-	5,5	V	
	V_{SL}	-	-	4,5	V	
Output HIGH	V_{QH}	10,0	11,3	-	V	} $V_{IL} \leq 4,5\text{ V}^2)$ and $-I_{QH} = 0,1\text{ mA}$
Output LOW	V_{QL}	-	0,9	1,7	V	} $V_{IH} \geq 7,5\text{ V}^2)$ $I_{QL} = 15\text{ mA}$
D. C. noise margin: HIGH LOW	M_H	2,5	5,0	-	V	} $V_{IL} \leq 4,5\text{ V}^2)$ and $-I_{QH} = 0,1\text{ mA}$
	M_L	2,8	5,0	-	V	
<u>Currents</u>						
Input HIGH: T J; K; S	I_{TH}	-	-	3	μA	} $V_{IH} = 13,5\text{ V}$ (other inputs 0V)
	I_{IH}	-	-	1	μA	
Input LOW: T J; K; S ³⁾	$-I_{TL}$	-	1,6	3,0	mA	} $V_{IL} = 1,7\text{ V}$ $V_{IL} = 1,7\text{ V}$
	$-I_{IL}$	-	0,8	1,5	mA	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	} $V_{QH} = 10\text{ V}$
Output LOW	I_{QL}	15	-	-	mA	} $V_{QL} = 1,7\text{ V}$
<u>Supply data</u>						
Supply current	I_P	-	15	24	mA	13,5

1) All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.
 2) Measured to S_2 and S_1 .
 3) For dynamic: $-I_{SL} = 1,5 \times$ specified values.

CHARACTERISTICS (continued)Test conditions: at range I ($V_p = 12$ V); $T_{amb} = 0$ to $+70$ °C

	Sym- bol	min.	typ. 1)	max.		Conditions and references
Dynamic data						
<u>Times</u>						
Propagation delay:						
T → Q						
fall time	t_{pdf}	270	450	770	ns	$C_L = 10$ pF $N = 1$ $T_{amb} = 25$ °C $V_{pd} = 4,5$ V
rise time	t_{pdr}	160	290	520	ns	
R or S → Q						
fall time	t_{pdf}	180	330	580	ns	
rise time	t_{pdr}	70	165	330	ns	
output fall time	t_f	70	120	210	ns	
output rise time	t_r	200	340	570	ns	
Clock rate (duty cycle 50%)	f_c	0,2	0,5	-	MHz	
Input times						
T input	t_{TH}	0,6	-	-	µs	
R input	t_{RL}	1,0	-	-	µs	
S input	t_{SL}	1,0	-	-	µs	
J or K input						
hold time	t_{hold}	0	-	-	ns	
set-up time	t_{su}	0	-	-	ns	
T input slope	$(-dV/dt)_{Tmin}$			1	V/µs	

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_p = 12$ V.

CHARACTERISTICS (continued)

Test conditions: at range II ($V_P = 15 \text{ V}$); $T_{amb} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

	Sym- bol	min. typ. 1) max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH: T J; K S	V_{TH}	6,5	-	-	V	} $V_{QL} \leq 1,7 \text{ V}$ $I_{QL} = 18 \text{ mA}$
	V_{IH}	8,0	-	-	V	
	V_{SH}	7,5	-	-	V	
Input LOW: T J; K S	V_{TL}	-	-	4,0	V	} $V_{QH} \geq 12 \text{ V}$ $-I_{QH} = 0,1 \text{ mA}$
	V_{IL}	-	-	5,5	V	
	V_{SL}	-	-	4,5	V	
Output HIGH	V_{QH}	12,0	14,3	-	V	11,4 } $V_{IL} \leq 4,5 \text{ V}^2)$ and } $-I_{QH} = 0,1 \text{ mA}$ 13,5
Output LOW	V_{QL}	-	1,1	1,7	V	13,5 } $V_{IH} \geq 7,5 \text{ V}^2)$ $I_{QL} = 18 \text{ mA}$
D. C. noise margin: HIGH LOW	M_H	4,5	8,0	-	V	13,5
	M_L	2,8	5,0	-	V	
<u>Currents</u>						
Input HIGH: T J; K; S	I_{TH}	-	-	3,0	μA	17 } $V_{IH} = 17 \text{ V}$ (other inputs 0V)
	I_{IH}	-	-	1,0	μA	
Input LOW: T J; K; S 3)	$-I_{TL}$	-	2,0	3,6	mA	17 } $V_{IL} = 1,7 \text{ V}$ 17
	$-I_{IL}$	-	1,0	1,8	mA	
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5 } $V_{QH} = 12 \text{ V}$ and } 17
Output LOW	I_{QL}	18	-	-	mA	13,5 } $V_{QL} = 1,7 \text{ V}$
Supply data						
Supply current	I_P	-	20	32	mA	17

1) All typical values under test conditions: $T_{amb} = 25 \text{ }^\circ\text{C}$ and $V_P = 15 \text{ V}$.

2) Measured to S_2 and S_1 .

3) For dynamic: $-I_{SL} = 1,5 \times$ specified values.

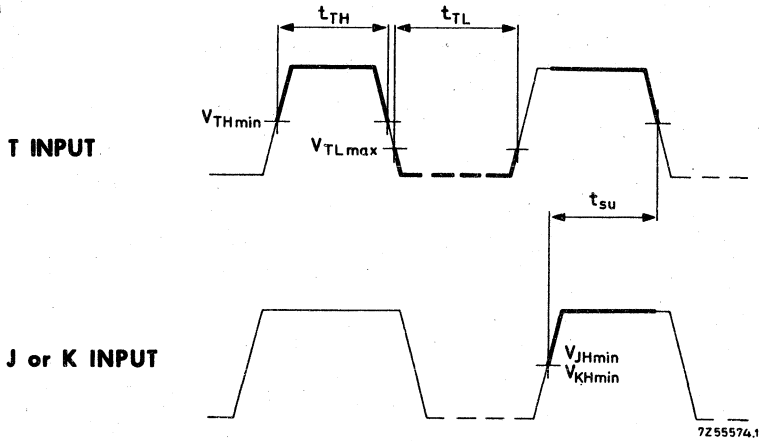
CHARACTERISTICS (continued)Test conditions at range II ($V_P = 15\text{ V}$); $T_{\text{amb}} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min.	typ. ¹⁾	max.	Conditions and references
Dynamic data					
Times					
Propagation delay:					
T \rightarrow Q					$C_L = 10\text{ pF}$ $N = 1$ $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ $V_{\text{pd}} = 4,5\text{ V}$
fall time	t_{pdf}	-	470	- ns	
rise time	t_{pdr}	-	330	- ns	
R or S \rightarrow Q					
fall time	t_{pdf}	-	340	- ns	
rise time	t_{pdr}	-	195	- ns	
output fall time	t_f	-	75	- ns	
output rise time	t_r	-	410	- ns	
Clock rate (duty cycle 50%)	f_c	0,2	0,5	- MHz	
Input times					
T input	t_{TH}	0,6	-	- μs	
R input	t_{RL}	0,6	-	- μs	
S input	t_{SL}	1,0	-	- μs	
J or K input					
hold time	t_{hold}	0	-	- ns	
set-up time	t_{su}	0	-	- ns	
T input slope	$(-dV/dt)_{\text{Tmin}}$			1 V/ μs	

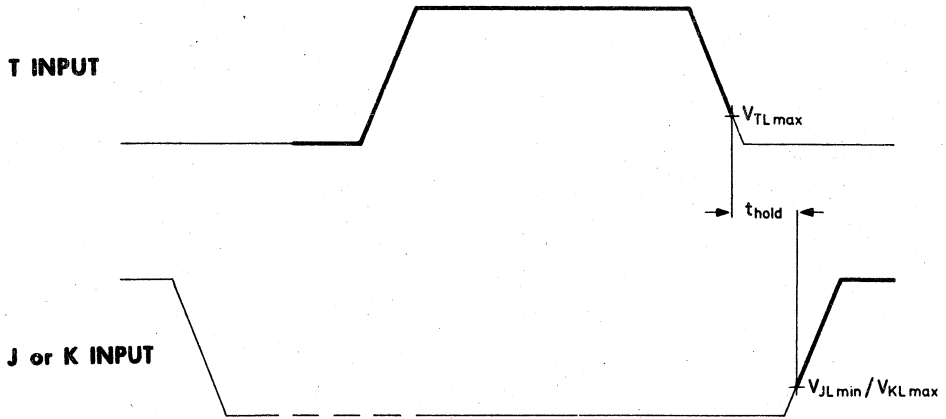
¹⁾ All typical values under test conditions: $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ and $V_P = 15\text{ V}$.

CHARACTERISTICS (continued)

Dynamic data



Waveforms illustrating conditions for change of state



Waveforms illustrating conditions for no change of state

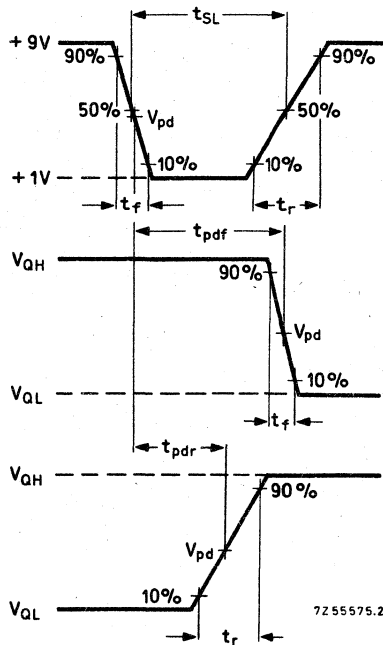
CHARACTERISTICS (continued)

Dynamic data

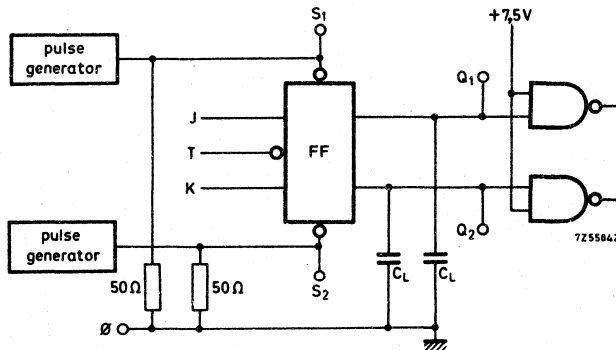
$S_2(S_1)$ INPUT

$Q_1(Q_2)$ OUTPUT

$Q_2(Q_1)$ OUTPUT



Pulse generator (S-input): $t_r = 350$ ns; $t_f = 120$ ns; $t_{SL} = 700$ ns; $V_{pd} = +4, 5$ V



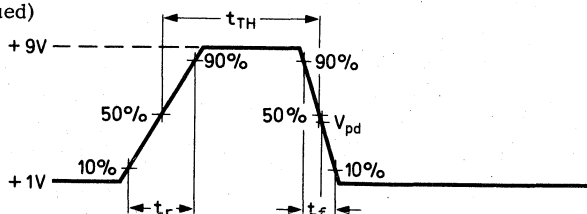
Measuring conditions: $V_p = +12$ V; $+15$ V
 $C_L = 10$ pF (including probe and jig capacitance)
 $T_{amb} = 25$ °C
 All other inputs are floating.

Waveforms illustrating conditions for set inputs. Set input signals are not supplied simultaneously.

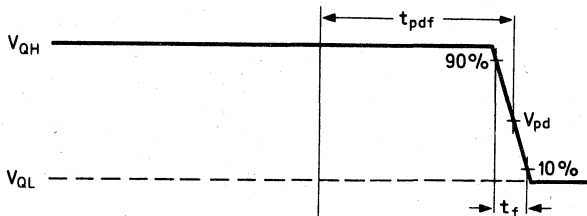
CHARACTERISTICS (continued)

Dynamic data

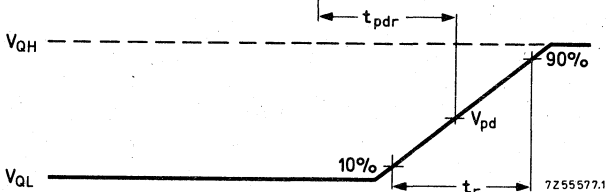
T INPUT



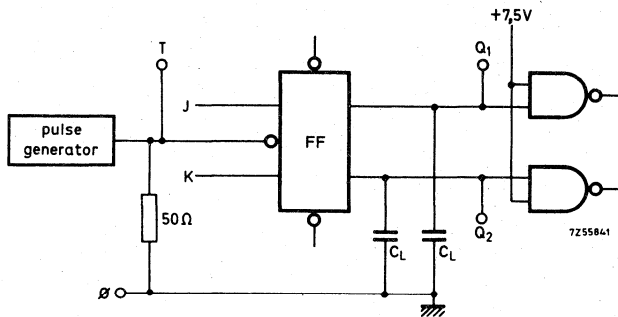
Q₁(Q₂) OUTPUT



Q₂(Q₁) OUTPUT



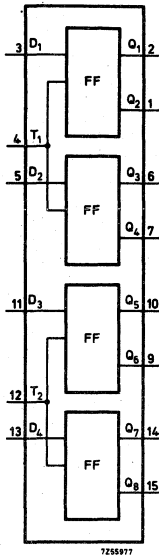
Pulse generator (T-input): $t_r = 350$ ns; $t_f = 120$ ns; $t_{TH} = 400$ ns; $V_{pd} = +4,5$ V



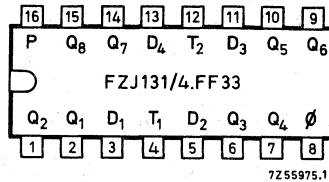
Measuring conditions: $V_p = +12$ V; $+15$ V
 $C_L = 10$ pF (including probe and jig capacitance)
 $T_{amb} = 25$ °C
 All other inputs are floating.

Waveforms and loading circuit illustrating measurement of t_{pdr} and t_{pdf} .

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.



QUADRUPLE D-TYPE LATCH FLIP-FLOP

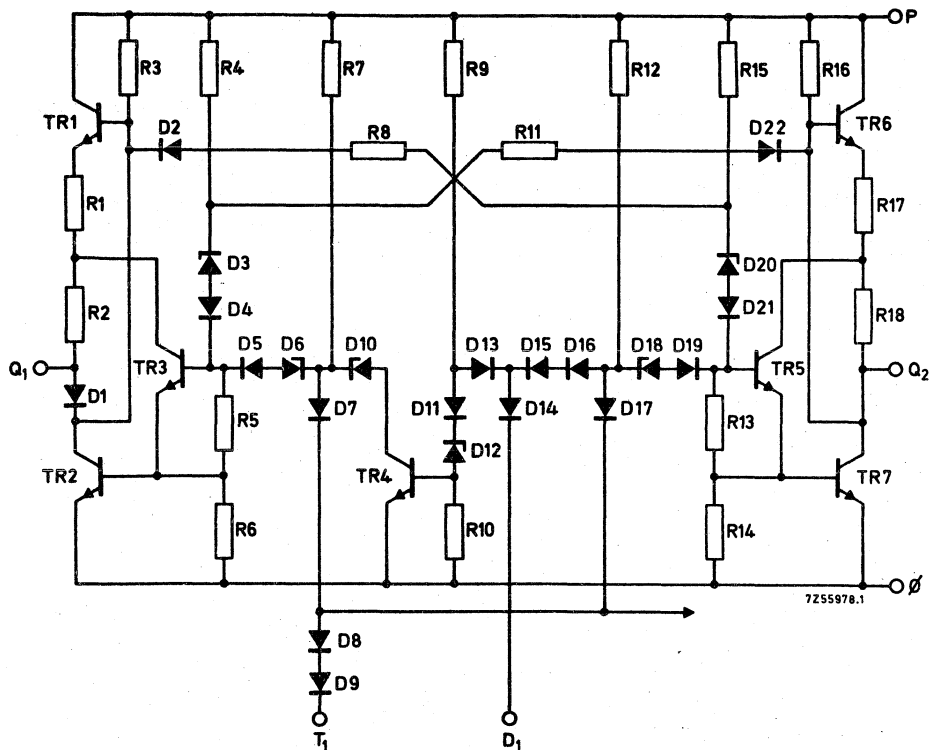


QUICK REFERENCE DATA

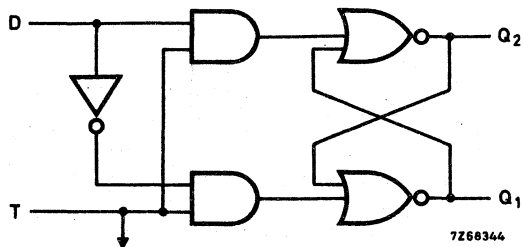
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d. c. fan-out } $T_{amb} = 0$ to +70 °C } LOW state	N_{aL}	max.	10	
Average supply current at $T_{amb} = 25$ °C				
$V_P = 13,5$ V	I_{Pav}	typ.	22	mA
$V_P = 17$ V	I_{Pav}	typ.	28	mA
D. C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II : $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Average power consumption				
(50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	264	mW
range II : $V_P = 15$ V	P_{av}	typ.	420	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC DIAGRAM



LOGIC FUNCTIONS

The FZJ131/4.FF33 comprises four D-type latch flip-flops. Information present at a data input D, is transferred to Q as long as T is HIGH. When T is LOW, D does not affect Q.

Function table

input		output
T	D (t_n)	Q (t_{n+1})
L	L	Q_n
L	H	Q_n
H	L	L
H	H	H

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

 t_n = bit-time before trigger pulse t_{n+1} = bit-time after trigger pulse**RATING** Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Output voltage	V_Q	max.	V_P
Input voltage	V_D, V_T	max.	18 V
Storage temperature	T_{stg}		-65 to +150 °C
Operating ambient temperature	T_{amb}		0 to +70 °C
Output short-circuit duration	t_{Qsc}	max.	1 s ¹⁾

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70 °C
Uniform system supply voltage (range I) (range II)	V_P		11,4 to 13,5 V
	V_P		13,5 to 17 V
Available d. c. fan-out	N_{aL}	max.	10
D. C. noise margin to all inputs: range I at V_{Pmin} range II at V_{Pmin}	M_L	min.	2,8 V
	M_H	min.	2,5 V
	M_L	min.	2,8 V
	M_H	min.	4,5 V
Power consumption (50% duty cycle) at range I : V_{Pmax} at range II : V_{Pmax}	P_{av}	max.	432 mW
	P_{av}	max.	720 mW
Supply current at range I : $V_P = 12$ V range II : $V_P = 15$ V	I_P	max.	32 mA
	I_P	max.	42 mA
Thermal resistance from system to ambient	R_{th}	max.	150 °C/W

1) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I ($V_p = 12\text{ V}$); $T_{\text{amb}} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.				Conditions and references	
						V_p (V)	
Static data							
<u>Voltages</u>							
Input HIGH: D, T	V_{IH}	7,5	-	-	V		
Input LOW: D, T	V_{IL}	-	-	4,5	V		
Output HIGH	V_{QH}	10	11,3	-	V	11,4	$\left\{ \begin{array}{l} V_I = 7,5\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	0,9	1,7	V	11,4	
<u>D. C. noise margin</u>							
HIGH	M_H	2,5	5,0	-	V	11,4	
LOW	M_L	2,8	5,0	-	V	11,4	
<u>Currents</u>							
Input HIGH: D, T	I_{IH}	-	-	1	μA	13,5	$V_{IH} = 13,5\text{ V}$ other inputs 0 V
Input LOW: D T	$-I_{DL}$	-	-	3	mA	13,5	$V_{DL} = 1,7\text{ V}$
	$-I_{TL}$	-	-	6	mA	13,5	$V_{TL} = 1,7\text{ V}$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4	$V_{QH} = 10\text{ V}$
Output LOW	I_{QL}	15	-	-	mA	11,4	$V_{QL} = 1,7\text{ V}$
Output short- circuited	$-I_{Qsc}$	9	15	25	mA	13,5	$V_I = 0; V_Q = 0$
<u>Supply data</u>							
Supply current	I_p	-	22	32	mA	13,5	$V_I = 0$

1) All typ. values under test conditions: $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ and $V_p = 12\text{ V}$.

CHARACTERISTICS (continued)

Test conditions: at range I ($V_p = 12$ V); $T_{amb} = 0$ to $+70$ °C

	Symbol	min. typ. 1) max.				conditions and references
Dynamic data						
<u>Times</u>						
Propagation delay:						
$T_1 \rightarrow Q_1$						$C_L = 10$ pF $N = 1$ $T_{amb} = 25$ °C $V_{pd} = 4, 5$ V
fall time	t_{pdf}	70	120	210	ns	
rise time	t_{pdr}	90	160	310	ns	
$T_1 \rightarrow Q_2$						
fall time	t_{pdf}	70	120	210	ns	
rise time	t_{pdr}	90	150	310	ns	
$D_1 \rightarrow Q_1$						
fall time	t_{pdf}	30	70	150	ns	
rise time	t_{pdr}	90	175	310	ns	
$D_1 \rightarrow Q_2$						
fall time	t_{pdf}	70	130	290	ns	
rise time	t_{pdr}	30	70	150	ns	
output fall time	t_f	15	35	60	ns	
output rise time	t_r	50	90	170	ns	
Clock rate (duty cycle 50%)	f_c	0, 5	-	-	MHz	
D input						
hold time	t_{holdH}	150	-	-	ns	
	t_{holdL}	50	-	-	ns	
set-up time	t_{suH}	300	-	-	ns	
	t_{suL}	500	-	-	ns	
T input	$(-dV/dt)_{Tmin}$		1		V/ μ s	

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_p = 12$ V.

CHARACTERISTICS (continued)

Test conditions: at range II ($V_P = 15\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.				Conditions and references	
						V_P (V)	
Static data							
<u>Voltages</u>							
Input HIGH: D, T	V_{IH}	7,5	-	-	V		
Input LOW: D, T	V_{IL}	-	-	4,5	V		
Output HIGH	V_{QH}	12	14,3	-	V	13,5	$\left\{ \begin{array}{l} V_I = 7,5\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	1,0	1,7	V	13,5	
D. C. noise margin							
HIGH	M_H	4,5	8,0	-	V	13,5	
LOW	M_L	2,8	5,0	-	V	13,5	
<u>Currents</u>							
Input HIGH: D, T	I_{IH}	-	-	1,0	μA	17	$V_{IH} = 17\text{ V}$ (other inputs 0 V)
Input LOW: D T	$-I_{DL}$	-	-	3,6	mA	17	$V_{DL} = 1,7\text{ V}$
	$-I_{TL}$	-	-	7,2	mA	17	$V_{TL} = 1,7\text{ V}$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5	$V_{QH} = 12\text{ V}$
Output LOW	I_{QL}	18	-	-	mA	13,5	$V_{QL} = 1,7\text{ V}$
Output short-circuited	$-I_{Qsc}$	9	15	25	mA	17	$V_I = 0; V_Q = 0$
Supply data							
Supply current	I_p	-	28	42	mA	17	$V_I = 0$

1) All typ. values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 15\text{ V}$.

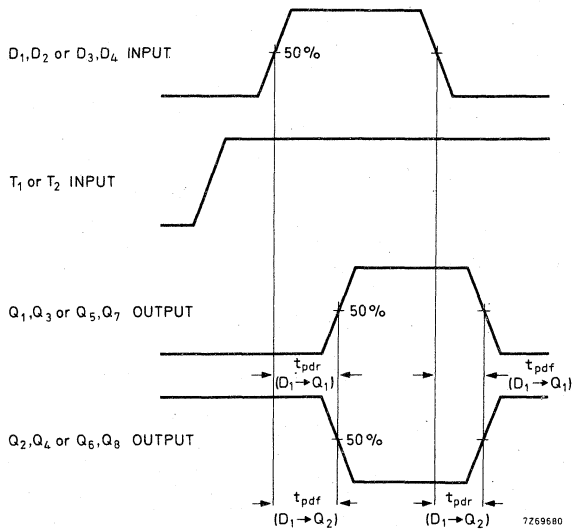
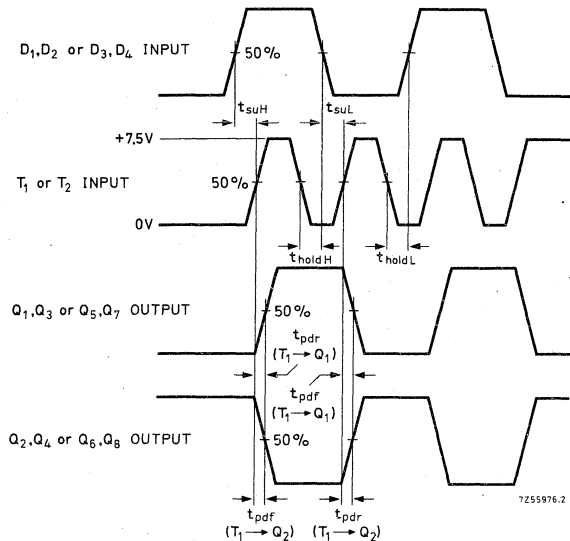
CHARACTERISTICS (continued)Test conditions: at range II ($V_p = 15\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Symbol	min. typ. ¹⁾ max	conditions and references
Dynamic data			
<u>Times</u>			
Propagation delay:			
$T_1 \rightarrow Q_1$			
fall time	t_{pdf}	} t. b. f.	} $C_L = 10\text{ pF}$ $N = 1$ $T_{amb} = 25\text{ }^\circ\text{C}$ $V_{pd} = 4,5\text{ V}$
rise time	t_{pdr}		
$T_1 \rightarrow Q_2$			
fall time	t_{pdf}		
rise time	t_{pdr}		
$D_1 \rightarrow Q_1$			
fall time	t_{pdf}		
rise time	t_{pdr}		
$D_1 \rightarrow Q_2$			
fall time	t_{pdf}		
rise time	t_{pdr}		
output fall time	t_f		
output rise time	t_r		
Clock rate (duty cycle 50%)	f_c		
D input hold time			
set-up time			
T input slope	$(-dV/dt)_{Tmin}$	- - 1 V/ μs	

1) All typ. values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_p = 15\text{ V}$.

CHARACTERISTICS (continued)

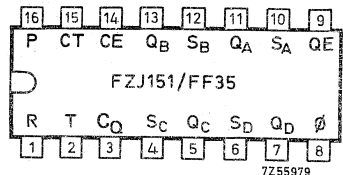
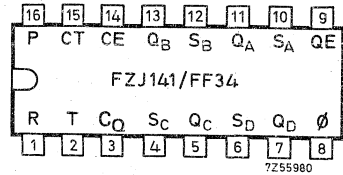
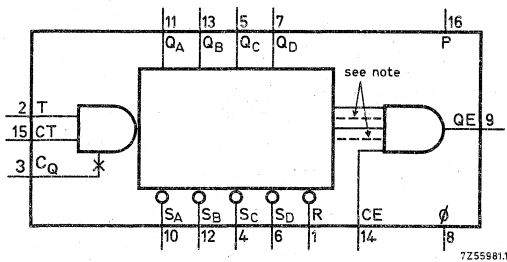
Dynamic data



Waveforms illustrating measurement of t_{pdr} and t_{pdf} ($T \rightarrow Q$): ($D \rightarrow Q$)

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SINGLE SYNCHRONOUS DECIMAL COUNTER
SINGLE SYNCHRONOUS 4-BIT BINARY COUNTER



Note

- FZJ141/FF34: without connections indicated by dotted line
- FZJ151/FF35: with connections indicated by dotted line

QUICK REFERENCE DATA			
Supply voltage (range I)	V _P	nom.	12 V
(range II)	V _P	nom.	15 V
Operating ambient temperature	T _{amb}		0 to +70 °C
Available d. c. fan-out } LOW state	N _{aL}	max.	10
Operating frequency at T _{amb} = 25 °C duty cycle 50%: range I/II	f _c	max.	1,5 MHz
Average supply current at T _{amb} = 25 °C	I _{Pav}	typ.	20 mA
V _P = 13,5 V at V _{QL}	I _{Pav}	typ.	23 mA
V _P = 17 V at V _{QL}			
D. C. noise margin at T _{amb} = 25 °C	M _L = M _H	typ.	5 V
range I : V _P = 12 V	{ M _L	typ.	5 V
range II : V _P = 15 V	{ M _H	typ.	8 V

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

GENERAL DESCRIPTION

The FZJ141/FF34 and FZJ151/FF35 are synchronous counters consisting of 4 master-slave flip-flops.

The FZJ141/FF34 is a decimal counter with common T and R input and a set (S) input for each bit. The condition input (CE) and output (QE) are for coupling these circuits.

The FZJ151/FF35 is a 4-bit binary counter with a common T and R input and a set input per bit. The direct reset inhibits the count and simultaneously all flip-flops return to LOW. The output information of each flip-flop of both circuits changes when T goes from HIGH to LOW.

LOGIC FUNCTIONS

Count condition: $S_A = S_B = S_C = S_D = CT = CE = R = HIGH$

FZJ141/FF34

count	outputs				
	Q _A	Q _B	Q _C	Q _D	QE
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	H

FZJ151/FF35

count	outputs				
	Q _A	Q _B	Q _C	Q _D	QE
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	L
10	L	H	L	H	L
11	H	H	L	H	L
12	L	L	H	H	L
13	H	L	H	H	L
14	L	H	H	H	L
15	H	H	H	H	H

Pin description

CT = condition enable trigger at input T

CE = condition enable for output QE

QE = output enable

Set and reset conditions

inputs					outputs			
R	S _A	S _B	S _C	S _D	Q _A	Q _B	Q _C	Q _D
L	H	H	H	H	L	L	L	L
L	L	X	X	X	H	X	X	X
L	X	L	X	X	X	H	X	X
L	X	X	L	X	X	X	H	X
L	X	X	X	L	X	X	X	H

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

All set and reset inputs, when LOW, override the count input signal and set the flip-flops corresponding to the table at the left.

Set and reset terminals may not be left floating but must be connected to the supply voltage V_p.

LOGIC FUNCTIONS (continued)

Enable conditions

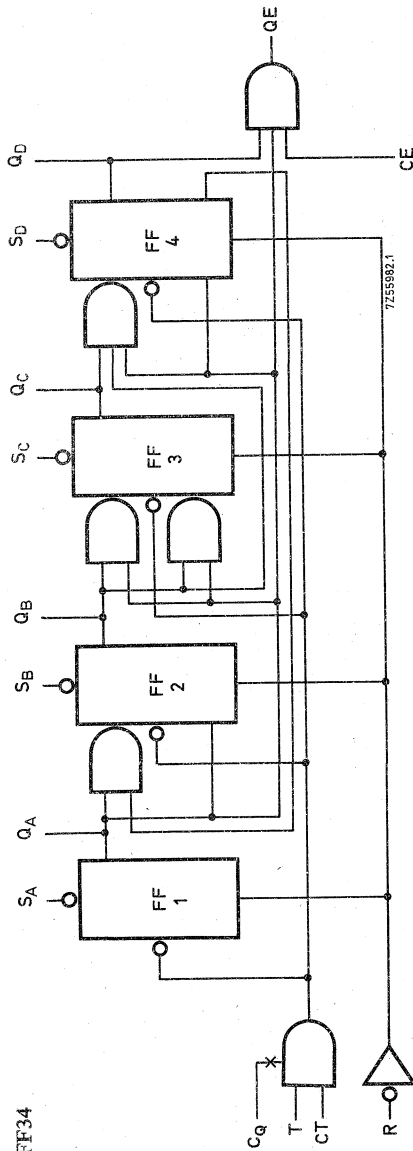
input CT		input CE	enable output QE
L	no count count	L	L
H		H	X*)

*) Depends on logic state of other inputs of the final gate.

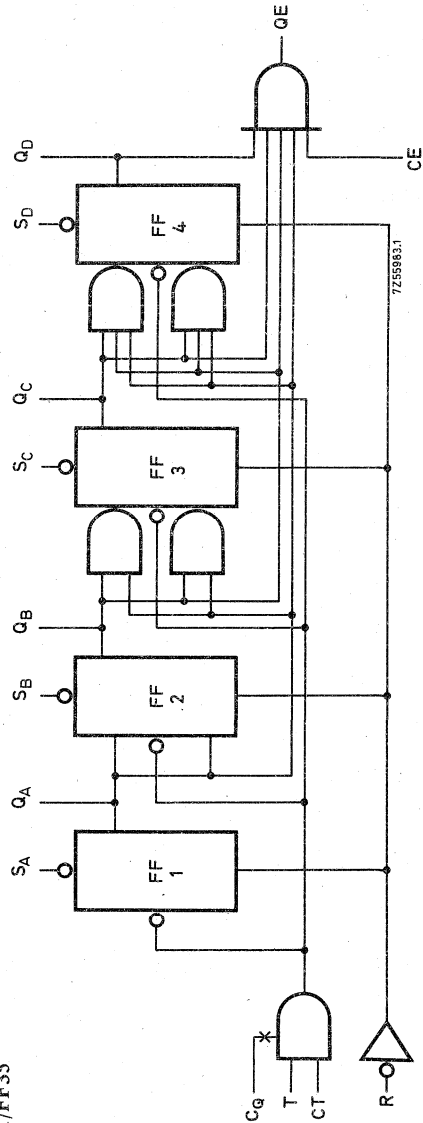
RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_I	max.	18	V
Input current at $V_P = 17$ V	$-I_{IL}$	max.	25	mA
Storage temperature	T_{stg}		-65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

LOGIC DIAGRAMS
FZJ141/FF34



FZJ151/FF35



SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70	°C
Uniform system supply voltage (range I) (range II)	V_P	11, 4 to 13, 5	V
	V_P	13, 5 to 17	V
Available d.c. fan-out	N_{aL}	max. 10	
D.C. noise margin to all inputs: range I at V_{Pmin}	$\left\{ \begin{array}{l} M_L \\ M_H \end{array} \right.$	min. 2, 8	V
		min. 2, 5	V
range II at V_{Pmin}	$\left\{ \begin{array}{l} M_L \\ M_H \end{array} \right.$	min. 2, 8	V
		min. 4, 5	V
Clock rate at $T_{amb} = 25$ °C duty cycle 50%; range I/II	f_c	min. 0, 5	MHz
	f_c	typ. 1, 5	MHz
Supply current at range I : $V_P = 12$ V at V_{QH} at V_{QL}	I_P	typ. 12	mA
	I_P	typ. 20	mA
at range II : $V_P = 15$ V at V_{QH} at V_{QL}	I_P	typ. 15	mA
	I_P	typ. 23	mA
Thermal resistance from system to ambient	R_{th}	max. 150	°C/W

CHARACTERISTICS Test conditions: at range I ($V_P = 12 \text{ V}$); $T_{amb} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{IH}	7,5	-	-	V	11,4
Input LOW	V_{IL}	-	-	4,5	V	13,5
Output HIGH	V_{QH}	10	11,3	-	V	11,4
Output LOW	V_{QL}	-	0,9	1,7	V	11,4
D. C. noise margin: HIGH LOW	M_H	2,5	5,0	-	V	11,4
	M_L	2,8	5,0	-	V	11,4
<u>Currents</u>						
Input HIGH	I_{IH}	-	-	1	μA	13,5
Input LOW	$-I_{IL}$	-	0,8	1,5	mA	13,5
Output HIGH	$-I_{QH}$	0,1	-	-	mA	11,4 and 13,5
Output LOW	I_{QL}	15	-	-	mA	11,4
Output short-circuited	$-I_{Qsc}$	9	15	25	mA	13,5
Supply data						
Supply current at V_{QH}	I_P	-	12	-	mA	13,5
at V_{QL}	I_P	-	20	-	mA	13,5

1) All typical values under test conditions: $T_{amb} = 25 \text{ }^\circ\text{C}$ and $V_P = 12 \text{ V}$.

CHARACTERISTICS (continued)

Test conditions: at range I ($V_p = 12\text{ V}$)

	Sym- bol	min. typ. ¹⁾ max.				Conditions and references
Dynamic data						
<u>Times</u>						
Propagation delay:						
T → QA; QB; QC; QD						
fall time	t _{pdf}	90	200	450	ns	$V_{pd} = 4,5\text{ V}$ $N = 1$ $C_L = 10\text{ pF}$ $T_{amb} = 25\text{ °C}$
rise time	t _{pdr}	90	200	450	ns	
T → QE						
fall time	t _{pdf}	150	300	500	ns	
rise time	t _{pdr}	200	400	700	ns	
CE → QE						
fall time	t _{pdf}	25	60	200	ns	
rise time	t _{pdr}	90	200	450	ns	
R → QA; QB; QC; QD						
fall time	t _{pdf}	70	150	310	ns	
SA → QA; SB → QB; SC → QC; SD → QD						
rise time	t _{pdr}	30	120	210	ns	
Clock pulse duration	t _T	0,5	-	-	μs	$V_{pd} = 4,5\text{ V}; N = 1$ duty cycle 50%
Clock rate	f _c	0,5	-	-	MHz	
Reset pulse duration	t _{RL}	0,5	-	-	μs	$V_{pd} = 4,5\text{ V}$ $N = 1$ $T_{amb} = 25\text{ °C}$
Reset recovery time (T input)	t _{Rrec}	-	-	2	μs	
Reset pulse duration during set operation	t _{RLS}	1	-	-	μs	
Set inputs (SA; SB; SC; SD) set-up time	t _{su}	1	-	-	μs	
Set inputs (SA; SB; SC; SD) hold time	t _{hold}	1	-	-	μs	
Output fall time } at Q	t _f	5	20	60	ns	
Output rise time } at Q	t _r	90	250	450	ns	
Output fall time } at QE	t _f	30	60	210	ns	
Output rise time } at QE	t _r	70	140	310	ns	
T input slope	(-dV/dt) _{Tmin}		1		V/μs	

¹⁾ All typical values under test conditions: $T_{amb} = 25\text{ °C}$ and $V_p = 12\text{ V}$.

CHARACTERISTICS (continued)

Test conditions: at range II ($V_P = 15 \text{ V}$); $T_{\text{amb}} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references		
					V_P (V)		
Static data							
<u>Voltages</u>							
Input HIGH	V_{IH}	7,5	-	-	V	13,5	
Input LOW	V_{IL}	-	-	4,5	V	17,0	
Output HIGH	V_{QH}	12	14,3	-	V	13,5	$\left. \begin{array}{l} V_{IL} = 4,5 \text{ V} \\ -I_{QH} = 0,1 \text{ mA} \end{array} \right\}$
Output LOW	V_{QL}	-	1	1,7	V	13,5	$\left. \begin{array}{l} V_{IH} = 7,5 \text{ V} \\ I_{QL} = 18 \text{ mA} \end{array} \right\}$
D. C. noise margin: HIGH LOW	M_H	4,5	8	-	V	13,5	
	M_L	2,8	5	-	V	13,5	
<u>Currents</u>							
Input HIGH	I_{IH}	-	-	1	μA	17,0	$V_I = 17,0 \text{ V}$
Input LOW	$-I_{IL}$	-	1,0	1,8	mA	17,0	$V_I = 1,7 \text{ V}$
Output HIGH	$-I_{QH}$	0,1	-	-	mA	13,5	$V_{QH} = 12 \text{ V}$
Output LOW	I_{QL}	18	-	-	mA	13,5	$V_{QL} = 1,7 \text{ V}$
Output short-circuited	$-I_{Qsc}$	9	15	25	mA	17,0	$V_I = 0; V_Q = 0$
Supply data							
Supply current at V_{QH}	I_P	-	15	23	mA	17,0	$V_I = 17,0 \text{ V}$
at V_{QL}	I_P	-	23	36,5	mA	17,0	$\left. \begin{array}{l} V_R = 0 \text{ V} \\ \text{other inputs } 17,0 \text{ V} \end{array} \right\}$

1) All typical values under test conditions: $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ and $V_P = 15 \text{ V}$.

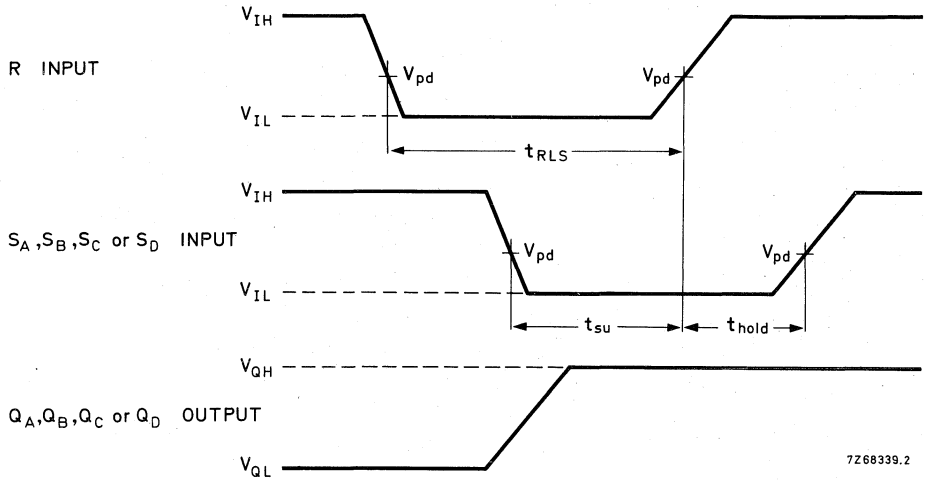
CHARACTERISTICS (continued)

Test conditions: at range II ($V_p = 15 \text{ V}$); $T_{amb} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.	Conditions and references
Dynamic data			
<u>Times</u>			
Propagation delay:			
T → Q			$C_L = 10 \text{ pF}$ $N = 1$ $T_{amb} = 25 \text{ }^\circ\text{C}$ $V_{pd} = 4,5 \text{ V}$
fall time	t_{pdf}	ns	
rise time	t_{pdr}	ns	
T → QE			
fall time	t_{pdf}	ns	
rise time	t_{pdr}	ns	
$C_E \rightarrow QE$			
fall time	t_{pdf}	ns	
rise time	t_{pdr}	ns	
R → Q			
fall time	t_{pdf}	t. b. f. ns	
$S_A \rightarrow Q_A, S_B \rightarrow Q_B$			
rise time	t_{pdr}	ns	
$S_C \rightarrow Q_C, S_D \rightarrow Q_D$			
fall time	t_{pdf}	ns	
output fall time } at Q	t_f	ns	
output rise time } at Q	t_r	ns	
output fall time } at QE			
output rise time } at QE			
T input slope	$(-dV/dt)_{Tmin}$	1 V/ μs	

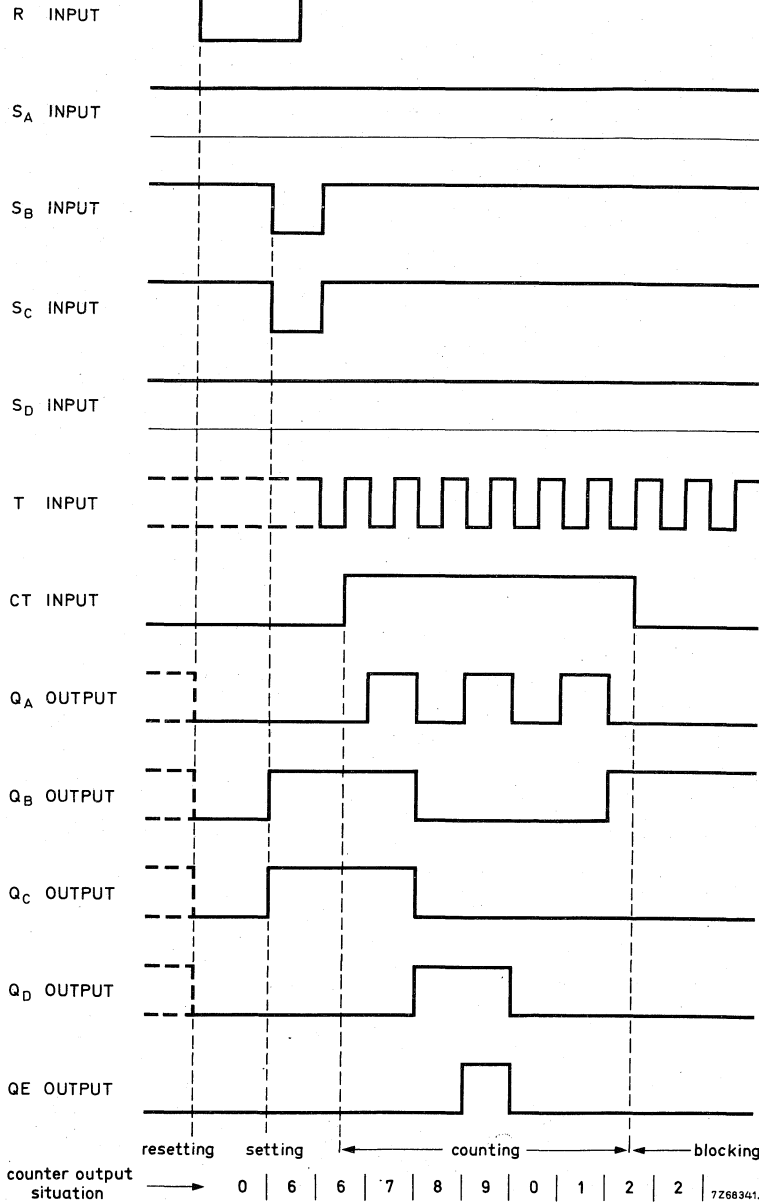
¹⁾ All typical values under test conditions: $T_{amb} = 25 \text{ }^\circ\text{C}$ and $V_p = 15 \text{ V}$.

CHARACTERISTIC (continued)



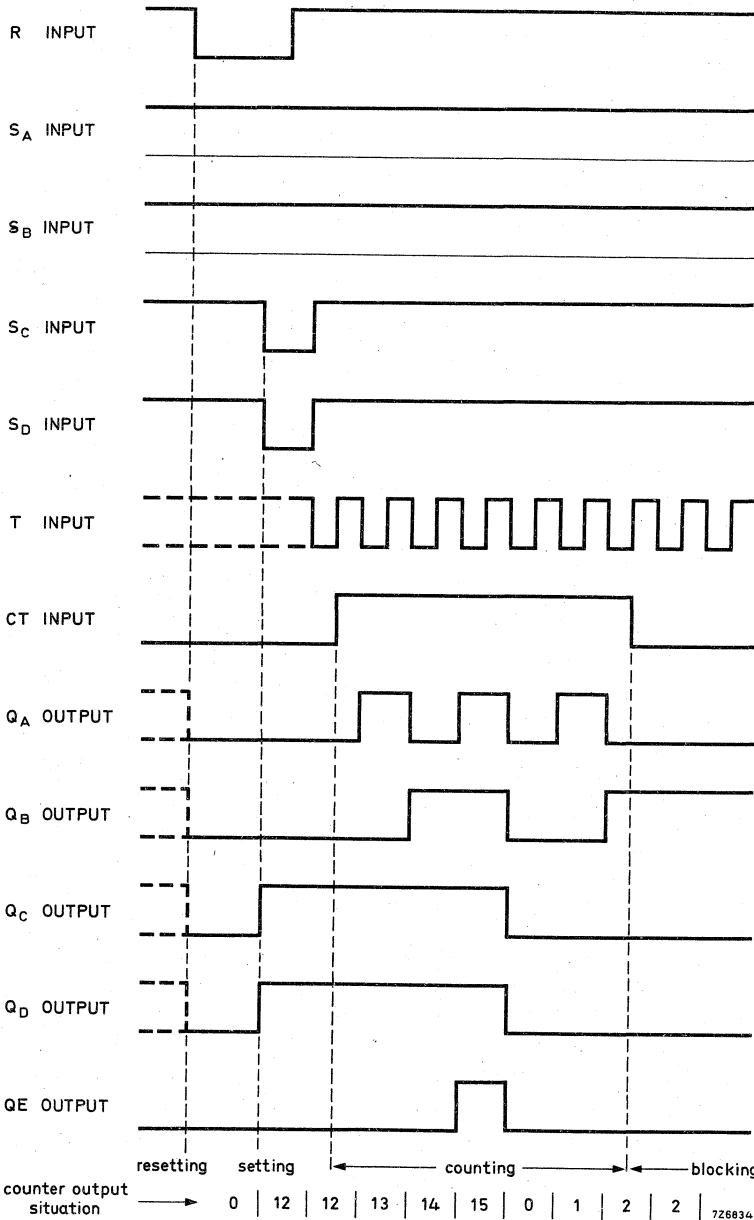
CHARACTERISTICS (continued)

FZJ141/FF34



CHARACTERISTICS (continued)

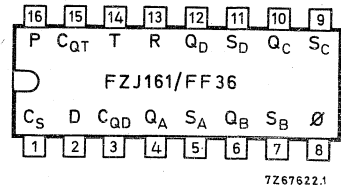
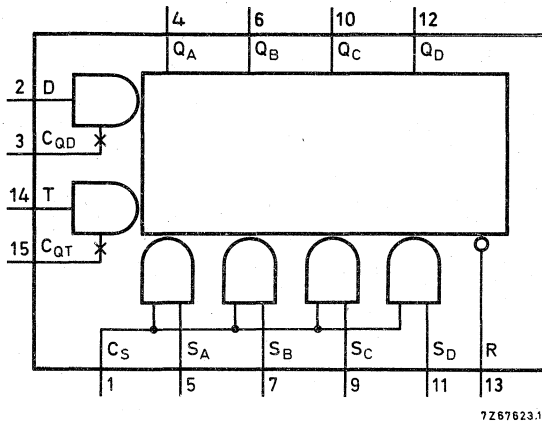
FZJ151/FF35



The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SINGLE SYNCHRONOUS 4-BIT SHIFT REGISTER

with slow-down capability



QUICK REFERENCE DATA

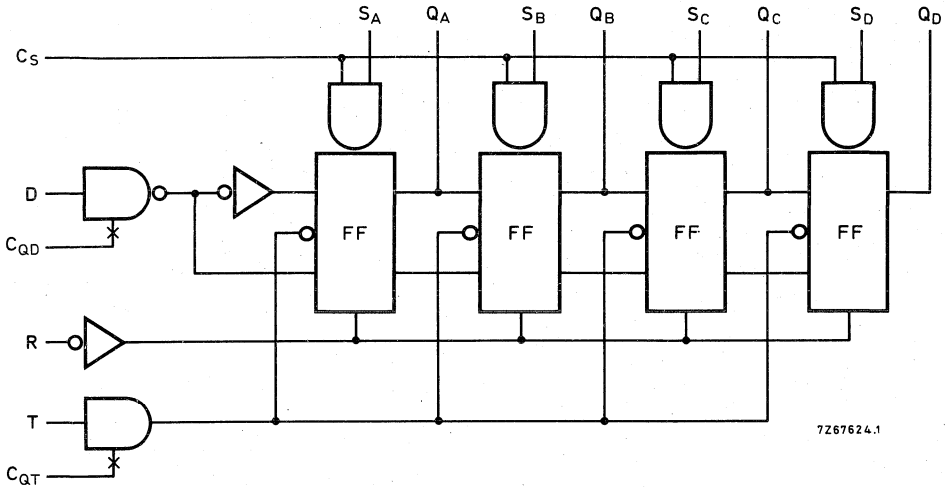
Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Available d. c. fan-out } LOW state $T_{amb} = 0$ to +70 °C	N_{aL}	max.	10	
Average supply current at $T_{amb} = 25$ °C				
$V_P = 13,5$ V	I_{Pav}	typ.	21	mA
$V_P = 17$ V	I_{Pav}	typ.	26	mA
D. C. noise margin at $T_{amb} = 25$ °C				
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5	V
range II : $V_P = 15$ V	M_L	typ.	5	V
	M_H	typ.	8	V
Average power consumption				
(50% duty cycle) range I : $V_P = 12$ V	P_{av}	typ.	180	mW
range II : $V_P = 15$ V	P_{av}	typ.	390	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

GENERAL DESCRIPTION

The FZJ161/FF36 consists of a synchronous 4-bit shift register with serial or parallel inputs and serial or parallel outputs. It is used as serial to parallel or parallel to serial converter, register and memory. The device has slow-down inputs (C_{QD} and C_{QT}).

LOGIC DIAGRAM



Pin description

- C_S = condition set input
- D = data input
- C_{QD} = slow-down data input
- R = reset input
- T = trigger input
- C_{QT} = slow-down trigger input
- S = set input
- Q = output

FUNCTION TABLE

inputs						outputs			
C _S	R	S _A	S _B	S _C	S _D	Q _A	Q _B	Q _C	Q _D
L	L	X	X	X	X	L	L	L	L
H	L	H	L	H	H	H	L	H	H
L	H	X	X	X	X	shift			

H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_I	max.	18	V
Input current at $V_P = 17$ V	$-I_{IL}$	max.	25	mA
Storage temperature	T_{stg}		-65 to +150	$^{\circ}\text{C}$
Operating ambient temperature	T_{amb}		0 to +70	$^{\circ}\text{C}$
Output short-circuit duration	t_{Qsc}	max.	1	s 1)

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70	$^{\circ}\text{C}$
Uniform system supply voltage (range I) (range II)	V_P		11, 4 to 13, 5	V
	V_P		13, 5 to 17	V
Available d. c. fan-out	N_{aL}	max.	10	
D. C. noise margin to all inputs: range I at V_{Pmin} range II at V_{Pmin}	{ M_L	min.	2, 8	V
		{ M_H	min.	2, 5
	{ M_L	min.	2, 8	V
		{ M_H	min.	4, 5
Power consumption (50% duty cycle) at range I : V_{Pmax} at range II : V_{Pmax}	P_{av}	max.	340	mW
	P_{av}	max.	715	mW
Supply current at range I : $V_P = 12$ V range II : $V_P = 15$ V	I_P	max.	33	mA
	I_P	max.	42	mA
Thermal resistance from system to ambient	R_{th}	max.	150	$^{\circ}\text{C}/\text{W}$

1) Only one output may be shorted at a time.

CHARACTERISTICS Test conditions: at range I ($V_P = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{IH}	7,5	-	- V	11,4	
Input LOW	V_{IL}	-	-	4,5 V	11,4 and 13,5	
Output HIGH	V_{QH}	10	11,3	- V	11,4	$\left\{ \begin{array}{l} V_{IL} = 4,5\text{ V} \\ -I_{QH} = 0,1\text{ mA} \end{array} \right.$
Output LOW	V_{QL}	-	0,9	1,7 V	11,4	$\left\{ \begin{array}{l} V_{IH} = 7,5\text{ V} \\ I_{QL} = 15\text{ mA} \end{array} \right.$
D.C. noise margin : HIGH	M_H	2,5	5,0	- V	11,4	
LOW	M_L	2,8	5,0	- V	11,4	
<u>Currents</u>						
Input HIGH	I_{IH}	-	-	1 μA	13,5	$V_{IH} = 13,5\text{ V}$
Input LOW						
CS-input	$-I_{CSL}$	-	-	6 mA	13,5	$V_{IL} = 1,7\text{ V}$
other inputs	$-I_{IL}$	-	-	1,5 mA	13,5	$V_{IL} = 1,7\text{ V}$
Output short-circuited ²⁾	$-I_{Qsc}$	9	15	25 mA	13,5	$V_I = 0; V_Q = 0$
Supply data						
Supply current	I_P	-	21	33 mA	13,5	$V_I = 0$

1) All typ. values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

2) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Test conditions: at range I ($V_p = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$.

	Sym- bol	min. typ. 1) max.			Conditions and references
Dynamic data					
<u>Times</u>					
Propagation delay:					
T → Q					
fall time	t_{pdf}	90	140	450	ns
rise time	t_{pdr}	90	140	450	ns
R → Q					
fall time	t_{pdf}	0,6	0,85	1,3	μs
$C_S \rightarrow Q, S_A \rightarrow Q_A, S_B \rightarrow Q_B,$					
$S_C \rightarrow Q_C, S_D \rightarrow Q_D$					
fall time	t_{pdf}	90	140	450	ns
rise time	t_{pdr}	100	240	500	ns
output fall time	t_f	5	20	60	ns
output rise time	t_r	70	150	290	ns
Clock pulse duration	t_T	0,5	-	-	μs
Clock rate	f_C	0,5	1,5	-	MHz
Reset pulse duration	t_{RL}	0,5	-	-	μs
Reset pulse duration during set operation	t_{RLS}	1	-	-	μs
Set-up times at					
$S_A; S_B; S_C; S_D; C_S$	t_{su}	1	-	-	μs
D	t_{su}	0	-	-	μs
Hold times at					
$S_A; S_B; S_C; S_D; C_S$	t_{hold}	1	-	-	μs
D	t_{hold}	0,5	-	-	μs
T input slope	$(-dV/dt)_{Tmin}$			1	V/ μs

1) All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_p = 12\text{ V}$.

CHARACTERISTICS (continued)Test conditions: at range II ($V_P = 15\text{ V}$); $T_{\text{amb}} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. 1) max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{IH}	7,5	-	-	V	13,5
Input LOW	V_{IL}	-	-	4,5	V	13,5 and 17,0
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5
Output LOW	V_{QL}	-	1,0	1,7	V	13,5
D.C. noise margin: HIGH	M_H	4,5	8,0	-	V	13,5
LOW	M_L	2,8	5,0	-	V	13,5
<u>Currents</u>						
Input HIGH	I_{IH}	-	-	1	μA	17,0
Input LOW						$V_I = 17,0\text{ V}$
CS-input	$-I_{CSL}$	-	-	7,2	mA	17,0
other inputs	$-I_{IL}$	-	-	1,8	mA	17,0
Output short-circuited 2)	I_{Qsc}	9	15	25	mA	17,0
Supply data						
Supply current	I_P	-	26	42	mA	17,0
						$V_I = 0$

1) All typ. values under test conditions: $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ and $V_P = 15\text{ V}$.

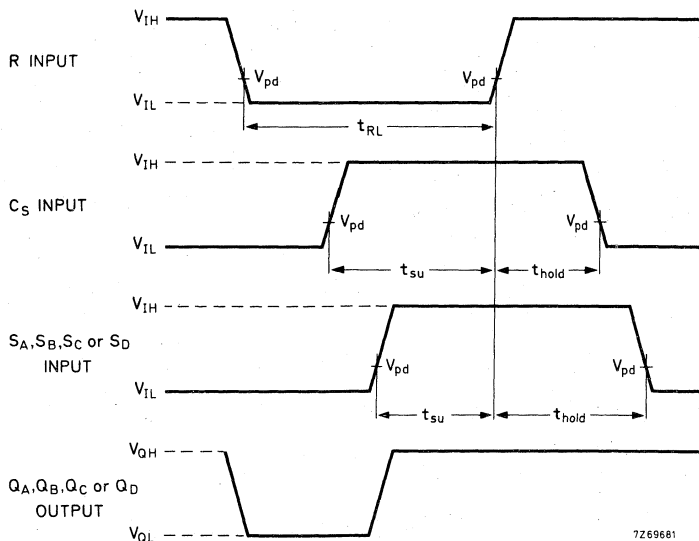
2) Short-circuit duration max. 1 s.

CHARACTERISTICS (continued)

Test conditions: at range II ($V_P = 15\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. 1) max.	Conditions and references
Dynamic data			
<u>Times</u>			
Propagation delay:			
T → Q			$C_L = 10\text{ pF}$ $N = 1$ $T_{amb} = 25\text{ }^\circ\text{C}$ $V_{pd} = 4,5\text{ V}$
fall time	t_{pdf}	ns	
rise time	t_{pdr}	ns	
R → Q			
fall time	t_{pdf}	μs	
$C_S \rightarrow Q, S_A \rightarrow Q_A, S_B \rightarrow Q_B,$ $S_C \rightarrow Q_C, S_D \rightarrow Q_D$		t. b. f.	
rise time	t_{pdr}	ns	
fall time	t_{pdf}	ns	
output fall time	t_f	ns	
output rise time	t_r	ns	
T input slope	$(-dV/dt)_{Tmin}$	1 V/ μs	

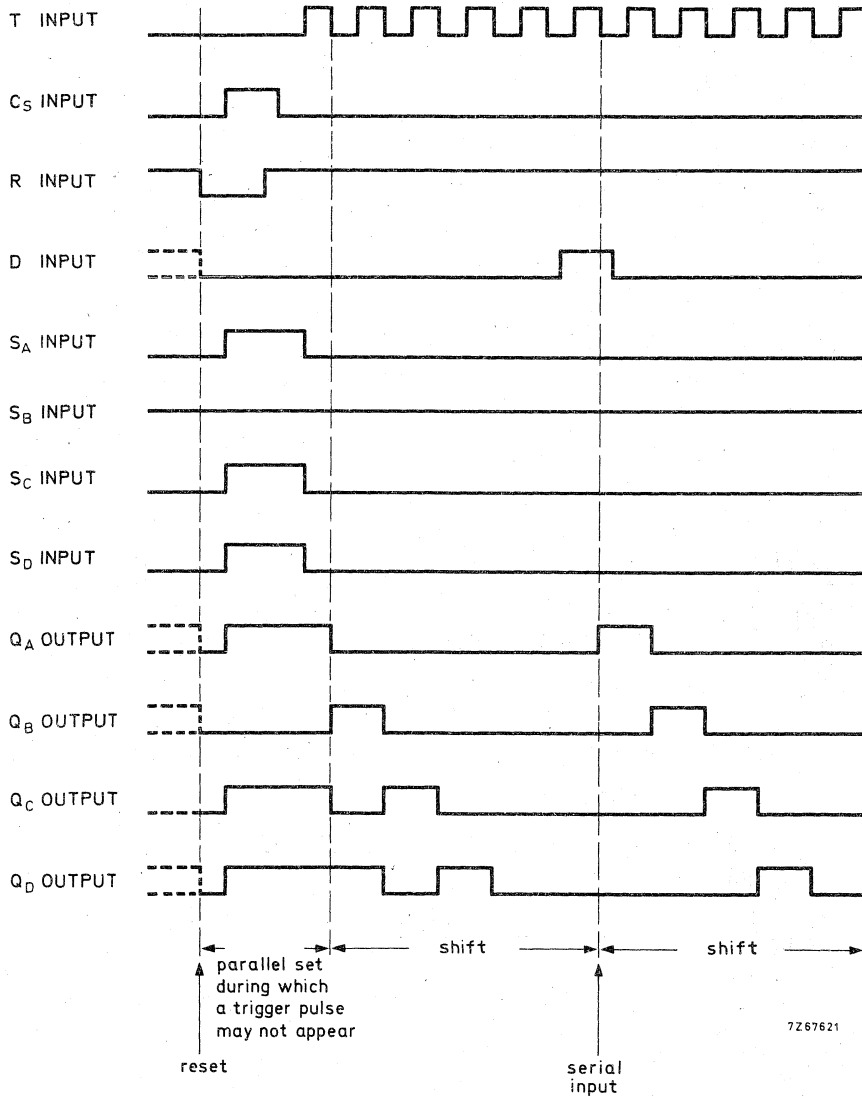
Waveforms for set operation



1) All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 15\text{ V}$.

CHARACTERISTICS (continued)

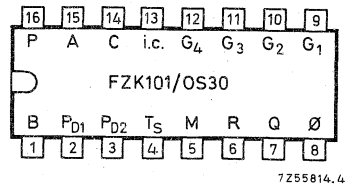
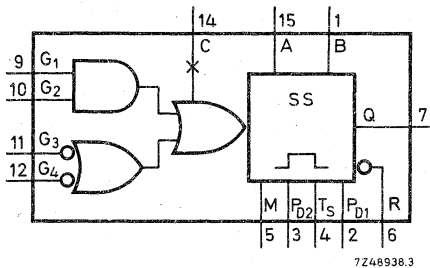
Dynamic data



The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

MONOSTABLE MULTIVIBRATOR

with slow-down capability

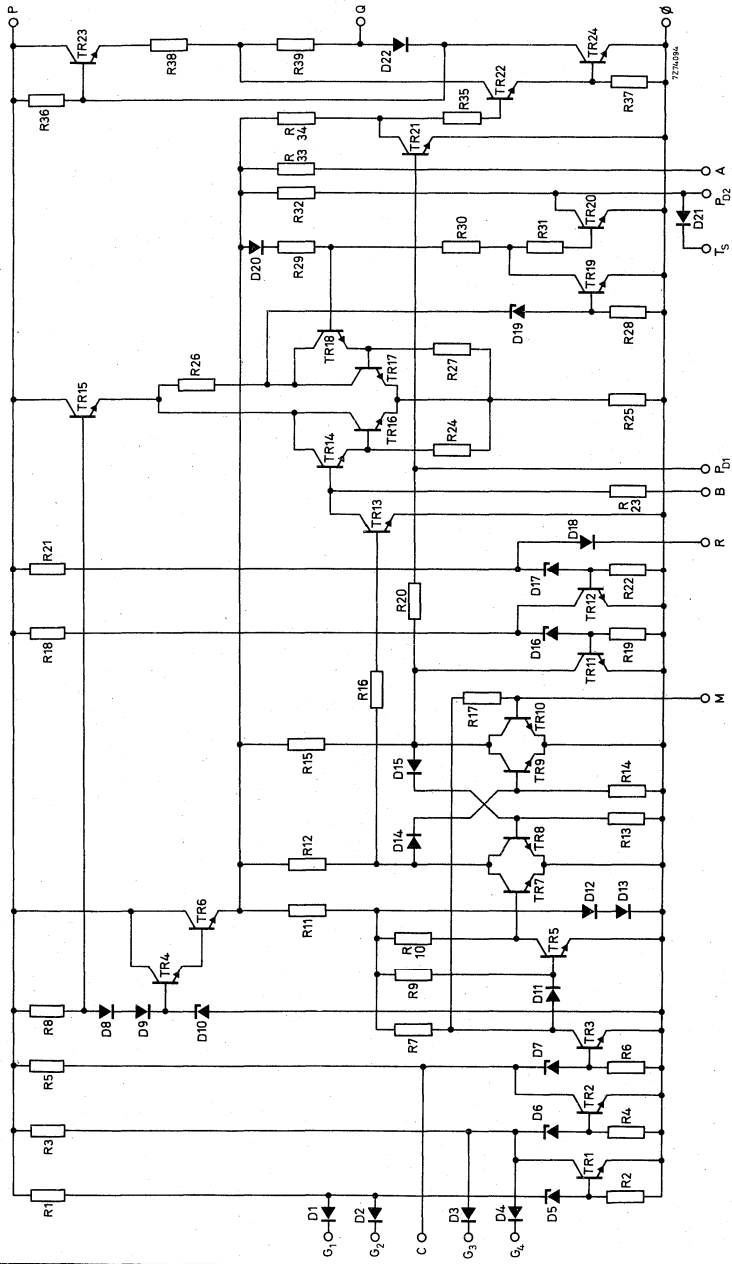


QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Average propagation delay: $T_{amb} = 25\text{ °C}; V_{pd} = 4, 5\text{ V}$ (ranges I and II)	t_{pdr}	typ.	270	ns
Available d. c. fan-out: LOW state	N_{aL}	max.	10	
D. C. noise margin at $T_{amb} = 25\text{ °C}$				
range I : $V_P = 12\text{ V}$	$M_L = M_H$	typ.	5	V
	M_L	typ.	5	V
range II : $V_P = 15\text{ V}$	M_H	typ.	8	V
Average power consumption				
(50% duty cycle) range I : $V_P = 12\text{ V}$	P_{av}	typ.	145	mW
range II: $V_P = 15\text{ V}$	P_{av}	typ.	180	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

CIRCUIT DIAGRAM



GENERAL DESCRIPTION

The FZK101/OS30 has the following electrical functions and properties.

If the FZK101/OS30 is used as :

- a. Monostable multivibrator: P_{D2} , T_S and M have to be interconnected
- b. Pulse delaying circuit : P_{D1} and P_{D2} have to be interconnected
- c. Pulse shortening circuit : T_S and M have to be interconnected.
- d. Delay switch : P_{D1} with P_{D2} and M with ϕ have to be interconnected.

The output-pulse duration and pulse-delaying duration depend upon a resistor R_t which is externally connected between A and B and a capacitor C_t between B and ϕ . Output pulse durations and propagation delay are very stable with temperature and supply voltage changes.

The LOW state of output Q can be obtained by a LOW signal at input R.

The noise immunity of the G-inputs will be increased by connecting a capacitor (max. 500 pF) between slow-down terminal C and ϕ .

To the terminals P_{D1} , P_{D2} , T_S and M no voltages or currents may be applied.

External interconnections between these terminals have to be as short as possible.

If input signals are applied to the inputs G_3 and G_4 , inputs G_1 and/or G_2 have to be LOW.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	18	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_G	max.	18	V
Voltage difference between any two inputs		max.	18	V
Storage temperature	T_{stg}		-65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C
Slow-down input voltage	$+V_C$	max.	0,6	V
	$-V_C$	max.	1,0	V
Slow-down input current	$+I_C$	max.	2,0	mA
	$-I_C$	max.	10,0	mA
Output short-circuit duration	t_{Qsc}	max.	1	s ¹⁾

1) Only one output may be shorted at a time.

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0	to	+70	$^{\circ}C$
Uniform system supply voltage (range I) (range II)	V_P	11,4	to	13,5	V
	V_P	13,5	to	17	V
D.C. noise margin; range I at V_{Pmin}	M_L	min.		2,8	V
	M_H	min.		2,5	V
range II at V_{Pmin}	M_L	min.		2,8	V
	M_H	min.		4,5	V
Supply current at range I; output HIGH	I_{Pav}	typ.		12	mA
	I_{Pav}	typ.		13	mA
output LOW	I_{Pav}	typ.		13	mA
	I_{Pav}	typ.		14	mA
at range II; output HIGH	I_{Pav}	typ.		14	mA
	I_{Pav}	typ.		15	mA
output LOW	I_{Pav}	typ.		15	mA
	I_{Pav}	typ.		15	mA
Power consumption (50% duty cycle) at range I = V_{Pmax}	P_{av}	max.		257	mW
	P_{av}	max.		391	mW
at range II = V_{Pmax}	P_{av}	max.		391	mW
Slow-down capacitor	C_M	max.		500	pF
Thermal resistance from system to ambient	R_{th}	max.		150	$^{\circ}C/W$

CHARACTERISTICS Test conditions: at range I ($V_P = 12\text{ V}$); $T_{\text{amb}} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym - bol	min. typ. ¹⁾ max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{GH}	7,5	-	-	V	11,4
Input LOW	V_{GL}	-	-	4,5	V	11,4 and 13,5
Output HIGH	V_{QH}	10,0	11,3	-	V	11,4 and 13,5
Output LOW	V_{QL}	-	0,9	1,7	V	11,4
D.C.noise margin: HIGH	M_H	2,5	5,0	-	V	11,4
LOW	M_L	2,8	5,0	-	V	11,4
<u>Currents (per input)</u>						
Input HIGH	I_{GH}	-	-	1,0	μA	13,5
Input LOW	$-I_{GL}$	-	0,8	1,5	mA	13,5
Output HIGH	$-I_{QH}$	-	-	0,1	mA	11,4 and 13,5
Output LOW	I_{QL}	15	-	-	mA	11,4
Output short-circuited	$-I_{Qsc}$	10	30	50	mA	13,5
Supply data						
<u>Currents</u>						
at V_{GL}	I_P	-	13,0	18,5	mA	13,5
at V_{GH}	I_P	-	12,0	17,0	mA	13,5

¹⁾ All typical values under test conditions: $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

CHARACTERISTICS (continued)

Test conditions: at range I ($V_P = 12$ V); $T_{amb} = 0$ to $+70$ °C

	symbol	min. typ. ¹⁾ max.				conditions and references
Dynamic data						
<u>Times</u>						
Propagation delay:						
G → Q						$C_L = 10$ pF $N = 1$ $T_{amb} = 25$ °C $V_{pd} = 4,5$ V $C_o = 10$ pF between B and ϕ $V_P = 11,4$ V $R_t = 0,5$ M Ω $C_t = 2$ nF see note 2
fall time	t_{pdf}	110	180	450	ns	
rise time	t_{pdr}	220	270	740	ns	
R → Q						
fall time	t_{pdf}	150	300	550	ns	
Output fall time	t_f	30	80	150	ns	
Output rise time	t_r	50	100	200	ns	
Input pulse duration	t_{GH}	0,5	-	-	μ s	
Reset pulse duration	t_{RL}	0,5	-	-	μ s	
Recovery time	t_{rec}	$(C_o + C_t) \times 10^3$			s/F	
Set-up time						
at G_1, G_2	t_{su}	0	-	-	μ s	
at G_3, G_4	t_{su}	0,5	-	-	μ s	
Output pulse duration ₁	t_{QHmin}	400			ns	
Output pulse duration	t_{QH}	650	700	780	μ s	
Capacitor	C_t	0	-	∞	μ F	
Resistor	R_t	5	-	500	k Ω	
Input slope, G_1, G_2	$(dV/dt)_T$	0,1			V/ μ s	
G_3, G_4		1			V/ μ s	

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_P = 12$ V.2) For higher accuracy $R_t = 40$ to 200 k Ω .

CHARACTERISTICS Test conditions: at range II ($V_P = 15 \text{ V}$); $T_{\text{amb}} = 0 \text{ to } +70 \text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{GH}	7,5	-	-	V	13,5 { $V_{QL} \leq 1,7 \text{ V}$ $I_{QL} = 18 \text{ mA}$
Input LOW	V_{GL}	-	-	4,5	V	13,5 and 17 { $V_{QH} \geq 12 \text{ V}$ $-I_{QH} = 0,1 \text{ mA}$
Output HIGH	V_{QH}	12,0	14,3	-	V	13,5 and 17 { $V_{GL} = 4,5 \text{ V}$ $-I_{QH} = 0,1 \text{ mA}$
Output LOW	V_{QL}	-	1,0	1,7	V	13,5 { $V_{GH} = 7,5 \text{ V}$ $I_{QL} = 18 \text{ mA}$
D. C. noise margin: HIGH	M_H	4,5	8,0	-	V	13,5
LOW	M_L	2,8	5,0	-	V	13,5
<u>Currents (per input)</u>						
Input HIGH	I_{GH}	-	-	1,0	μA	17 { $V_G = 17 \text{ V}$ other inputs 0 V
Input LOW	$-I_{GL}$	-	1,0	1,8	mA	17 { $V_{GL} = 1,7 \text{ V}$ other inputs 17V
Output HIGH	$-I_{QH}$	-	-	0,1	mA	13,5 and 17 { $V_{GL} = 4,5 \text{ V}$ $V_{QH} = 12 \text{ V}$
Output LOW	I_{QL}	18	-	-	mA	13,5 { $V_{GH} = 7,5 \text{ V}$ $V_{QL} = 1,7 \text{ V}$
Output short-circuited	$-I_{Qsc}$	15	37	50	mA	17 $V_G = 0 \text{ V}; V_Q = 0 \text{ V}$
Supply data						
<u>Currents</u>						
at V_{GH}	I_P	-	14,0	20,0	mA	17
at V_{GL}	I_P	-	15,0	21,5	mA	17

¹⁾ All typical values under test conditions: $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ and $V_P = 15 \text{ V}$.

CHARACTERISTICS (continued)

Test conditions: at range II ($V_P = 15\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

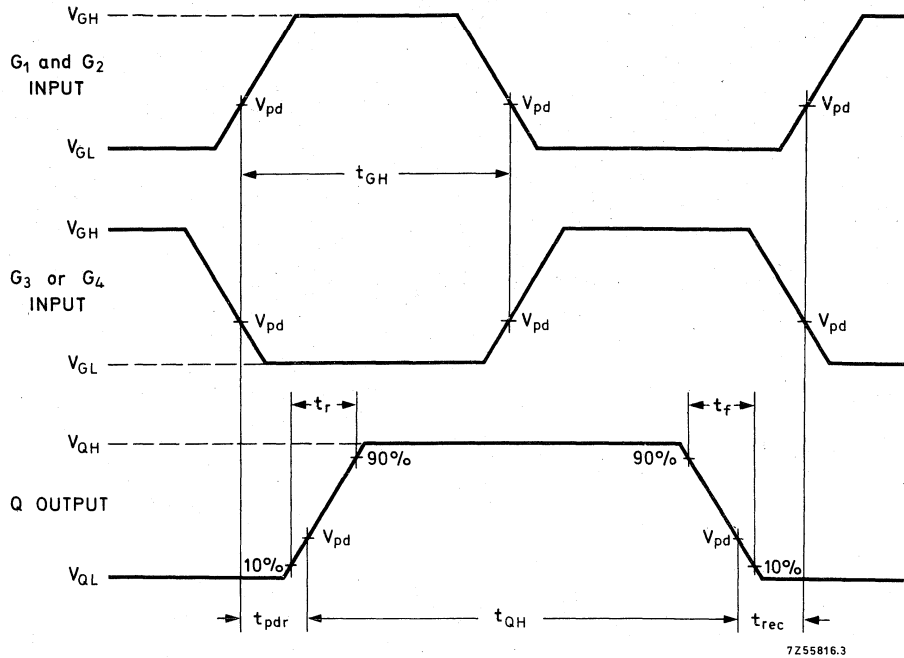
	symbol	min. typ. ¹⁾ max.	conditions and references	
Dynamic data				
<u>Times</u>				
Propagation delay:				
G → Q				
fall time	t_{pdf}	} t. b. f.	} $C_L = 10\text{ pF}$ $N = 1$ $T_{amb} = 25\text{ }^\circ\text{C}$ $V_{pd} = 4,5\text{ V}$	
rise time	t_{pdr}			ns
R → Q				
fall time	t_{pdf}			ns
Output fall time	t_f	ns		
Output rise time	t_r	ns		
Input pulse duration	t_{GH}	0,5 - - μs		} $C_o = 10\text{ pF}$ between B and ϕ
Reset pulse duration	t_{RL}	0,5 - - μs		
Recovery time	t_{rec}	$(C_o + C_t) \times 10^3\text{ s/F}$		
Set-up time				
at G_1, G_2	t_{su}	0 - - μs		
at G_3, G_4	t_{su}	0,5 - - μs		
Output pulse duration	t_{QHmin}	400 700 ns	} $V_P = 13,5\text{ V}$ $R_t = 0,5\text{ M}\Omega$ $C_t = 2\text{ nF}$	
Output pulse duration	t_{QH}	650 700 780 μs		
Capacitor	C_t	0 - $\infty\text{ }\mu\text{F}$	} see note 2	
Resistor	R_t	5 - 500 $\text{k}\Omega$		
Input slope, G_1, G_2	$(dV/dt)_T$	0,1	$\text{V}/\mu\text{s}$	
G_3, G_4		1	$\text{V}/\mu\text{s}$	

1) All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 15\text{ V}$.

2) For higher accuracy $R_t = 40\text{ to }200\text{ k}\Omega$.

CHARACTERISTICS (continued)**Dynamic data**

FZK101/OS30 used as monostable multivibrator

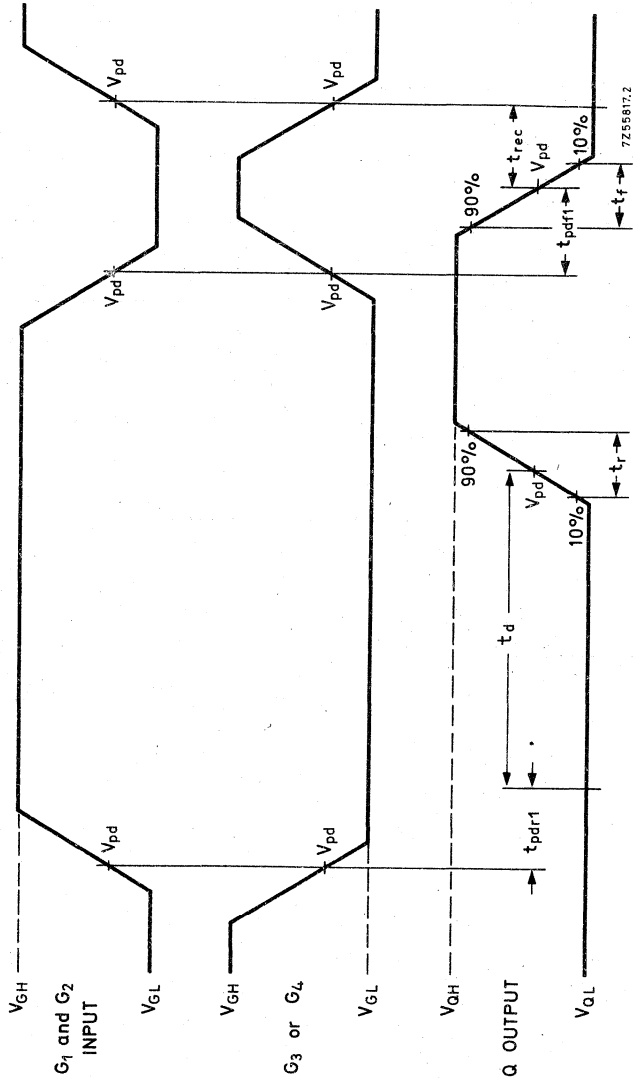
Conditions: P_{D2} and M interconnected

$$t_{QH} = 0,7 \times R_t (C_o + C_t)$$

CHARACTERISTICS (continued)

Dynamic data

FZK101/OS30 used as pulse delayed circuit

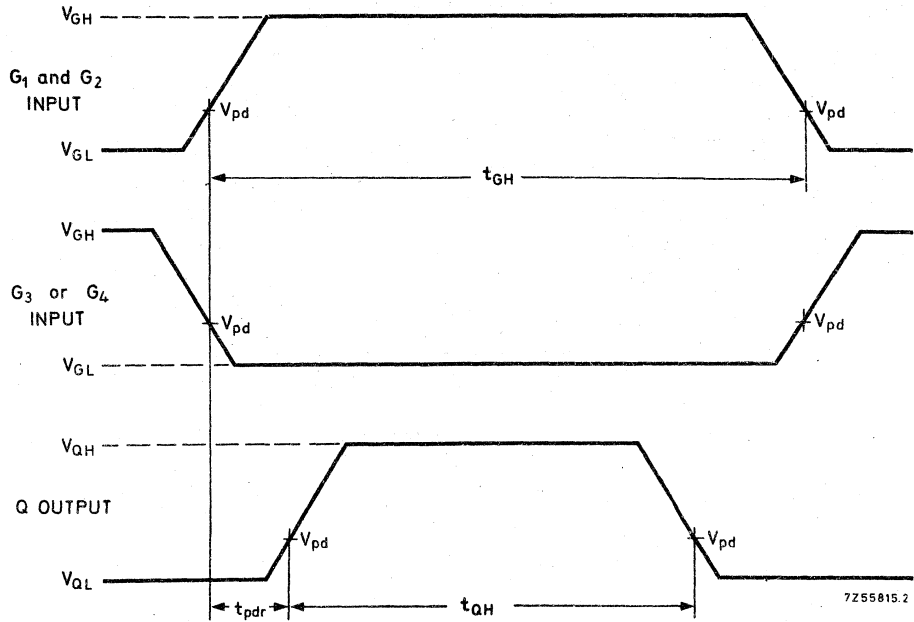


Conditions: P_{D1} and P_{D2} interconnected
 $t_d = 0.7 \times R_t (C_o + C_t)$

CHARACTERISTICS (continued)

Dynamic data

FZK101/OS30 used as pulse shortened circuit

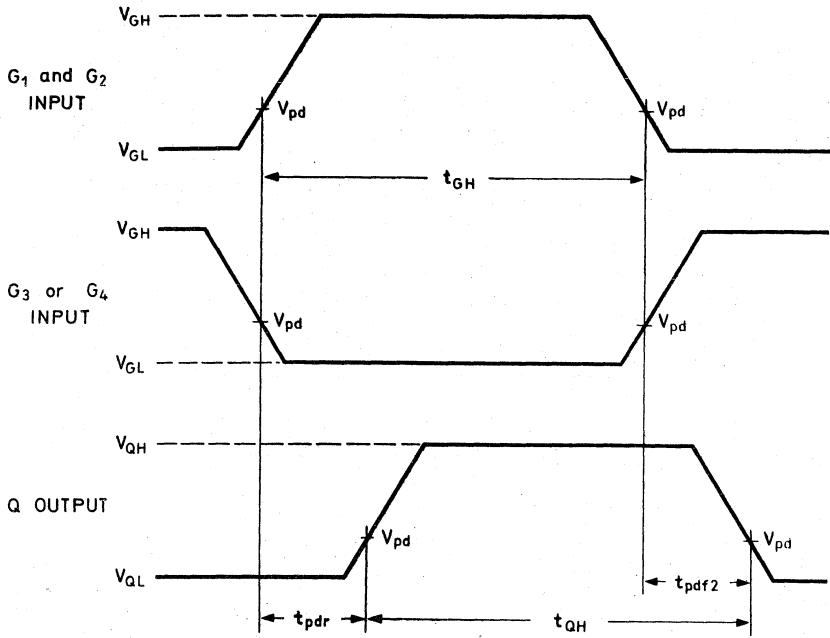


Conditions: T_S and M interconnected
 $t_{GH} > 0,7 \times R_t (C_o + C_t)$
 $t_{QH} = 0,7 \times R_t (C_o + C_t)$

CHARACTERISTICS (continued)

Dynamic data

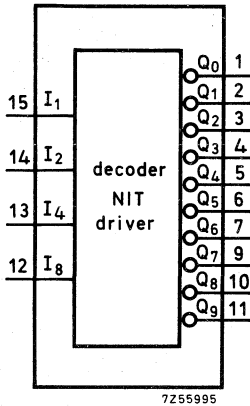
FZK 101/OS30 used as pulse shortened circuit



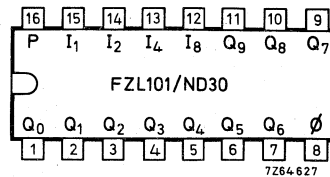
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Conditions: T_S and M interconnected
 $t_{GH} \leq 0,7 \times R_t (C_o + C_t)$
 $t_{QH} = t_{GH}$

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.



SINGLE BCD-DECIMAL DECODER N.I.T.¹⁾ DRIVER



QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12	V
(range II)	V_P	nom.	15	V
Operating ambient temperature	T_{amb}		0 to +70	°C
Output current (per output):				
output transistor in off-state	I_Q	max.	2	mA
output transistor in on-state	I_Q	max.	20	mA
Output voltage at any output (output transistor in cut-off)	V_Q	max.	80	V
Average supply current at $T_{amb} = 25\text{ °C}$				
$V_P = 13,5\text{ V}$	I_{Pav}	typ.	17	mA
$V_P = 17\text{ V}$	I_{Pav}	typ.	18	mA
D. C. noise margin at $T_{amb} = 25\text{ °C}$				
range I : $V_P = 12\text{ V}$	} M_L	typ.	5,5	V
		} M_H	typ.	4,5
range II : $V_P = 15\text{ V}$	} M_L	typ.	5,5	V
		} M_H	typ.	7,5
Average power consumption				
(50% duty cycle) range I : $V_P = 12\text{ V}$	P_{av}	typ.	205	mW
range II : $V_P = 15\text{ V}$	P_{av}	typ.	270	mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section).

¹⁾ N.I.T. = numerical indicator tube.

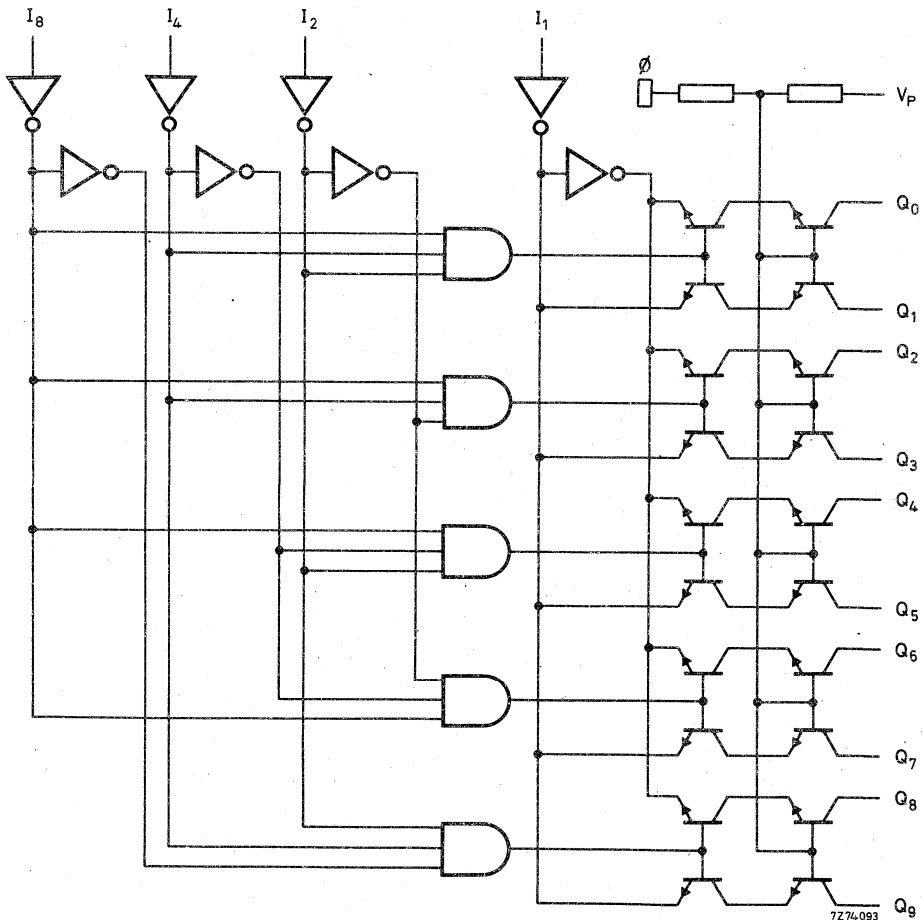
GENERAL DESCRIPTION

The FZL101/ND30 is a BCD (1-2-4-8 code) to decimal decoder incorporating high voltage output transistors for driving numerical indicator tubes.

Note

When used as HNIL decoder for every output a 10 kΩ resistor, connected to V_P, is required. At the outputs hazard pulses can appear during transition stages.

LOGIC DIAGRAM



FUNCTION TABLE

inputs				outputs (on-state = L)										
I ₁	I ₂	I ₄	I ₈	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇	Q ₈	Q ₉	
L	L	L	L	L	H	H	H	H	H	H	H	H	H	
H	L	L	L	H	L	H	H	H	H	H	H	H	H	
L	H	L	L	H	H	L	H	H	H	H	H	H	H	
H	H	L	L	H	H	H	L	H	H	H	H	H	H	
L	L	H	L	H	H	H	H	L	H	H	H	H	H	
H	L	H	L	H	H	H	H	H	L	H	H	H	H	
L	H	H	L	H	H	H	H	H	H	L	H	H	H	
H	H	H	L	H	H	H	H	H	H	H	L	H	H	
L	L	L	H	H	H	H	H	H	H	H	H	L	H	
H	L	L	H	H	H	H	H	H	H	H	H	H	L	
L	H	L	H	H	H	H	H	H	H	H	H	H	H	
H	H	L	H	H	H	H	H	H	H	H	H	H	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	H	
H	L	H	H	H	H	H	H	H	H	H	H	H	H	
L	H	H	H	H	H	H	H	H	H	H	H	H	H	
H	H	H	H	H	H	H	H	H	H	H	H	H	H	

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V _p	max.	18	V
Output voltage (at any output)	V _Q	max.	80	V
Input voltage	V _I	max.	18	V
Current into any output (off-state)	I _Q	max.	2	mA
Current into any output (on-state)	I _Q	max.	20	mA
Storage temperature	T _{stg}		-65 to +150	°C
Operating ambient temperature	T _{amb}		0 to +70	°C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}	0 to +70	°C
Uniform system supply voltage (range I) (range II)	V_P	11,4 to 13,5	V
	V_P	13,5 to 17	V
D. C. noise margin to all inputs: range I at V_{Pmin} range II at V_{Pmin}	{ M_L	min.	3,3 V
		{ M_H	min.
	{ M_L	min.	3,3 V
		{ M_H	min.
Power consumption (50% duty cycle) at range I : V_{Pmax} at range II : V_{Pmax}	P_{av}	max.	340 mW
	P_{av}	max.	460 mW
Supply current at range I : $V_P = 12 V$ range II : $V_P = 15 V$	I_P	max.	25 mA
	I_P	max.	27 mA
Thermal resistance from system to ambient	R_{th}	max.	150 °C/W



CHARACTERISTICS Test conditions: at range I ($V_P = 12\text{ V}$); $T_{\text{amb}} = 0$ to $+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. 1) max.				Conditions and refe- rences	
						V_P (V)	
Static data							
<u>Voltages</u>							
Input HIGH	V_{IH}	8,0	-	-	V		
Input LOW	V_{IL}	-	-	5,0	V		
Output HIGH	V_{QH}	80	-	-	V	13,5	$-I_{QH} = 1\text{ mA}$
Output LOW	V_{QL}	-	-	2,5	V	11,4	$I_{QL} = 9\text{ mA}$
D. C. noise margin							
HIGH	M_H	2,0	4,5	-	V	11,4	
LOW	M_L	3,3	5,5	-	V	11,4	
<u>Currents</u>							
Input HIGH	I_{IH}	-	-	1,0	μA	13,5	$V_{IH} = 13,5\text{ V}$
Input LOW	$-I_{IL}$	-	0,8	1,5	mA	13,5	$V_{IL} = 0\text{ V}$
Output HIGH:							
input combination 0 to 9	$-I_{QH}$	-	-	50	μA	13,5	$V_{QH} = 70\text{ V}$
input combination 10 to 15	$-I_{QH}$	-	-	5	μA	13,5	$V_{QH} = 60\text{ V}$
Supply data							
Supply current	I_P	-	17	25	mA	13,5	{ input voltage at $I_1, I_4, I_8 = 0\text{ V}$ and at $I_2 = 13,5\text{ V}$

1) All typical values under test conditions: $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

CHARACTERISTICS (continued)

Test conditions: at range I ($V_P = 12\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$.

	Sym- bol	min. typ. 1) max.				Conditions and references
Dynamic data						
<u>Times</u>						
Propagation delay:						
$I_2 \rightarrow Q_2$						$C_L = 10\text{ pF}$ $N = 1$ $T_{amb} = 25\text{ }^\circ\text{C}$ $V_L = 12\text{ V}$ $R_L = 1\text{ k}\Omega$
fall time	t_{pdf}	60	150	280	ns	
rise time	t_{pdr}	30	70	210	ns	
$I_2 \rightarrow Q_0$						
fall time	t_{pdf}	30	70	210	ns	
rise time	t_{pdr}	60	150	280	ns	

1) All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

CHARACTERISTICS (continued)Test conditions: at range II ($V_P = 15$ V); $T_{amb} = 0$ to $+70$ °C

	Sym- bol	min.	typ. 1)	max.	Conditions and refer- ences	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{IH}	8,0	-	-	V	
Input LOW	V_{IL}	-	-	5,0	V	
Output HIGH	V_{QH}	80	-	-	V	17,0 $-I_{QH} = 1$ mA
Output LOW	V_{QL}	-	-	2,5	V	13,5 $I_{QL} = 9$ mA
D. C. noise margin						
HIGH	M_H	4,0	7,5	-	V	13,5
LOW	M_L	3,3	5,5	-	V	13,5
<u>Currents</u>						
Input HIGH	I_{IH}	-	-	1,0	μ A	17,0 $V_I = 17,0$ V
Input LOW	$-I_{IL}$	-	1,0	1,8	mA	17,0 $V_I = 0$ V
Output HIGH:						
input combination 0 to 9	$-I_{QH}$	-	-	50	μ A	17,0 $V_{QH} = 70$ V
input combination 10 to 15	$-I_{QH}$	-	-	5	μ A	17,0 $V_{QH} = 60$ V
Supply data						
Supply current	I_P	-	18	27	mA	17,0 { input voltage at $I_1, I_4, I_8 = 0$ V and at $I_2 = 13,5$ V

1) All typical values under test conditions: $T_{amb} = 25$ °C and $V_P = 15$ V.

CHARACTERISTICS (continued)

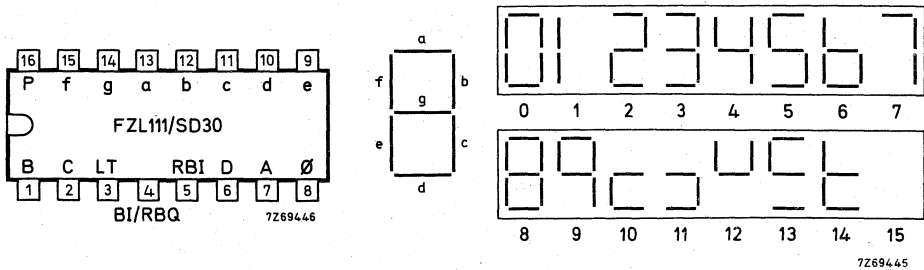
	Sym- bol	min. typ. 1) max.	Conditions and references
Dynamic data			
Propagation delay:			
$I_2 \rightarrow Q_2$			
fall time	t_{pdf}	} t. b. f.	
rise time	t_{pdr}		
$I_2 \rightarrow Q_0$			
fall time	t_{pdf}		
rise time	t_{pdr}		



¹⁾ All typical values under test conditions : $T_{amb} = 25 \text{ }^\circ\text{C}$ and $V_P = 12 \text{ V}$.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

BCD 7-SEGMENT DECODER-DRIVER with open collector outputs



QUICK REFERENCE DATA

Supply voltage (range I)	V_P	nom.	12 V
(range II)	V_P	nom.	15 V
Operating ambient temperature	T_{amb}		0 to +70 °C
Output current per output			
output transistor in off-state	I_Q	max.	25 μ A
output transistor in on-state	I_Q	max.	20 mA
Output voltage at any output (output transistor in off-state)	V_Q	max.	16,5 V
Average supply current at $T_{amb} = 25$ °C			
$V_P = 13,5$ V	I_{Pav}	<	40 mA
$V_P = 16,5$ V	I_{Pav}	<	44 mA
D.C. noise margin at $T_{amb} = 25$ °C			
range I : $V_P = 12$ V	$M_L = M_H$	typ.	5,0 V
range II: $V_P = 15$ V	$\left\{ \begin{array}{l} M_L \\ M_H \end{array} \right.$	typ.	5,0 V
		typ.	8,0 V
Average power consumption			
(50% duty cycle) range I : $V_P = 13,5$ V	P_{av}	max.	540 mW
range II: $V_P = 16,5$ V	P_{av}	max.	725 mW

PACKAGE OUTLINE 16 lead plastic dual in-line (see general section)

GENERAL DESCRIPTION

The FZL111/SD30 transforms 4-bit BCD-words at the inputs A, B, C, D into the 7-segment code. Control functions are provided by means of three auxiliary inputs; BI, RBI, LT. A LOW signal at the ripple-blanking input (RBI) suppresses the decimal 0-signal at the outputs. The ripple-blanking output (RBQ; internally connected with BI) provides an automatic 0-suppression over several decades. When the blanking input (BI) is supplied with a LOW signal, all outputs are blocked. A LOW signal at the lamp-test input (LT) forces all outputs into conduction.

FUNCTION TABLE

function	inputs						BI or RBQ	segment outputs (on-state = L)						
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g
0 ¹⁾	H	H	L	L	L	L	H	L	L	L	L	L	L	H
1	H	X	L	L	L	H	H	H	H	H	H	L	L	H
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H
BI ²⁾	X	X	X	X	X	X	L	H	H	H	H	H	H	H
RBI ³⁾	H	L	L	L	L	L	L	H	H	H	H	H	H	H
LT ⁴⁾	L	X	X	X	X	X	H	L	L	L	L	L	L	L

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

- 1) If 0-indication is desired, RBI must be supplied with a HIGH signal.
- 2) A LOW signal at BI forces all segment outputs into HIGH state independent of the other input conditions.
- 3) If a LOW signal is supplied to RBI and A, B, C, D; HIGH signals result at all outputs and LOW signal at RBQ (zero condition).
- 4) A LOW signal at LT switches all outputs to L only if BI/RBQ is supplied with a HIGH signal regardless of the input condition at A, B, C, D and RBI.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18 V
Output voltage (outputs a to g; off-state)	V_Q	max.	16,5 V
Output current (outputs a to g; off-state)	I_Q	max.	25 μ A
Output current (outputs a to g; on-state) with 50% duty cycle	I_Q	max.	20 mA
	I_Q	max.	40 mA
Storage temperature	T_{stg}		-65 to +150 $^{\circ}$ C
Operating ambient temperature	T_{amb}		0 to +70 $^{\circ}$ C

SYSTEM DESIGN DATA

Uniform system temperature	T_{amb}		0 to +70 $^{\circ}$ C
Uniform system supply voltage (range I) (range II)	V_P	11, 4 to 13, 5 V	
	V_P	13, 5 to 16, 5 V	
D.C. noise margin to all inputs: range I at V_{Pmin} range II at V_{Pmin}	{	M_L	min. 2, 8 V
		M_H	min. 2, 5 V
	{	M_L	min. 2, 8 V
		M_H	min. 4, 5 V
Power consumption (50% duty cycle) at range I : V_{Pmax} at range II: V_{Pmax}	P_{av}	max.	540 mW
	P_{av}	max.	725 mW
Supply current at range I : $V_P = 12$ V at range II: $V_P = 15$ V	I_P	max.	40 mA
	I_P	max.	44 mA
Thermal resistance from system to ambient	R_{th}	max.	150 $^{\circ}$ C/W

CHARACTERISTICS Test conditons: at range I ($V_P = 12\text{ V}$); $T_{\text{amb}} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min.	typ. ¹⁾	max.	Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{IH}	7,5	-	-	V	11,4
Input LOW	V_{IL}	-	-	4,5	V	11,4 and 13,5
Outputs a to g	V_Q	-	-	16,5	V	11,4
Output HIGH at BI/RBQ	V_{QH}	10	11,3	-	V	13,5
Output LOW at outputs a to g	V_{QL}	-	0,4	0,7	V	11,4
	V_{QL}	-	0,7	1,0	V	11,4
at outputs BI/RBQ	V_{QL}	-	-	1,7	V	11,4
D. C. noise margin HIGH	M_H	2,5	5,0	-	V	11,4
LOW	M_L	2,8	5,0	-	V	11,4
<u>Currents</u>						
Input HIGH at A, B, C, D, RBI	I_{IH}	-	-	10	μA	13,5
at BI/RBQ	I_{IH}	-	-	20	μA	13,5
at LT	I_{IH}	-	-	30	μA	13,5
Input LOW at A, B, C, D, RBI	I_{IL}	-	1,0	2,1	mA	13,5
at BI/RBQ	I_{IL}	-	2,0	4,2	mA	13,5
at LT	I_{IL}	-	3,0	5,3	mA	13,5
<u>Supply data</u>						
Supply current	I_P	-	-	40	mA	13,5

¹⁾ All typical values under test conditions: $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ and $V_P = 12\text{ V}$.

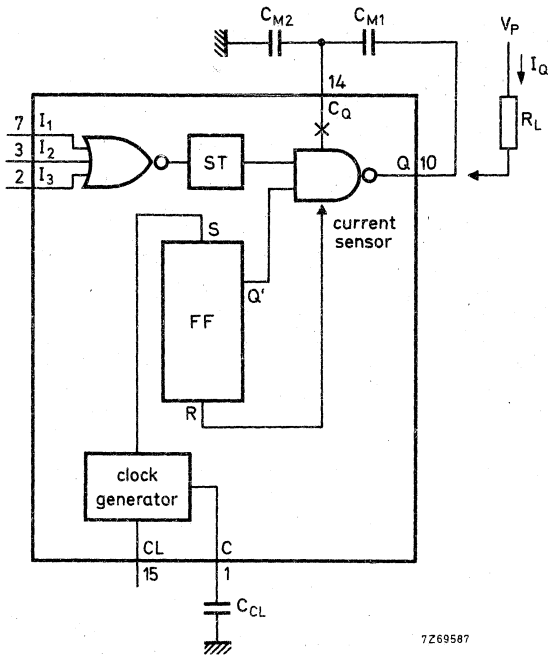
CHARACTERISTICS Test conditions: at range II ($V_P = 15\text{ V}$); $T_{amb} = 0\text{ to }+70\text{ }^\circ\text{C}$

	Sym- bol	min. typ. ¹⁾ max.			Conditions and references	
					V_P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V_{IH}	7,5	-	-	V	13,5
Input LOW	V_{IL}	-	-	4,5	V	13,5 and 16,5
Outputs a to g	V_Q	-	-	16,5	V	13,5 $I_Q = 25\text{ }\mu\text{A}$
Output HIGH at BI/RBQ	V_{QH}	12	14,3	-	V	16,5 $-I_{QH} = 0,1\text{ mA}$
Output LOW at outputs a to g	V_{QL}	-	0,4	0,7	V	13,5 $I_{QL} = 20\text{ mA}$
	V_{QL}	-	0,7	1,0	V	13,5 $I_{QL} = 40\text{ mA}$
at output BI/RBQ	V_{QL}	-	-	1,7	V	13,5 $I_{QL} = 9\text{ mA}$
<u>D. C. noise margin</u>						
HIGH	M_H	4,5	8,0	-	V	13,5
LOW	M_L	2,8	5,0	-	V	13,5
<u>Currents</u>						
Input HIGH at A, B, C, D, RBI at BI/RBQ at LT	I_{IH} I_{IH} I_{IH}	-	-	10 20 30	μA μA μA	16,5 16,5 16,5
						} $V_{IH} = 16,5\text{ V}$
Input LOW at A, B, C, D, RBI at BI/RBQ at LT	I_{IL} I_{IL} I_{IL}	-	-	2,6 5,2 7,8	mA mA mA	16,5 16,5 16,5
						} $V_{IL} = 1,7\text{ V}$
<u>Supply data</u>						
Supply current	I_p	-	-	44	mA	16,5 outputs open

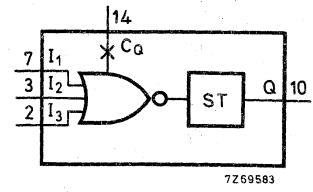
¹⁾ All typical values under test conditions: $T_{amb} = 25\text{ }^\circ\text{C}$ and $V_P = 15\text{ V}$.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

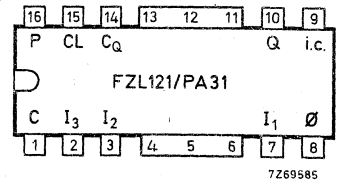
SHORT-CIRCUIT- PROOF POWER STAGE with open collector output



Logic diagram for short-circuit operation



Logic diagram for normal operation



pins 4 to 6 and 11 to 13 are connected to provide a heatsink

QUICK REFERENCE DATA

Supply voltage range	V_P	11, 4 to 20 V
Operating ambient temperature	T_{amb}	0 to +70 °C
Output current	I_Q	max. 400 mA
Supply current	I_P	typ. 5 mA
Capacitance at CL	C_{CL}	typ. 39 nF
Capacitance at CQ	C_{M1}	typ. 500 pF
	C_{M2}	typ. 1, 8 nF

PACKAGE OUTLINE 16 lead plastic dual in-line (see page 218).

GENERAL DESCRIPTION

The FZL121/PA31 is a power stage for output currents up to 400 mA. It has 3-NOR gate inputs with Schmitt trigger characteristics.

The load is connected between the output Q (open collector) and the supply terminal P. If a short circuit occurs the current is turned off and the circuit checks periodically whether the short circuit is still present.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	20	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_{IH}	max.	V_P	
Output current	I_Q	max.	400	mA
Storage temperature	T_{stg}		-65 to +150	°C
Operating ambient temperature	T_{amb}		0 to +70	°C

CHARACTERISTICS Test conditions: $T_{amb} = 0$ to $+70$ °C

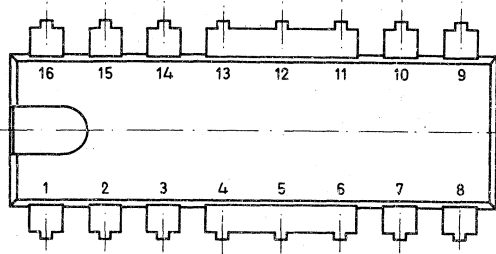
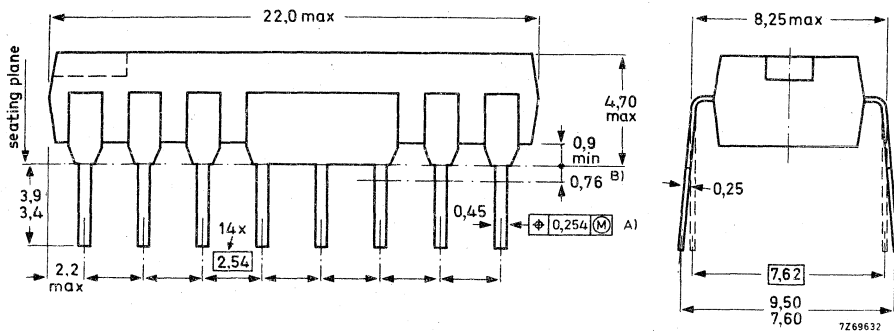
	Sym- bol	min.	typ.	max.	Conditions and refer- ences		
					V_P (V)		
<u>Voltages</u>							
Input HIGH	V_{IH}	8	-	-	V	11, 4	
Input LOW	V_{IL}	-	-	6	V	20	
Hysteresis	V_H	-	0, 4	-	V	15	
Output LOW	V_{QL}	-	1, 6	2, 6	V	$\left\{ \begin{array}{l} I_Q = 0, 4 \text{ A} \\ V_I = V_P \end{array} \right.$	
<u>Currents</u>							
Input current	I_I	0, 1	-	0, 2	mA	$V_I = 2 \text{ V to } V_P$	
Output current	I_Q	-	-	400	mA		20
Supply current	I_P	-	5	-	mA	15	$I_Q = 0$
Nominal lamp current	I_Q	-	-	150	mA	20	
<u>Capacitors</u>							
Capacitance at CL	C_{CL}	-	39	-	nF	$f = 0, 5 \text{ kHz}$	
Capacitance at C_Q	C_{M1}	-	500	-	pF		
	C_{M2}	-	1, 8	-	nF		
Capacitive loads	C_L	-	-	each C_M	nF		

OPERATING NOTES (see also logic diagram on page 215)

To avoid oscillations during a short circuit it is necessary to connect two capacitors to the C_Q -terminal (C_{M1} , C_{M2}). The transition at the output Q can be varied by means of C_{M1} . A capacitor C_{CL} between the C-terminal and ground is required for the clock generator. Up to 8 clock terminals CL of the types FZL121/PA31, FZL131/PA32 may be connected in parallel so that only one capacitor C_{CL} is required. The C-terminals of the remaining circuits must then be connected to V_p . Inductive loads must be provided with a flywheel diode.



16 LEAD PLASTIC DUAL IN-LINE



top view

A) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal positions shown; in the worst case, the spacing between adjacent leads may deviate from nominal by $\pm 0,254$ mm.

B) Tolerances of note A within this distance

⊕ Locational truth

(M) Maximum Material Condition

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

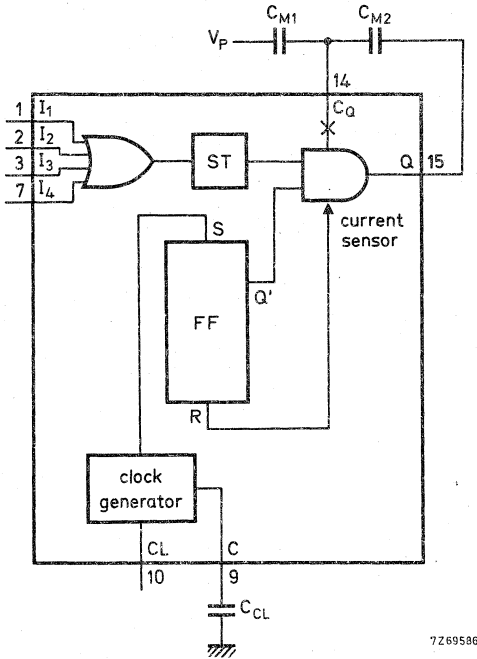
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

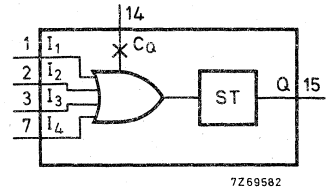
The same precautions and limits apply as in (1) above.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

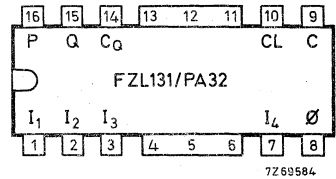
SHORT-CIRCUIT-PROOF POWER STAGE with open collector output



Logic diagram for short circuit operation



Logic diagram for normal operation



pins 4 to 6 and 11 to 13 are connected to provide a heatsink

QUICK REFERENCE DATA

Supply voltage range	V_P	11,4 to 20 V
Operating ambient temperature	T_{amb}	0 to +70 °C
Output current	I_Q	max. 400 mA
Supply current	I_P	typ. 5 mA
Capacitance at CL	C_{CL}	typ. 39 nF
Capacitance at CQ	C_{M1}	typ. 500 pF
	C_{M2}	typ. 1,8 nF

PACKAGE OUTLINE 16 lead plastic dual in-line (see page 222).

GENERAL DESCRIPTION

The FZL131/PA32 is a power stage for output currents up to 400 mA and for nominal lamp currents of up to 150 mA. It has 4-OR gate inputs with Schmitt trigger characteristics. The load is connected between the output Q (open emitter) and the ground terminal ϕ . If a short circuit occurs the current is turned off and the circuit checks periodically whether the short circuit is still present.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Supply voltage	V_P	max.	20	V
Output voltage	V_Q	max.	V_P	
Input voltage	V_{IH}	max.	V_P	
Output current	I_Q	max.	400	mA
Storage temperature	T_{stg}		-65 to +150	$^{\circ}C$
Operating ambient temperature	T_{amb}		0 to +70	$^{\circ}C$

CHARACTERISTICS Test conditions: $T_{amb} = 0$ to $+70$ $^{\circ}C$

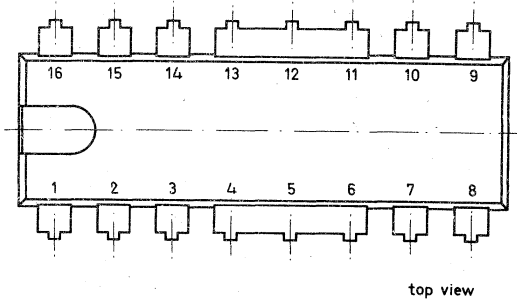
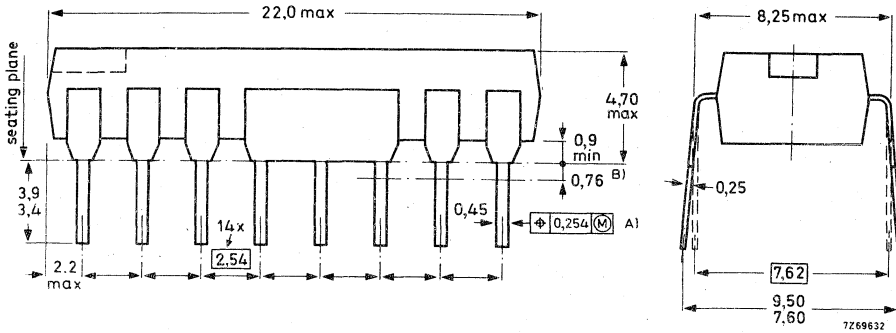
	Sym- bol	min.	typ.	max.	Conditions and refer- ences	
					V_P (V)	
<u>Voltages</u>						
Input HIGH	V_{IH}	8	-	-	V	11, 4
Input LOW	V_{IL}	-	-	6	V	20
Hysteresis	V_H	-	0, 4	-	V	15
Output HIGH	V_{QH}	V_P-3	$V_P-1, 8$	-	V	$-I_Q = 0, 4$ A
<u>Currents</u>						
Input current	I_I	0, 1	-	0, 2	mA	$V_I = 2$ V to V_P
Output current HIGH	$-I_{QH}$	-	-	400	mA	20
Supply current	I_P	-	5	-	mA	15 $I_Q = 0$
Nominal lamp current	I_Q	-	-	150	mA	20
<u>Capacitors</u>						
Capacitance at CL	C_{CL}	-	39	-	pF	$f = 0, 5$ kHz
Capacitance at CQ	CM1	-	500	-	pF	
	CM2	-	1, 8	-	nF	

OPERATING NOTES (see also logic diagram on page 219)

To avoid oscillations during a short circuit it is necessary to connect two capacitors to the C_Q -terminal (C_{M1} , C_{M2}). The transition at the output Q can be varied by means of C_{M1} . A capacitor C_{CL} between the C-terminal and ground is required for the clock generator. Up to 8 clock terminals CL of the types FZL121/PA31, FZL131/PA32 may be connected in parallel so that only one capacitor C_{CL} is required. The C-terminals of the remaining circuits must then be connected to V_p . Inductive loads must be provided with a flywheel diode.



16 LEAD PLASTIC DUAL IN-LINE



A) Centre-lines of all leads are within $\pm 0,127$ mm of the nominal positions shown; in the worst case, the spacing between adjacent leads may deviate from nominal by $\pm 0,254$ mm.

B) Tolerances of note A within this distance

- ⊕ Locational truth
- Ⓜ Maximum Material Condition

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

260 °C is the maximum allowable temperature of the solder; it must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

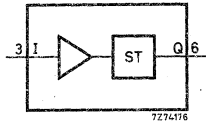
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the allowable limit.

3. Repairing soldered joints

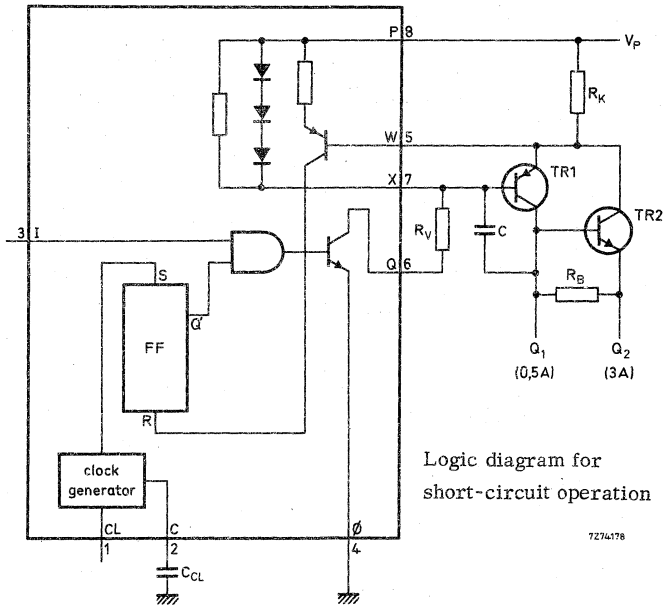
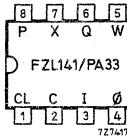
The same precautions and limits apply as in (1) above.

The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

SHORT-CIRCUIT-PROOF POWER DRIVER FOR TRANSISTOR STAGES



Logic diagram for normal operation



QUICK REFERENCE DATA

Supply voltage range	V_p	11,4 to 20	V
Operating ambient temperature	T_{amb}	0 to +70	°C
Output current at Q	$-I_Q$	max.	25 mA
at Q ₁	I_{Q1}	max.	500 mA
at Q ₂	I_{Q2}	max.	3 A

PACKAGE OUTLINE 8 lead plastic dual in-line (see page 225).

GENERAL DESCRIPTION

The FZL141/PA33 is a driver for transistor power stages with output currents up to 3 A and it has a SCHMITT trigger input. The output (Q_2) of the controlled power stage is short-circuit-proof. If a short circuit occurs the current is turned off and the circuit checks periodically whether the short circuit is still present. The load is connected between output Q_1 (or Q_2) and the ground terminal ϕ .

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	20 V
Output voltage at Q_1	V_{Q1}	max.	V_P
at Q_2	V_{Q2}	max.	V_P
Output current at Q	$-I_Q$	max.	25 mA
at Q_1	I_{Q1}	max.	500 mA
at Q_2	I_{Q2}	max.	3 A
Input voltage	V_I	max.	V_P
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$
Operating ambient temperature	T_{amb}	0 to +70	$^{\circ}C$

CHARACTERISTICS Test conditions : $T_{amb} = 0$ to $+70$ $^{\circ}C$

	Sym- bol	min.	typ.	max.	Conditions and references	
					V_P (V)	
<u>Voltages</u>						
Input HIGH	V_{IH}	8	-	- V	11, 4	
Input LOW	V_{IL}	-	-	6 V	20	
Hysteresis	V_H	-	0, 4	- V		
Output at Q_1	V_{Q1}	$V_P-1, 8$	V_P-1	- V		$I_{Q1} = 0, 5$ A
Output at Q_2	V_{Q2}	$V_P-3, 2$	V_P-2	- V		$I_{Q2} = 3$ A
Turn-off voltage for overload	V_W	-	$V_P-0, 8$	- V		
<u>Currents</u>						
Input current	I_I	0, 1	-	0, 2 mA		$V_I = 2$ V to V_P
Input current at X	I_X	-	-	25 mA		
Output current at Q	$-I_Q$	-	-	25 mA		
at Q_1	I_{Q1}	-	-	500 mA		$R_K = 1, 6$ Ω
at Q_2	I_{Q2}	-	-	3 A		$R_K = 0, 33$ Ω
Resistance	R_v	$\frac{V_P-1(V)}{I_Q(mA)}$	-	- k Ω		
	R_B	-	68	- Ω		TR2 = 2N3055

OPERATING NOTES (see also logic diagram on page 223)

To avoid oscillations during a short-circuit it is necessary to connect a capacitor (C) between the base and collector of transistor TR1. A capacitor C_{CL} between the C-terminal and ground is required for the clock generator. Up to 8 clock terminals CL of the types FZL121/PA31, FZL131/PA32 and FZL141/PA33 may be combined in parallel so that only one capacitor C_{CL} is required. The C-terminals of the remaining circuits must then be connected to V_P . Inductive loads must be provided with a flywheel diode.

APPLICATION INFORMATION

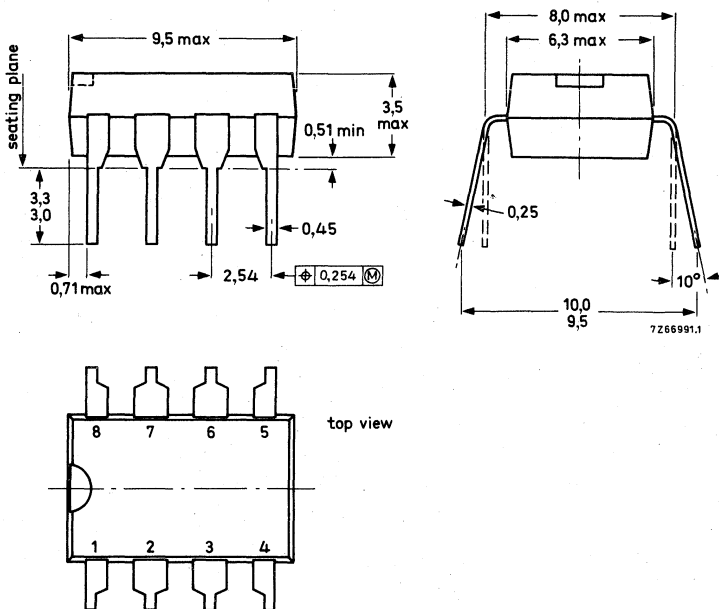
A recommended type for TR1 is the BD227 (if only 0,5 A is required). If 3 A output current is required, the BD227 for TR1 and the 2N3055 for TR2 are recommended, R_B is then 68Ω .

The 2N3055 must be mounted on a heatsink of $50 \times 50 \times 1$ mm Al.

Recommended value for $R_V = V_P/20$ k Ω .

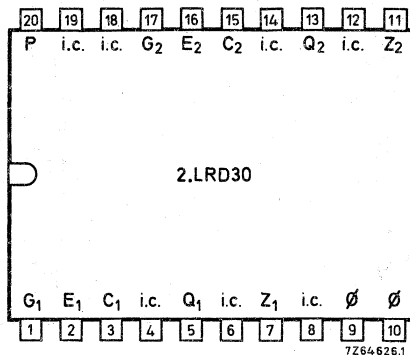
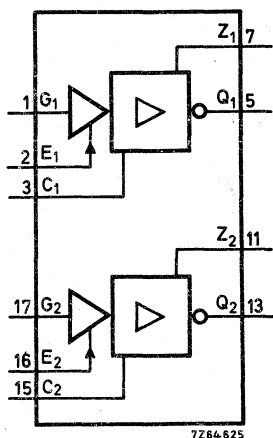
8 LEAD PLASTIC DUAL IN-LINE

Dimensions in mm



The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

DUAL LAMP/RELAY DRIVER



QUICK REFERENCE DATA

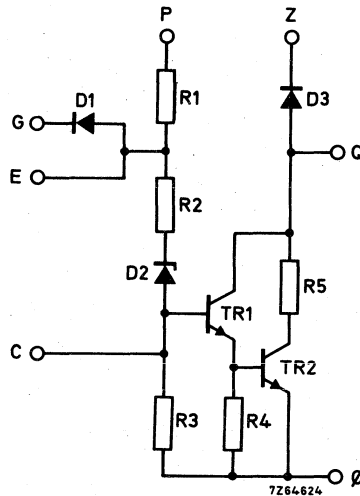
Supply voltage	V_P	11, 4 to 17, 0 V
when loaded	V_{Pload}	max. 30 V
Operating ambient temperature	T_{amb}	-30 to +75 °C
Output current (d. c.)		
$T_{amb} = -35$ to +75 °C; $V_{Pload} = 30$ V	I_{QL}	max. 200 mA
Non-repetitive peak output current		
$t_{max} = 20$ ms	I_{QLM}	max. 400 mA
D. C. noise margin at $T_{amb} = 25$ °C	M_L	typ. 6 V
	M_H	typ. 7 V
Average power consumption		
$T_{amb} = 25$ °C; $V_P = 15$ V; $Q =$ unloaded	P_{av}	typ. 40 mW

Note

Necessary input drive equal to 3 gate loads.

PACKAGE OUTLINE 20 lead dual in-line (see general section).

CIRCUIT DIAGRAM



GENERAL DESCRIPTION

The 2.LRD30 is a dual driver for output currents up to 200 mA at a supply voltage of maximum 30 V; it is used for driving lamps and relays.

The number of gate inputs can be extended by connecting up to 15 Si diodes to the expander terminal E (connect anodes of diodes to E) *).

With inductive loads the built-in clamping diode D3 must be used. This is done by connecting terminal Z to the load supply voltage, to protect the output transistor against damage caused by high inductive voltages.

To improve the a. c. noise immunity by increasing the propagation delay time, a capacitor has to be connected between terminals C and ϕ .

With a resistive load, the capacitor is connected between C and Q.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134).

Supply voltage	V_p	max.	20 V
when loaded	V_{pload}	max.	30 V
Output voltage	V_{QH}	max.	30 V
Input voltage	V_{GH}	max.	30 V
Negative input voltage	$-V_G$	max.	4 V
Storage temperature	T_{stg}		-30 to + 85 °C
Operating ambient temperature	T_{amb}		-30 to + 75 °C

*) Diode leads should be kept as short as possible.

CHARACTERISTICSTest conditions: $T_{amb} = -30$ to $+70$ °C

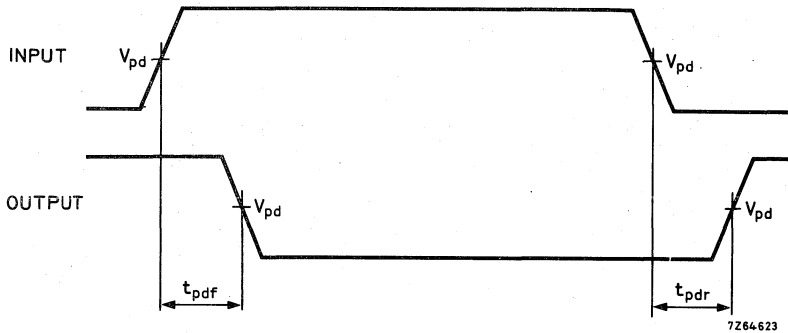
	sym- bol	min. typ. ¹⁾ max.			Conditions and references	
					V _P (V)	
Static data						
<u>Voltages</u>						
Input HIGH	V _{GH}	8,0	-	-	V	11,4 and 17,0 } V _Q = LOW
Input LOW	V _{GL}	-	-	4,5	V	11,4 and 17,0 } I _Q = 0,5 mA
Output LOW	V _{QL}	-	0,9	1,3	V	11,4 } V _{GH} ≥ 8,0 V I _Q = 200 mA
D.C. noise margin: HIGH	M _H	2,0	7	-	V	11,4
LOW	M _L	2,8	6	-	V	11,4 and 17,0
<u>Currents</u>						
Input HIGH	I _{GH}	-	0,1	10	μA	11,4 and 17,0 } V _G = 17,0 V
Input LOW	-I _{GL}	-	-	5,4	mA	17,0 } V _{GL} = 1,7 V
Output HIGH	I _{QH}	-	-	0,5	mA	11,4 and 17,0 } V _{GL} ≤ 4,5 V V _{Pload} = 30 V
Output LOW	I _{QL}	-	-	200	mA	11,4 and 17,0 } V _G ≥ 8,0 V
Non-repetitive peak value; t _{max} = 20 ms	I _{QLM}	-	-	400	mA	11,4 and 17,0 } V _{GH} ≥ 8,0 V
<u>Supply data</u>						
<u>Currents</u>						
at V _{QH}	I _P	-	4,2	4,9	mA	17,0 } V _G = 1,7 V
at V _{QL}	I _P	-	2,2	3,4	mA	17,0 } V _G ≥ 8,0 V
<u>Dynamic data</u>						
Input rise time	t _r	0,1	-	-	V/μs	
Input fall time	t _f	0,1	-	-	V/μs	

¹⁾ Typical values specified at V_P = 15 V and T_{amb} = 25 °C.

CHARACTERISTICS (continued)

Dynamic data

Loading capacitor connected between C and ϕ .



Waveforms illustrating measurement of t_{pdr} and t_{pdf} .

Measuring conditions: $V_P = 15\text{ V}$
 $I_{QL} = 200\text{ mA}$
 $C_L = 10\text{ pF}$
 resistive load

input waveform: $V_{pd} = \frac{1}{2} V_P$
 output waveform: $V_{pd} = \frac{1}{2} V_{Pload}$

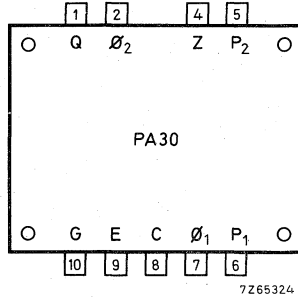
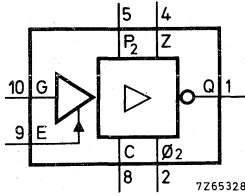
$$t_{pdf} = (0,55 + 0,55 \times C_L) \text{ ns}$$

$$t_{pdr} = (0,30 + 0,30 \times C_L) \text{ ns}$$

C_L in nF; C_L is 10 to 1000 nF

The 30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

POWER AMPLIFIER



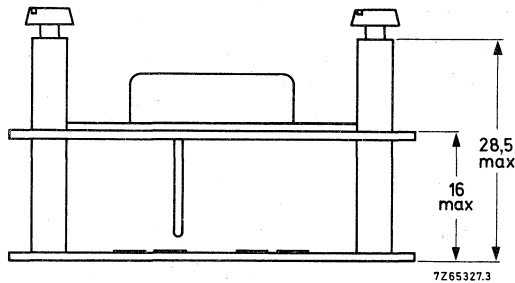
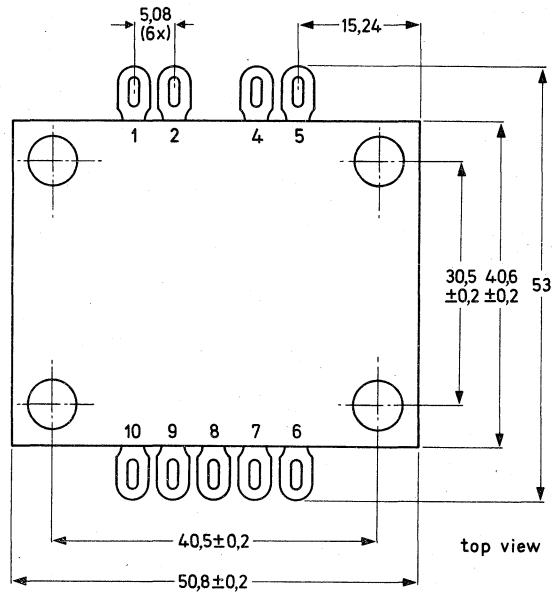
QUICK REFERENCE DATA				
Supply voltage	V _{P1}	11, 4 to 17, 0	V	
	V _{PS}	11, 4 to 55	V	
Operating ambient temperature	T _{amb}	-30 to +75	°C	
Output current (t _{av} = 20 ms)	I _{QL}	max. 2	A	
Repetitive peak output current	I _{QLM}	max. 5	A	
D.C. noise margin at T _{amb} = 25 °C	M _L	typ. 5	V	
	M _H	typ. 8	V	
Average power consumption at T _{amb} = 25 °C V _{P1} = 15 V; Q = unloaded; V _{PS} = 15 V; R _V = 0	P _{av}	typ. 240	mW	

PACKAGE OUTLINE 9 leads special execution (see next page).

PACKAGE OUTLINE

Dimensions in mm

9 leads special execution



GENERAL DESCRIPTION

The PA30 is a power amplifier for output currents up to 2 A and output voltages up to 55 V, intended for driving heavy resistive and inductive loads.

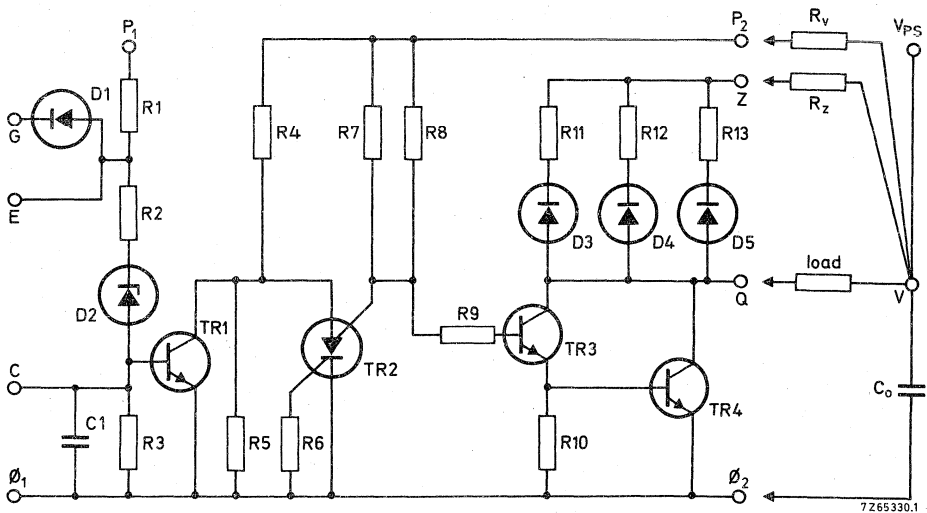
The number of gate inputs can be extended by connecting up to 15 diodes (type BAW62) to the expander terminal E (connect anode of diode to E). *)

To increase the a. c. noise immunity, a capacitor can be connected between terminals C and ϕ_1 (see also "Operating notes"). The load has to be connected between Q and point V. For inductive loads, terminal Z must also be connected to V, if necessary via a series resistor R_Z (see note 3 of "Operating notes").

Dependent on the V_{PS} value, a resistor R_V must be connected between terminal P_2 and point V (see note 1 of "Operating notes").

When the wire connection between V and supply voltage unit V_{PS} has some inductance, it is necessary to connect a capacitor C_0 ($\approx 10 \mu\text{F}$ per metre of wire) between V and ϕ_2 as close as possible to the unit.

CIRCUIT DIAGRAM



*) Diode leads should be kept as short as possible.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltages	V_{PI}	max.	20	V
	V_{PS}	max.	55	V ¹⁾
Output voltage	V_{QH}	max.	55	V
Input voltage	V_{GH}	max.	30	V
Negative input voltage	$-V_{GL}$	max.	4	V
Output current (average; $t_{av} = 20$ ms)	I_{QL}	max.	2	A
Output current (peak value)	I_{QLM}	max.	5	A
Storage temperature	T_{stg}		-40 to +85	°C
Operating ambient temperature	T_{amb}		-30 to +75	°C

¹⁾ See note 1 of "Operating notes".

CHARACTERISTICS Test conditions: $T_{amb} = -30$ to $+75$ °C

	Sym- bol	min. typ. ¹⁾ max.		Conditions and references			
				V _P (V)			
Static data							
<u>Voltages</u>							
Input HIGH	V _{GH}	7,5	-	-	V	11,4 and 17,0	} V _Q = LOW
Input LOW	V _{GL}	-	-	4,5	V	11,4 and 17,0	
Output HIGH	V _{QH}	-	-	55	V	11,4 and 17,0	} I _Q = 5 mA V _G ≤ 4,5 V
Output LOW	V _{QL}	-	0,9	1,3	V	11,4 and 17,0	
D. C. noise margin: LOW	M _L	2,8	5	-	V	11,4 and 17,0	} I _Q = 2 A V _G ≥ 7,5 V
	HIGH	M _H	2,5	8	-	V	
<u>Currents</u>							
Input HIGH	I _{GH}	-	0,1	10	μA	17,0	V _G = 17 V
Input LOW	-I _{GL}	-	-	5,1	mA	17,0	V _G = 1,7 V
Output HIGH	I _{QH}	-	1 μA	5	mA	11,4 and 17,0	} V _{QH} = 55 V V _G ≤ 4,5 V
Output LOW (t _{av} = 20 ms)	I _{QL}	-	-	2	A	11,4 and 17,0	
(peak value)	I _{QLM}	-	-	5	A	11,4 and 17,0	} V _{QL} = 1,3 V V _G ≥ 7,5 V

¹⁾ All typical values under test conditions: V_{P1} = 15 V; V_{PS} = 15 V; R_v = 0; T_{amb} = 25 °C.

CHARACTERISTICS (continued) Test conditions: $T_{amb} = -30$ to $+75$ °C

	Sym- bol	min. typ. I) max.	Conditions and references	
			V_P (V)	
Supply data				
<u>Currents</u>				
	I_{P1}	- 4,3 - mA	15	$V_G = 1,7$ V
	I_{P1}	- 2,6 - mA	15	$V_G \geq 7,5$ V
	I_{P2}	- 14,5 - mA	15	$V_G \leq 4,5$ V
	I_{P2}	- 12,5 - mA	15	$V_G \geq 7,5$ V

I) All typical values under test conditions: $V_{P1} = 15$ V; $V_{PS} = 15$ V; $R_V = 0$; $T_{amb} = 25$ °C.

OPERATING NOTES**1. Supply voltage V_{PS}**

When terminal P₂ is directly connected to point V the value of V_{PS} must be between 11, 4 V and 19 V ($15, 2 V \pm 25\%$).

By connecting a suitable resistor (R_V) between P₂ and V, any supply voltage V_{PS} between 11, 4 and 55 V may be used, having a tolerance of $\pm 25\%$.

The values of R_V can be calculated from:

$$R_V = 75 (V_{PSnom} - 15) \Omega \pm 8\%$$

2. For capacitor C_O see "General description"**3. Unit loaded with an inductive load**

When an inductive load is switched, the built-in diodes (which protect the output transistor against voltage transients) have to be connected (Z to point V).

This protection is realized at the expense of a very long decay time of the current in the load.

At V_{PS} below 55 V a resistor R_Z may be connected in series with the protection diodes to decrease this decay time.

The maximum permissible value of R_Z can be calculated from:

$$R_Z < \frac{1}{I_Q} (55 - V_{PSmax}) \Omega$$

Where: I_Q = the load current at switching-off.

The decay time of the load current can be calculated from:

$$I_L = I_Q \exp - \frac{t}{L/R}$$

Where: I_Q = the load current at switching-off in amperes

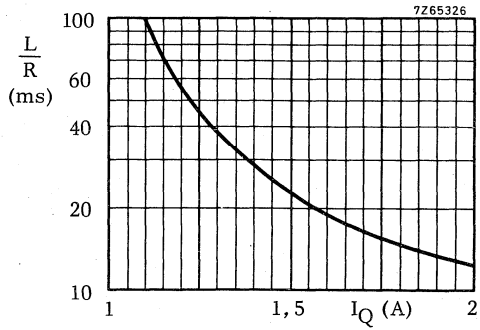
L = inductance of the load in henrys

R = sum resistance of load and possible applied R_Z in ohms

Note: V may be connected directly to Z ($R_Z = 0$) if there are no problems with decay time.

OPERATING NOTES (continued)

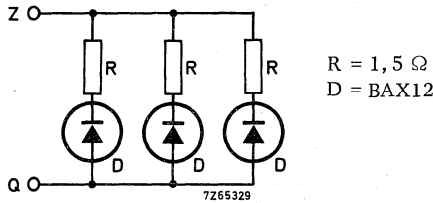
4. Inductance of the load



The maximum allowable inductance of the load can be calculated from the maximum permissible value of L/R as follows from the graph above.

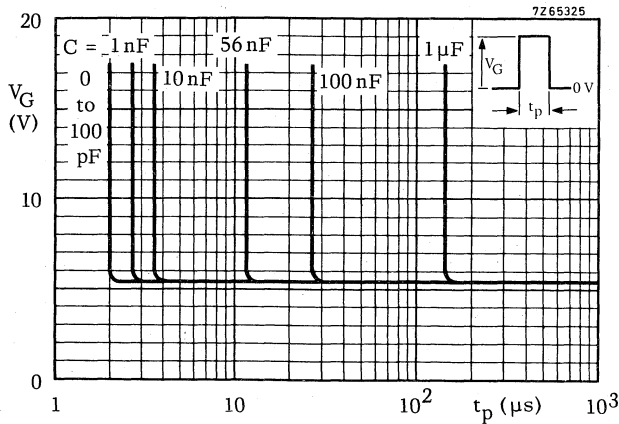
I_Q = the load current at switching-off.

R = sum resistance of load and possible applied R_Z .



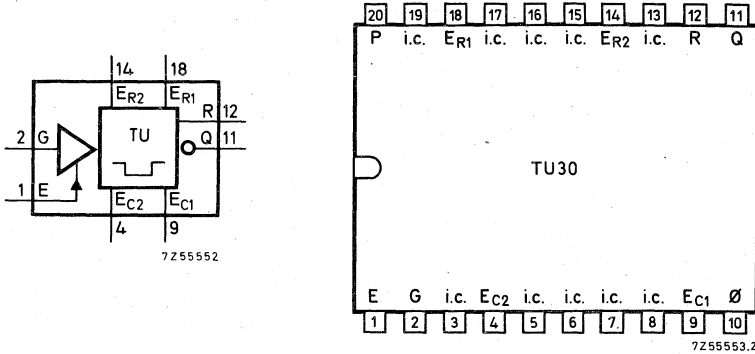
When the above circuit is connected between the terminals Z and Q, loads with any inductance value and currents up to 2 A can be applied.

5. Input voltage versus input pulse duration as a function of a capacitor between terminals C and ϕ_1 .



The FZ/30-Series has been designed for high noise immunity low speed digital applications in industrial control, computer periphery equipment and data processing.

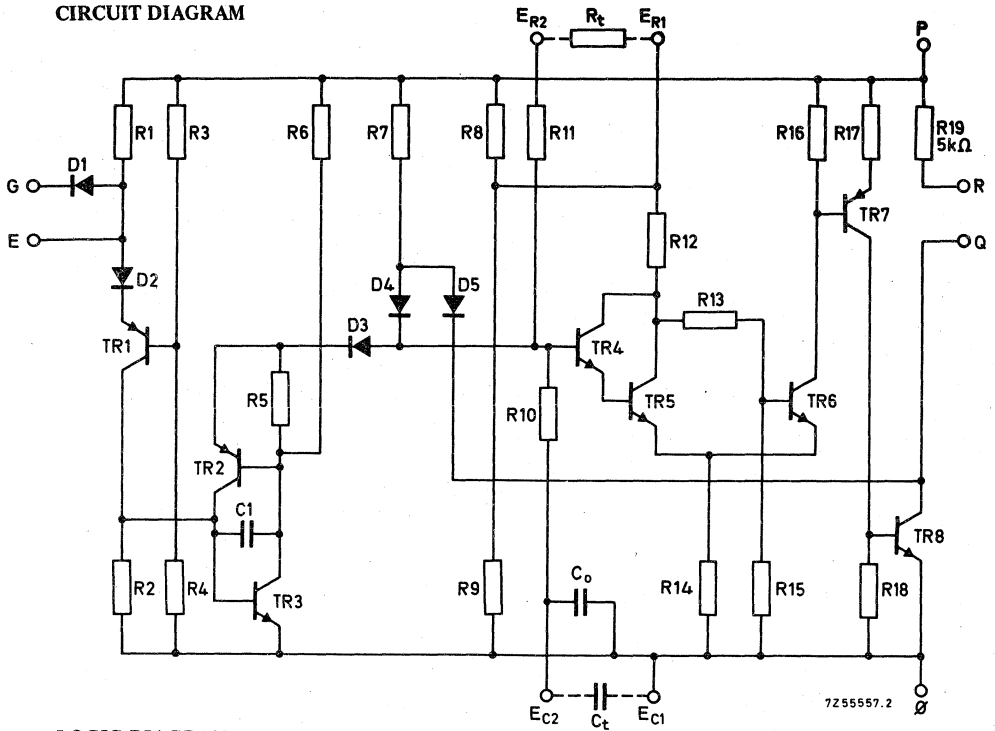
TIMER UNIT



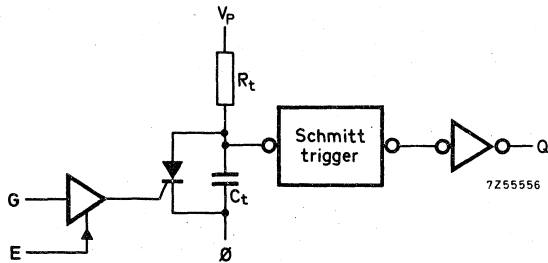
QUICK REFERENCE DATA			
Supply voltage	V_P	11, 4 to 17, 0	V
Operating ambient temperature	T_{amb}	-30 to +75	$^{\circ}C$
Delay time; $T_{amb} = 25^{\circ}C$	t_d	max. 10	s/ μF
Available d. c. fan-out ($T_{amb} = -25$ to $+70^{\circ}C$)	} LOW state	N_{aL}	max. 22
D. C. noise margin at $T_{amb} = 25^{\circ}C$ $V_P = 15$ V	M_L	typ. 6,5	V
	M_H	typ. 6,5	V
Power consumption at $T_{amb} = 25^{\circ}C$	P_{av}	typ. 300	mW

PACKAGE OUTLINE 20 lead dual in-line (see general section).

CIRCUIT DIAGRAM



LOGIC DIAGRAM



GENERAL DESCRIPTION

The TU30 is a direct-coupled timer that gives a constant delay irrespective of the duration of the gate input signal. The delay begins when the gate input changes from HIGH to LOW (see timing diagram). When the gate input changes from LOW to HIGH, the output goes LOW. A gate input signal during a delay cycle will restart the delay.

The length of the delay is determined by an external capacitor connected across terminals E_{C1} and E_{C2} , and an external resistor connected across terminals E_{R1} and E_{R2} .

The number of gate inputs can be extended by connecting up to 15 diodes (BAW62) to the expander input terminal E (connect anode of diode to terminal E). *)

To prevent capacitive coupling with other lines the connection between the diodes and expander inputs must be as short as possible.

When using the TU30 to drive other members of the FZ/30-Series, interconnect terminals Q and R.

When using it to drive a small relay, connect the relay across terminals Q and P, and leave terminal R unconnected (floating).

When driving an inductive load (also relays), connect a clamping diode (such as a BAW62) across terminals Q and P (anode of diode to terminal Q). *)

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_P	max.	18	V
Output voltage	V_{QH}	max.	V_P	
Output current (Q and R not interconnected)	I_{QL}	max.	46	mA
Input voltages	V_G	max.	18	V
	$-V_G$	max.	1	V
Input current (for negative input voltage)	$-I_G$	max.	2,0	mA
Output capacitance	C_L	max.	500	pF
Storage temperature	T_{stg}		-25 to +85	°C
Operating ambient temperature	T_{amb}		-25 to +70	°C

*) Diode leads should be kept as short as possible.

CHARACTERISTICS Test conditions: $T_{amb} = -25$ to $+70$ °C.

	Sym- bol	min. typ ¹⁾ max.		Conditions and references				
				V_P (V)				
Static data								
<u>Voltages</u>								
Input HIGH	V_{GH}	6,8	-	-	V	11,4	$I_{QL} = 43$ mA *) $I_{QL} = 46$ mA **)	
	V_{GH}	9,3	-	-	V	17,0		
Input LOW	V_{GL}	-	-	4,5	V	11,4	$V_{QHmin} = 0,9$ V _P $-I_{QH} = 0,25$ mA	
	V_{GL}	-	-	7,3	V	17,0		
Output HIGH	V_{QH}	10	13	-	V	11,4	} $V_{GL} = 4,5$ V } $-I_{QH} = 0,25$ mA	
	V_{QH}	15,3	-	-	V	17,0		
Output LOW	V_{QL}	-	-	0,5	V	11,4	{ $V_{GH} = 6,8$ V } $I_{QL} = 43$ mA *) } $I_{QL} = 46$ mA **)	
D.C. noise margin:	HIGH	M_H	3,2	-	-	V	11,4	$V_{GH} = 10$ V
	LOW	M_L	2,8	-	-	V	11,4	$V_{GL} = 1,7$ V
	HIGH	M_H	-	6,5	-	V	15,0	$V_{GH} = 1,4$ V
	LOW	M_L	-	6,5	-	V	15,0	$V_{GL} = 1,0$ V
<u>Currents</u>								
Input HIGH	I_{GH}	-	-	1	µA	17,0	$V_{GH} = 17,0$ V	
Input LOW	$-I_{GL}$	-	-	0,95	mA	11,4	} $V_{GL} = 1,7$ V	
	$-I_{GL}$	-	-	1,6	mA	17,0		
Output HIGH	$-I_{QH}$	-	-	0,50	mA	11,4	{ $V_{GL} = 4,5$ V } $V_{QH} = 10$ V *)	
	$-I_{QH}$	-	-	0,50	mA	17,0	{ $V_{GL} = 7,3$ V } $V_{QH} = 15,3$ V *)	
Output LOW	I_{QL}	-	-	43	mA	11,4 and 17,0	{ $V_{GH} = 0,6$ V _P } $V_{QL} = 0,5$ V *)	
	I_{QL}	-	-	46		11,4 and 17,0	{ $V_{GH} = 0,6$ V _P } $V_{QL} = 0,5$ V **)	
Supply data								
<u>Currents</u>								
Output HIGH	I_P	-	6,5	7,5	mA	17,0	$V_G = 0$ V	
Output LOW	I_P	-	17	20	mA	17,0	$V_G = 17$ V	

1) Typ. values specified at $V_P = 15$ V and $T_{amb} = 25$ °C.

*) Terminal R connected to terminal Q.

***) Terminal R not connected.

CHARACTERISTICS at $V_P = 15 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ **Dynamic data**

Gate input HIGH duration	T_{GH}	>	5	μs
Output rise time for $C_L = 10 \text{ pF}$	t_{QR}	typ.	110	ns ¹⁾
Output fall time for $R_C = 5 \text{ k}\Omega$; $C_L = 10 \text{ pF}$	t_{Qf}	typ.	50	ns
Fall propagation delay time	t_{pdf}	typ.	3	μs
Delay time (C_t in F; R_t in Ω)	t_d	>	1	ms
Timing resistor	R_t	typ. $C_t(R_t + 10 \text{ k}\Omega)$		s
Timing capacitor	C_t	no limit		$\text{M}\Omega$ ²⁾
Change in delay time versus temperature ($R_t = 1 \text{ M}\Omega$; $V_P = 15 \text{ V}$)		typ.	-0,1	%/ $^\circ\text{C}$
Change in delay time versus supply voltage ($T_{\text{amb}} = 25 \text{ }^\circ\text{C}$; $R_t = 1 \text{ M}\Omega$)		typ.	-0,5	%/ $^\circ\text{C}$

¹⁾ $t_{\text{QR}} = (11 \times C_L) \text{ ns}$. C_L is the wiring capacitance in pF with a maximum permissible value of 500 pF.

²⁾ Preferred value for C_t : $> 1 \text{ nF}$.

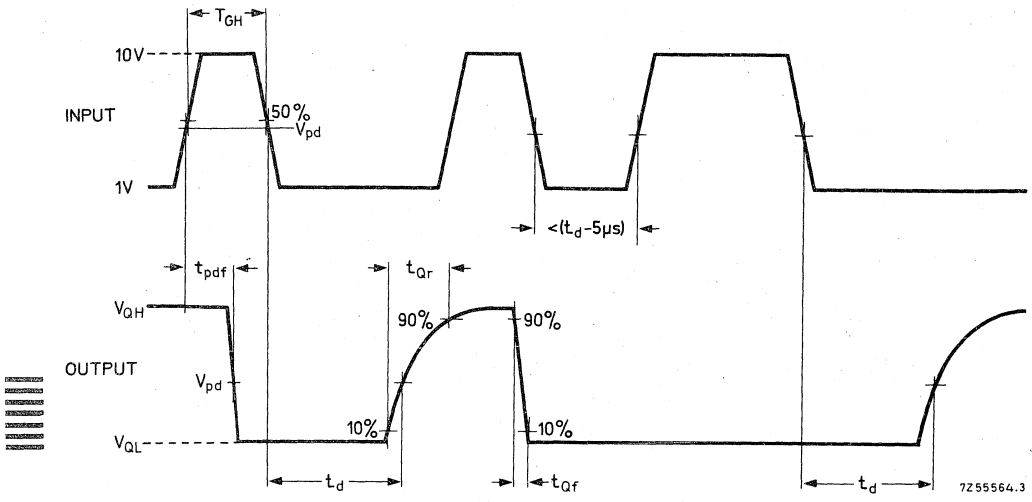
The circuit is not developed for electrolytic capacitors because of their high leakage currents. However, electrolytic capacitors may be used (+ side connected to terminal E_{C2}), provided that the charge current is large compared to the leakage current of the capacitor e. g.:

$$I_{\text{charge}} > 10 \cdot I_{\text{leakage}}$$

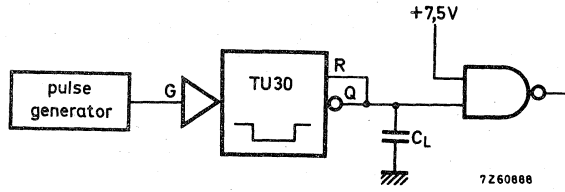
$$\text{where } I_{\text{charge}} = \frac{0,3 V_P}{R_t + 10 \text{ k}\Omega}$$

CHARACTERISTICS (continued)

Dynamic data



Pulse generator (G-input): $t_r = 350 \text{ ns}$
 $t_f = 120 \text{ ns}$
 $t_{GH} = 5 \mu\text{s}$
 $V_{pd} = 4,5 \text{ V}$



Measuring conditions: $V_P = +15 \text{ V}$
 $C_L = 10 \text{ pF}$ (including probe and jig capacitance)
 $T_{amb} = +25 \text{ }^\circ\text{C}$

Waveforms and loading circuit illustrating measurement of t_{Qr} , t_{Qf} and t_{pdf} .

Accessories for HNIL FZ/30-Series



STICKERS

The drawing of circuit diagrams is simplified by the use of stickers of the drawing symbols of the FZ/30-Series. These stickers, printed on self-adhesive transparent material, are available in sheets. Each sticker can be separately detached from the sheet without cutting.

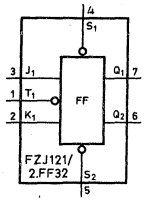
sheets with symbols for type	catalogue number for 25 sheets	symbols per sheet
FZH101/4.NAND32	4322 026 75420	{ 5 x NAND 10 x NAND* 10 x OR*● 5 x OR●
FZH111/4.NAND30		
FZH121/2.NAND30		
FZH131/2.NAND31		
FZH141/2.NAND32		
FZH151/2.AOR30	4322 026 75460	12 x
FZH161/4.LI31	4322 026 75420	{ 5 x NAND 10 x NAND* 10 x OR*● 5 x OR●
FZH171/2.NAND33		
FZH181/4.LI30		
FZH191/3.NAND33		
FZH201/6.IN30		
FZH211/4.NAND34		
FZH231/2.NAND35		
FZH241/2.AST30	4322 026 74350	9 x
FZH251/4.AND30	4322 026 74380	{ 5 x AND 5 x OR 5 x NOR 5 x EXCLUSIVE-OR 5 x INVERTER
FZH261/2.N-4.I30		
FZH271/4.EO30		
FZH281/4.NOR30		
FZH291/4.OR30		
FZJ101/FF30	4322 026 75430	15 x
FZJ111/FF31	4322 026 75440	15 x
FZJ121/2.FF32	4322 026 74100	8 x
FZJ131/4.FF33	4322 026 74110	4 x
FZJ141/FF34	4322 026 74120	12 x
FZJ151/FF35		
FZJ161/FF36	4322 026 74360	12 x
FFK101/OS30	4322 026 75450	6 x
FZL101/ND30	4322 026 74370	12 x
TU30	4322 026 75450	10 x
2.LRD30	4322 026 75490	12 x
PA30	4322 026 75480	16 x

* With slow-down terminal.

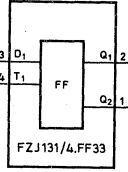
● With inverted inputs.



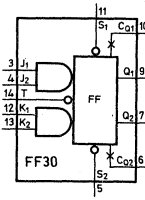
STICKERS FZ/30-Series



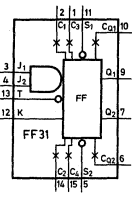
4322 026 74100



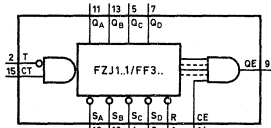
4322 026 74110



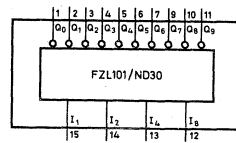
4322 026 75430



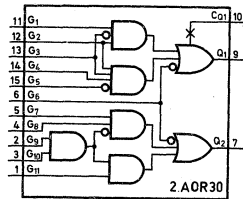
4322 026 75440



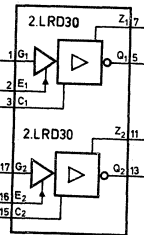
4322 026 74120



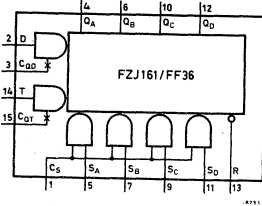
4322 026 74370



4322 026 75460

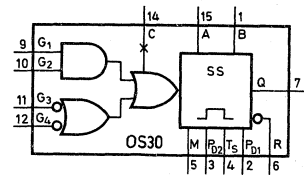


4322 026 75490



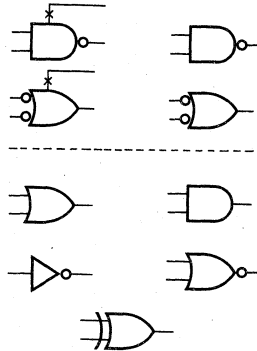
4322 026 74370

4322 026 75450

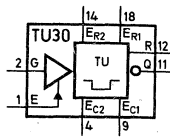


4322 026 75450

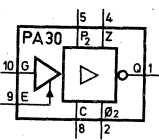
4322 026 75420



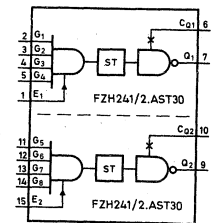
4322 026 74380



4322 026 75450



4322 026 75480



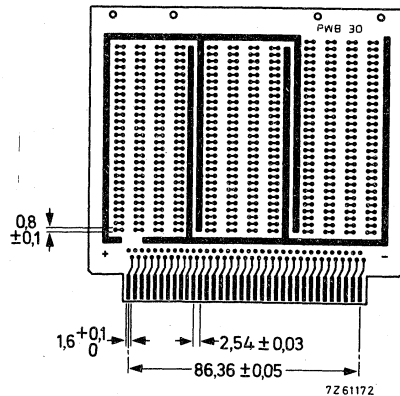
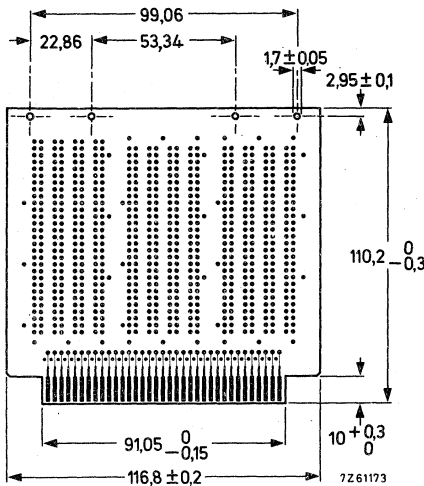
4322 026 74350

EXPERIMENTERS' PRINTED-WIRING BOARD for integrated circuits in dual-in-line package

This printed-wiring board has been designed for dual-in-line packages with a different number of pins; the packages are connected with each other and with the connector by means of insulated wires. The packages are mounted perpendicular to the connector, so the wires to the connector can run parallel to the rows of pins of the packages, instead of between the pins.

The maximum number of packages which can be mounted is given below:

number of pins of the package	max. number of packages per board
2 x 7	24
2 x 8	18
2 x 9	18
2 x 10	12
2 x 11	12



Material
Board thickness
Holes
Contact pads

glass-epoxy
1,6 mm
plated-through, 0,8 mm diameter,
provided with soldering lands
2 x 35, gold-plated

NORBITS 60-SERIES, 61-SERIES, 90-SERIES



INTRODUCTION

Our NORbits which use NOR logic as a basis of operation, represent an important advance in static switching devices for industrial control systems. The units of the 61-series facilitate using NORbits in thyristorized power control circuits; the units of the 90-series operate on the principle of trigger logic (that is, the units are driven by voltage transients in contrast with those of the 60-series which respond to voltage level), and the 90-series units allow the building of assemblies such as counters and shift registers simply and economically. They are so designed as to have a high noise immunity. However, care must be taken to avoid capacitive and inductive cross-talk between connecting wires.

The units have the following features in common:

- Single rail $24\text{ V} \pm 25\%$ supply, allowing the use of an inexpensive power supply – which helps to keep the cost down, particularly in small systems.
- Transfer moulded cases, giving optimum protection.
- Rigid terminals spaced at 0,2 in. pitch, permitting a variety of interconnection methods to be used (dip soldering, hand soldering, miniwire wrapping).
- Exceptionally good noise immunity.
- Easy to understand level logic, making it possible to carry out system tests with only a d.c. voltmeter.
- Silicon semiconductors throughout, ensuring reliable operation down to $-10\text{ }^{\circ}\text{C}$ and up to $+70\text{ }^{\circ}\text{C}$.
- Easy-to-use loading table for system design.

Compatible input and output devices as well as a full range of mounting accessories are available.

The following circuit blocks are available:

60-series *

2.NOR60	Dual 4-input NOR gate
4.NOR60	Quadruple 2 x 2 + 2 x 3 input NOR gate
2.IA60	Dual inverter amplifier
2.LPA60	Dual low power amplifier
TU60	Timer unit
2.ASF60	Dual active switch filter
HPA60	High power amplifier
GLD60	Grounded load driver

61-series *

2.NOR61	Dual NOR-gate with diode-resistor networks
RSA61	Rectifier and synchronization assembly
UPA61	Universal power amplifier
TT61	Dual thyristor trigger transformer

90-series

FF90	Flip-flop
2.TG90	Twin-trigger gate
PS90	Pulse shaper

* The types 2.SF60 (succeeded by 2.ASF60), and DOA61 are obsolete.

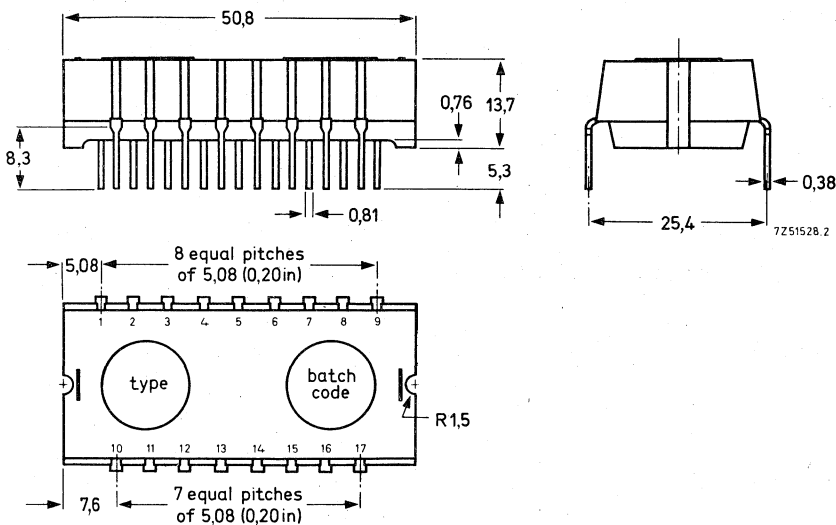
CONSTRUCTION

The circuit elements are housed in a transfer moulded encapsulation. The dimensions are as shown below. The pin connections for each unit are shown in the relevant data sheets. Pin numbering is moulded on both top and bottom of the unit. All pins are also accessible from the top of the unit to facilitate test requirements.

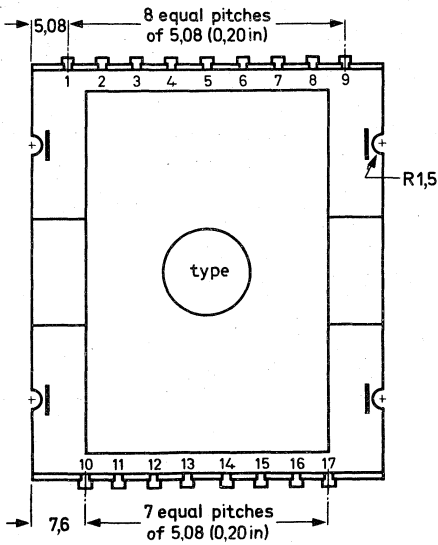
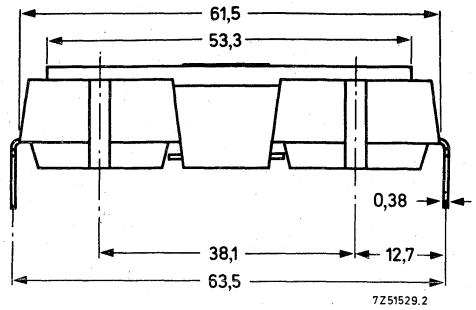
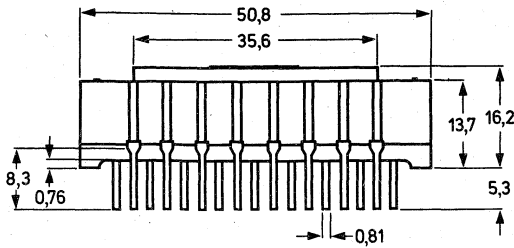
Mounting

The units may be mounted on printed-wiring boards, and a range of these is available with suitable metal mounting chassis. They may also be clamped in the moulded Universal Mounting Chassis UMC60 or fixed with 3 mm screws.

Dimensions in mm (inch equivalents within brackets).



Size A (all types except HPA60).



Size B (type HPA60).

Terminals

Wrap tool

Wrap wire size

Mass

size A

size B

Colour coding

suitable for soldering and miniwrap

Gardner Denver, bit number 506633

0,3 mm (0,012" = 28 U.S. gauge = 30 s.w.g.)

30 g approx.

85 g approx.

see data sheets of the units



CHARACTERISTICS AND DEFINITIONS

AMBIENT TEMPERATURE LIMITS

Storage

$$T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$$

Operating

$$T_{amb} = -10\text{ }^{\circ}\text{C to } +70\text{ }^{\circ}\text{C}$$

SUPPLY VOLTAGE (V_s)

Single rail, + 24 V d.c. \pm 25% (18 to 30 V) orSingle rail, + 12 V d.c. \pm 5% (11,4 to 12,6 V) at reduced ratings (except 90-series).

LOGIC LEVELS

The operation of the NORbits is based on positive logic, i.e. "1" level is a positive voltage that is more positive than "0" level, and "0" level is independent of supply voltage. Logic "1" depends upon supply and loading of the output of the logic functional block.

Levels with $V_s = 24\text{ V} \pm 25\%$

$$0\text{ V} < \text{"0"} < +0,3\text{ V}$$

$$11,4\text{ V} < \text{"1"} < V_s$$

Levels with $V_s = 12\text{ V} \pm 5\%$ *

$$0\text{ V} < \text{"0"} < +0,3\text{ V}$$

$$8,3\text{ V} < \text{"1"} < V_s$$

FAN OUT

Number of drive units that can be delivered by a logic function without exceeding the "1" level limits as defined above. The fan out actually indicates the number of NOR gates that can be driven into saturation (thereby bringing the respective outputs to "0" level).

60- AND 61-SERIES

D.C. NOISE IMMUNITY

"0" level immunity

A d.c. voltage of + 1 V with respect to the 0-volt line, applied to any one input (the other inputs floating) will not cause a change of output voltage.

"1" level immunity

- With a supply voltage of $24\text{ V} \pm 25\%$: A variation of 2 V of the "1" input level will not cause a unit to change its output voltage.
- With a supply voltage of $12\text{ V} \pm 5\%$: A variation of 0,25 V of the "1" input level will not cause a unit to change its output voltage.

DRIVE UNIT

Drive required on one input of a NOR60 (with all other inputs returned to the 0-volt line) to bring the output to "0" level (less than + 0,3 V).

* Not applicable to 90-series.

90-SERIES**TRIGGERING EDGE**

The unit FF90 is driven by a negative-going transient (from "1" to "0" level). The maximum duration of the transient, unless specified otherwise, is 3 μ s.

DRIVE UNIT (D.U.)

Drive required on reset input of FF90 to bring output Q1 to "1" level.*

ZERO UNIT (Z.U.)

Half the drive at "0" level required on one T terminal to trigger an FF90 unit.



* This drive unit has also been specified as the drive required on one input of a NOR60 (with all other inputs returned to the 0-volt line) to bring the output to "0" level.

INPUT AND OUTPUT DATA

EXTENSION OF THE DRIVE UNIT CONCEPT

System design is greatly simplified by expression of the input requirements and fan out capabilities of the various units in integral multiples of drive units (D.U.) and, for 90-series, circuit blocks also in zero units (Z.U.). To check that the loadability of a particular unit is not exceeded simply add the number of D.U.s (or Z.U.s) present at its output.

The table opposite shows the number D.U.s and Z.U.s that can be delivered by the different units of the 60 and 90-series.



LOADING TABLE

The data sheets of the units give impedances and current requirements for matching non-standard input signals to 60 and 61-series inputs as well as matching non-standard loads.

unit	input	output capability at $V_s =$		
		12 V \pm 5%	24 V \pm 25%	24 V \pm 25%
		"1" level	"1" level	"0" level
2.NOR60, per function *	1 D.U.	4 D.U.	6 D.U.	12 Z.U.
4.NOR60, per function **	1 D.U.	4 D.U.	6 D.U.	0 Z.U.
2.IA60, per function \blacktriangle	2 D.U.	13 D.U.	20 D.U.	50 Z.U.
2.IA60, connected as Low Power Amp.	2 D.U.	$R_{load} \geq 150 \Omega$	$R_{load} \geq 300 \Omega$	—
2.LPA60 per function **	2 D.U.	$R_{load} \geq 150 \Omega$	$R_{load} \geq 300 \Omega$	0 Z.U.
HPA60	1 D.U.	$R_{load} \geq 6 \Omega$	$R_{load} \geq 13,5 \Omega$	—
TU60 **	1 D.U.	3 D.U.	5 D.U.	0 Z.U.
2.ASF60, per filter **	100 V _{d.c.}	2 D.U.	2 D.U.	0 Z.U.
GLD60, NOR function GLD function	1 D.U.	—	6 D.U.	
	2 D.U.	—	900 D.U.	
PS90	—	—	6 D.U.	80 Z.U.
FF90	2 Z.U.	—	5 D.U.	7 Z.U.

* 2 inputs of the NOR must be connected in parallel. Signal must be derived from a chain of units that includes either a PS90, an FF90 or a TU60.

** No Z.U. available, therefore these units must not be used to drive an FF90 or 2.TG90 directly.

\blacktriangle IA60 driven by an IA60. Both the inverting and non-inverting connections can be used, but pins 5 and 6 must be interconnected. Signal must be derived from a chain of units that includes either a PS90, and FF90 or a TU60.

TEST SPECIFICATIONS

All units meet the following test specifications.

Test	IEC 68	MIL-STD-202C
Dry heat life test	56 days at max. diss. max. temp. check at: 0-10/14d-56d.	Method 108A, Cond. D; check at 0-10/14d-56d.
Long-term damp heat non-operating	Test C, 56 days check at 0-10/14d-56d.	Method 103B, Cond. D; check at 0-10/14d-56d.
Long-term damp heat operating	Test C, 56d. min., diss., check at 0-10/14d-56d.	Method 103B, Cond. D; check at 0-10/14d-56d.
Temp. cycle test	Test Na, 30 min., 2-3 min. in between; preferred: -40 °C; + 85 °C.	Method 107B, Cond. A; moderate temp.
Vibration	Test Fb; 10-500-10 Hz, 1 octave/min.; amplitude 0,75 mm max.; 10g max. 3 x 3 h.	Method 204A, Cond. A; 10-500-10 Hz, 15 min.; amplitude 0,75 max.; 10g max., 3 x 3 h.
Shock	—	Method 202B, 3 blows 50g.
Robustness of terminations	Test U _A + U _B .	Method 211A + (B or C).
Solderability + solder heat	Test T; at 0 h and at 56d; no electrical test.	Method 210, at 0 h and at 56d; no electrical test.
Corrosion resistance	1% SO ₂ solution, 95% R.H., 35 °C, 1 day. Recovery 27 days.	

DUAL FOUR INPUT NOR GATE

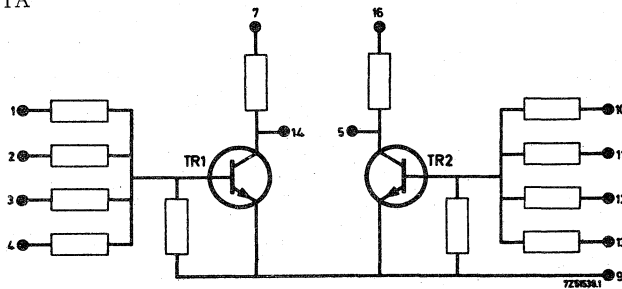
Function

dual NOR (positive logic)

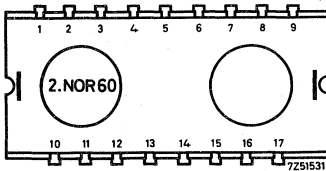
Case

size: A; colour: black

CIRCUIT DATA

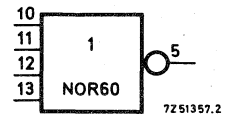
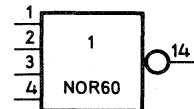


Circuit diagram



Terminal location

- 1, 2, 3, 4 = input NOR 1
- 5 = output NOR 2
- 6 = n. c.
- 7 = for supply NOR 1 (V_S)
- 8 = n. c.
- 9 = 0 V common
- 10, 11, 12, 13 = input NOR 2
- 14 = output NOR 1
- 15 = n. c.
- 16 = for supply NOR 2 (V_S)
- 17 = n. c.



Drawing symbols

The unit contains two identical transistor-resistor NOR circuits. Each circuit has 4 inputs. If any input of a NOR is at "1" level the output of that NOR will be at "0" level.

CHARACTERISTICS

	at $V_S = 24\text{ V} \pm 25\%$	at $V_S = 12\text{ V} \pm 5\%$
Supply current at V_S nom	3,5 mA	1,75 mA
at V_S max	$\leq 4,8\text{ mA}$	$\leq 1,95\text{ mA}$
Input requirement	1 D.U.	1 D.U.
Output capability	6 D.U.	4 D.U.

	single input	two paralleled inputs	three paralleled inputs	four paralleled inputs
Input impedance ¹⁾	90 k Ω	50 k Ω	35 k Ω	30 k Ω
Input current for "0" output ¹⁾²⁾	0,13 mA	0,125 mA	0,11 mA	0,1 mA

Switching speed

Fall time defined below

$$t_f \leq 1,25\ \mu\text{s}$$

Fall delay time defined below

$$t_{fd} \leq 6\ \mu\text{s}$$

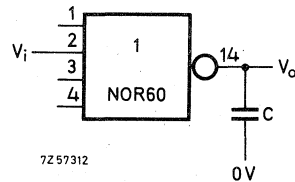
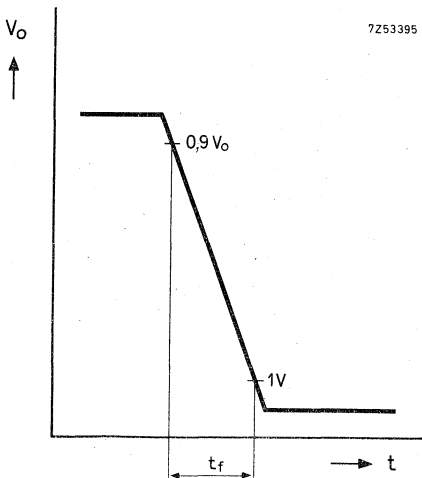


Fig.A

The fall time t_f is defined as the time required for the output voltage V_o to change from 90% of its full value to 1 V after application of a step input, the output being loaded with $C = 200\text{ pF}$ (see Fig. A).

1) Unused inputs returned to 0-volt line.

2) At $V_S = 30\text{ V}$,

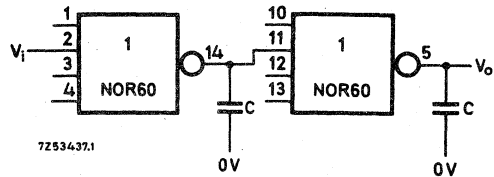
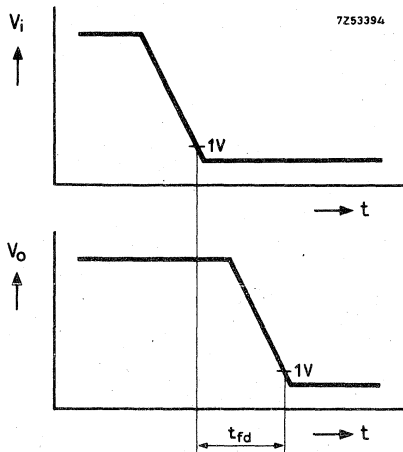


Fig.B

The fall delay time t_{fd} is defined as the time between the 1V points of the negative-going input and output voltages of two cascaded NORs, each being loaded with $C = 200$ pF (see Fig.B).

LIMITING VALUES (Destruction may occur when these values are exceeded)

Supply voltage	V_s	max. 30 V d.c. min. 0 V
Positive transient on V_s		max. 10 V during 10 μ s
Positive input voltage	$+V_i$	max. 90 V
Negative input voltage	$-V_i$	max. 18 V

QUADRUPLE 2x2 + 2x3 INPUT NOR GATE

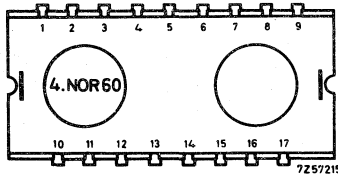
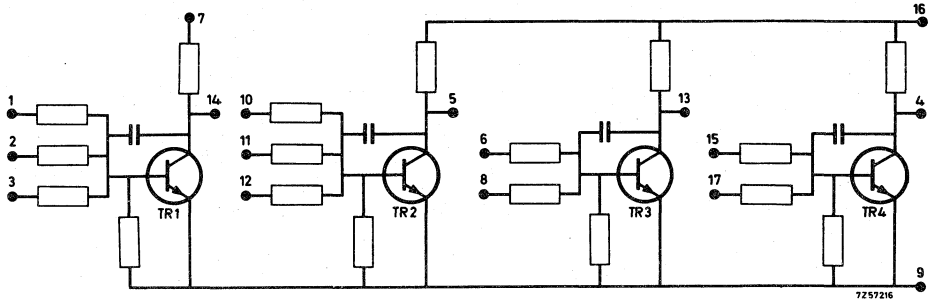
Function

quadruple NOR (positive logic)

Case

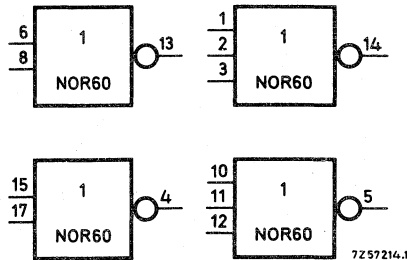
size: A; colour: black

CIRCUIT DATA



Terminal location

- 1, 2, 3 = input NOR 1
- 4 = output NOR 4
- 5 = output NOR 2
- 6, 8 = input NOR 3
- 7 = for supply NOR 1 (V_S)
- 9 = 0 V common
- 10, 11, 12 = input NOR 2
- 13 = output NOR 3
- 14 = output NOR 1
- 15, 17 = input NOR 4
- 16 = for supply NOR 2, 3, 4 (V_S)



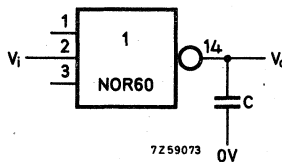
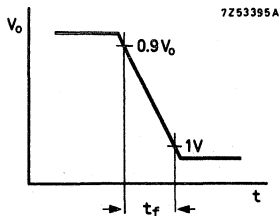
Drawing symbols

The unit contains two identical 2-input and two identical 3-input NOR circuits. If any input of a NOR is at "1" level the output of that NOR will be at "0" level.

CHARACTERISTICS

	at $V_S = 24 V \pm 25\%$	at $V_S = 12 V \pm 5\%$
Supply current at V_{Snom}	3,5 mA	1,75 mA
at V_{Smax}	$\leq 4,8$ mA	$\leq 1,95$ mA
Input requirement	1 D.U.	1 D.U.
Output capability	6 D.U.	4 D.U.

	single input	two paralleled inputs	three paralleled inputs
Input impedance ¹⁾	90 k Ω	50 k Ω	35 k Ω
Input current for "0" output ¹⁾²⁾	0,13 mA	0,125 mA	0,11 mA
Switching speed			
Fall time defined below	$t_f \leq 14 \mu s$		
Fall delay time defined below	$t_{fd} \leq 26 \mu s$		



The fall time t_f is defined as the time required for the output voltage V_0 to change from 90% of its full value to 1 V after application of a step input, the output being loaded with $C = 200$ pF (see Fig. A).

¹⁾ Not used inputs returned to 0-volt line.
²⁾ At $V_S = 30$ V.

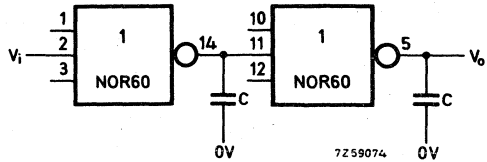
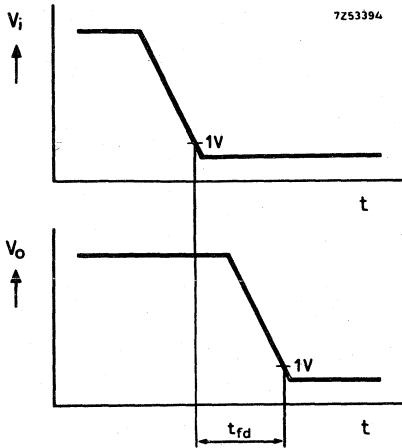


Fig.B

The fall delay time t_{fd} is defined as the time between the 1 V points of the negative-going input and output voltages of two cascaded NORs, each being loaded with $C = 200$ pF (see Fig.B).

LIMITING VALUES (Destruction may occur when these values are exceeded)

Supply voltage	V_s	max. 30 V _{d.c.} min. 0 V
Positive transient on V_s		max. 10 V for 10 μ s
Positive input voltage	$+V_i$	max. 90 V
Negative input voltage	$-V_i$	max. 24 V



DUAL INVERTER AMPLIFIER

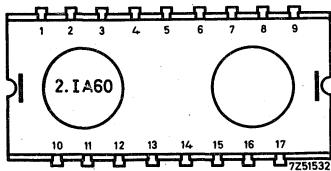
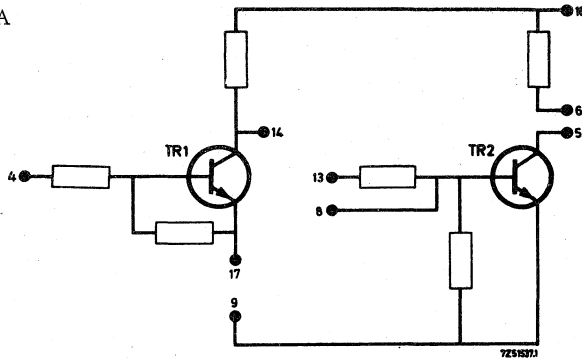
Function

The unit comprises two identical Inverter Amplifiers. Use as a single inverting Low Power Amplifier is feasible.

Case

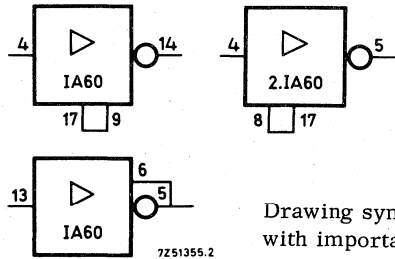
Size:A; colour: blue

CIRCUIT DATA



Terminal location

- 1, 2, 3 = n.c.
- 4 = input IA 1
- 5 = output IA 2
- 6 = collector resistor IA 2
- 7 = n.c.
- 8 = base of IA 2 transistor
- 9 = 0 V common
- 10, 11, 12 = n.c.
- 13 = input IA 2
- 14 = output IA 1



Drawing symbols with important connections

- 15 = n.c.
- 16 = for supply (V_S)
- 17 = emitter of IA 1 transistor

To obtain the dual I.A., pin 17 should be connected to pin 9 and pin 6 to pin 5. A "1" level input (pin 4 or 13) will cause a "0" level output (pin 14 or 5-6 respectively).

To obtain the inverting L.P.A., pin 17 should be connected to pin 8 and the load connected between pins 5 and 16. When pin 4 is at "1" level, pin 5 will be at "0" level.

Notes to the load of the L.P.A.

1. Care should be taken that the value of a varying load should not drop below the specified minimum.
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks upon switching off. To avoid destruction the load should be provided with a flywheeling diode, type BAX12. The anode should be connected to pin 5, the cathode to pin 16 (positive supply).

CHARACTERISTICS

	at $V_S = 24 V \pm 25\%$		at $V_S = 12 V \pm 5\%$	
	per I.A.	as L.P.A.	per I.A.	as L.P.A.
Supply current at $V_{S \text{ nom}}$	10,9 mA	10,9 mA + I_{load}	5,5 mA	5,5 mA + I_{load}
Supply current at V_S max and "1" input	$\leq 15,5 \text{ mA}$	$\leq 114 \text{ mA}$ $R_{\text{load}} = 300 \Omega$	$\leq 6,5 \text{ mA}$	$\leq 89,9 \text{ mA}$ $R_{\text{load}} = 150 \Omega$
Input requirement	2 D.U.	2 D.U.	2 D.U.	2 D.U.
Output capability	20 D.U.	140 D.U. ¹⁾	13 D.U.	
Minimum load resistance		300Ω ¹⁾		150Ω ¹⁾

Input impedance	45 k Ω
Input current for "0" output of I.A. at $V_S = 30 V$	0,285 mA
Switching speed	
Fall time defined below	$t_f \leq 1 \mu s$
Fall delay time defined below	$t_{fd} \leq 3 \mu s$

¹⁾ This load is permissible only if the input switched between "0" and "1" levels by a preceding 60 Series unit or other true digital input, avoiding excessive dissipation during transitions.

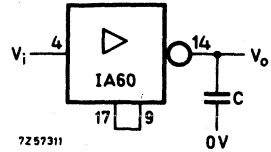
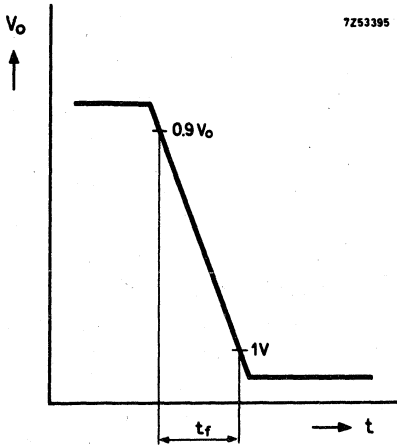


Fig.A

The fall time t_f is defined as the time required for the output voltage V_o to change from 90% of its full value to 1 V, after application of a step input, the output being loaded with $C = 200 \text{ pF}$ (see Fig.A).

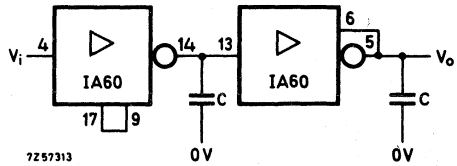
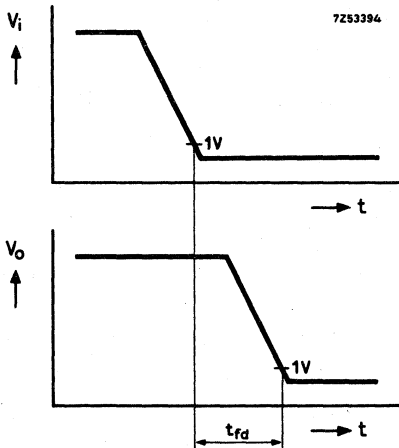


Fig.B

The fall delay time t_{fd} is defined as the time between the 1 V points of the negative-going input and output voltages of two cascaded Inverter Amplifiers, each being loaded with 200 pF (see Fig.B).

LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage	V_S	max. 30 V _{d.c.} min. 0 V
Positive transient on V_S		max. 10 V during 10 μ s
Positive input voltage	$+V_4, +V_{13}$	max. 70 V
Negative input voltage	$-V_4, -V_{13}$	max. 16 V
Positive voltage at pin 8	$+V_8$	max. 4 V via min. 500 Ω
Negative voltage at pin 8	$-V_8$	max. 5 V



DUAL LOW POWER AMPLIFIER

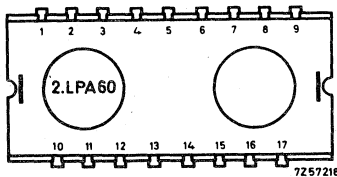
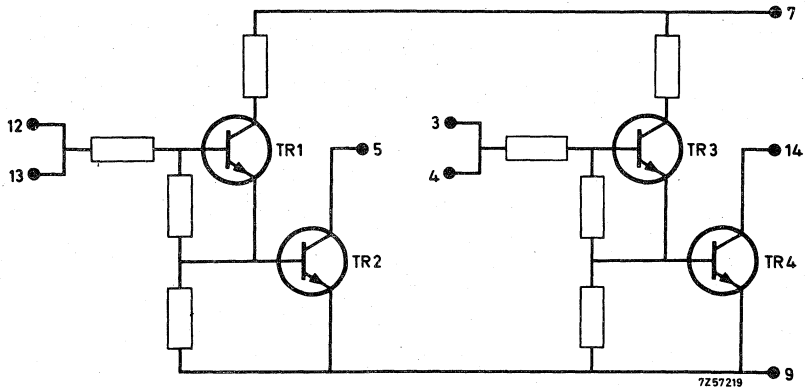
Function

The unit comprises two identical inverting
Low Power Amplifiers

Case

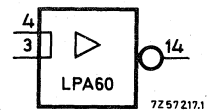
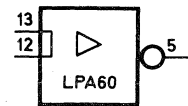
size: A; colour: blue

CIRCUIT DATA



Terminal location

- 1, 2 = n.c.
 3, 4 = input LPA2
 5 = output LPA1
 6 = n.c.
 7 = for supply (V_S)
 8 = n.c.
 9 = 0 V common
 10, 11 = n.c.
 12, 13 = input LPA1
 14 = output LPA2
 15, 16, 17 = n.c.



Drawing symbols

The load should be connected between pins 5 and 7 for LPA1 and between pins 14 and 7 for LPA2.

When the input (12/13 or 3/4) is at "1" level, the output (5 or 14) will be at less than 1 V. This being no true "0" level, it is not recommended to use an LPA as a logic operator.

Notes to the loading

1. Care should be taken that the value of a varying load should not drop below the specified minimum.
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks upon switching off. To avoid destruction the load should be provided with a flywheeling diode, type BAX12. The anode should be connected to pin 5 (14), the cathode to pin 7 (positive supply).

CHARACTERISTICS

	at $V_S = 24\text{ V} \pm 25\%$	at $V_S = 12\text{ V} \pm 5\%$
Supply current at V_S nom, $I_{load} = 0\text{ mA}$	8 mA	4 mA
Supply current at V_S max and "1" input, $R_{load} = 300\ \Omega$ $R_{load} = 150\ \Omega$	$\leq 108\text{ mA}$ -	- $\leq 89.9\text{ mA}$
Input requirement	2 D.U.	2 D.U.
Output capability	100 mA	80 mA
Min. load resistance	300 Ω	150 Ω
Input impedance		45 k Ω
Input current for "0" output at $V_S = 30\text{ V}$		0.285 mA
Output voltage at "1" input		< 1 V
Switching speed		
Fall time (Fig. A)	t_f	$\leq 0.4\ \mu\text{s}$
Rise time (Fig. B and Fig. C)	t_r	$\leq 2\ \mu\text{s}$
Storage time (Fig. B and Fig. C)	t_s	$\leq 10\ \mu\text{s}$

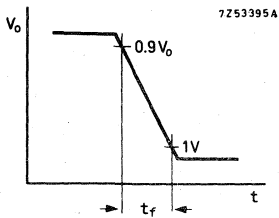


Fig. A

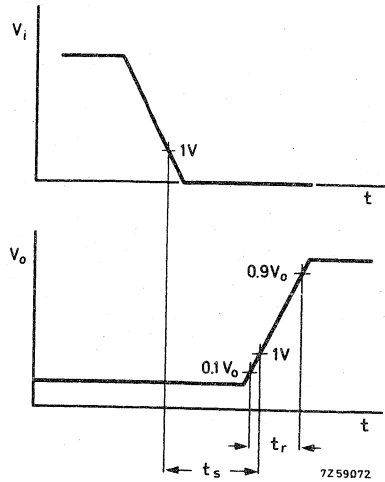


Fig. B

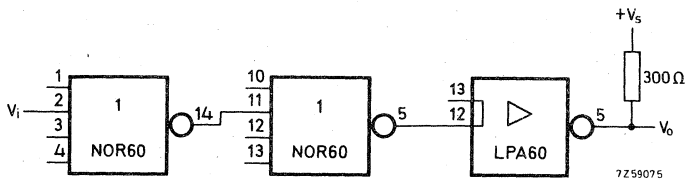


Fig. C

LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage	V_s	max. 30 V _{d.c.}
		min. 0 V
Positive transient on V_s		max. 10 V for 10 μ s
Positive input voltage	$+V_i$	max. 70 V
Negative input voltage	$-V_i$	max. 16 V

TIMER

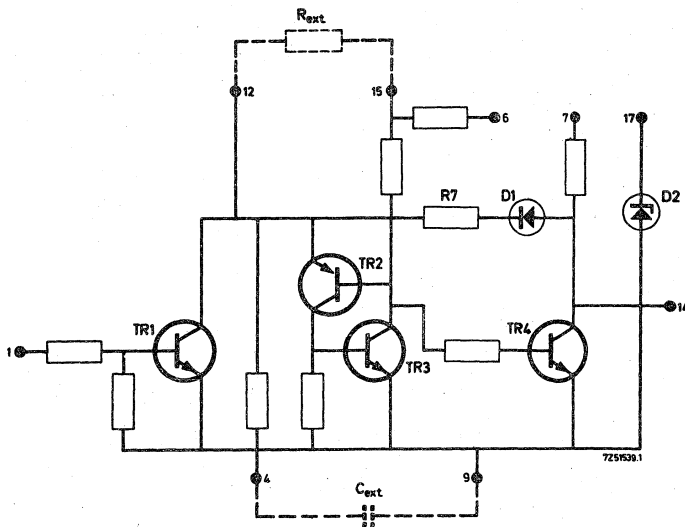
Function

Gives an inverted output. The output of a "1" is delayed following a "0" input. No delay occurs when the input returns to "1"

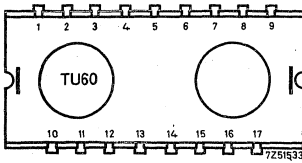
Case

Size: A; colour: red

CIRCUIT DATA

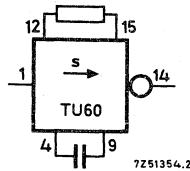


With the input at "1" the capacitor (C_{ext}) is discharged. When the input goes to "0", TR_1 ceases to conduct so that the capacitor is allowed to slowly charge until the base potential of TR_2 is exceeded. TR_2 starts to conduct and provides base current for TR_3 , which speeds the turn-on of TR_2 . TR_4 ceases to conduct and the output level changes from "0" to "1". Positive feedback is provided via D_1 and R_7 .



Terminal location

- 1 = input
- 2, 3 = n.c.
- 4 = for external capacitor
- 5 = n.c.
- 6 = see instructions below
- 7 = positive supply
- 8 = n.c.
- 9 = 0 V common
- 10, 11 = n.c.
- 12 = for external resistor
- 13 = n.c.
- 14 = output
- 15 = for external resistor
- 16 = n.c.
- 17 = see instructions below



Drawing symbol with significant connections

Instructions for connection of the supply

When $V_S = 24 V \pm 25\%$: connect 6 and 7,
connect 15 and 17.

When $V_S = 12 V \pm 5\%$: connect 15 and 7,
do not connect 6 and 7.

CHARACTERISTICS

Supply current at $V_{S \text{ nom}}$
at $V_{S \text{ max}}$

Input requirement

Output capability

Input impedance

Input current for "0" output,
at $V_S = 30 V$

External resistance

	at $V_S = 24 V \pm 25\%$	at $V_S = 12 V \pm 5\%$
Supply current at $V_{S \text{ nom}}$	6.9 mA	1.9 mA
at $V_{S \text{ max}}$	10.1 mA	2.1 mA
Input requirement	1 D.U.	1 D.U.
Output capability	5 D.U.	3 D.U.

90 k Ω

0.125 mA

R_{ext} min. 100 k Ω , max. 1 M Ω

Leakage current of external
capacitor when connected between

pins 4 and 9

pins 15(+) and 4

max. 100 nA at 10 V

max. 100 μ A at 25 V

Delay time (see Fig.A)	t_{delay} about $R_{\text{ext}} C_{\text{ext}} s (M\Omega \times \mu F)^1$
Max. change of delay time with temperature (C_{ext} pins 4 and 9)	- 0,14 %/°C
Switching speed	
Fall time as defined below	$t_f \leq 1 \mu s$
Rise time as defined below	$t_r \leq 6 \mu s$
Timing requirements (see Fig.A)	
Set time	t_{set} min. 11,9 C_{ext} ms (C_{ext} in μF)
Recovery time	t_{rec} min. 11,9 C_{ext} ms
Start inhibit before end of delay	$t_{\text{st inh}}$ min. 18,9 C_{ext} ms
Inhibit duration	t_{inh} min. 18,9 C_{ext} ms (A shorter t_{inh} gives a shorter delay)

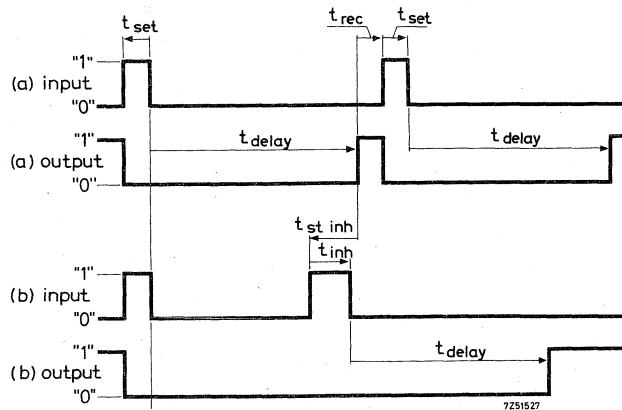


Fig.A

1) For long delay times the 25 μF , 160 V_{RMS} film capacitor, catalogue number 2222 325 50256 is recommended.

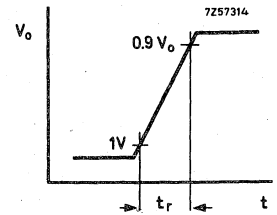
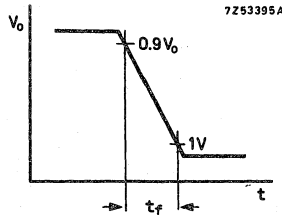
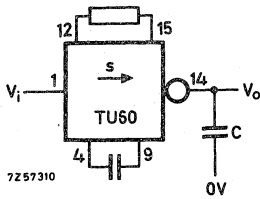


Fig.B

The fall time t_f is defined as the time required for the output voltage V_o to change from 90% of its full value to 1V, after application of a step input and being loaded with $C = 200$ pF (see Fig.B).

The rise time t_r is defined as the time required for the output voltage V_o to change from 1 V to 90% of its full value, after application of a step input and being loaded with $C = 200$ pF (see Fig.B).

LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply	V_s	max. 30 V d.c. min. 0 V
Positive transient on V_s		max. 10 V for 10 μ s
Positive input voltage	$+V_1$	max. 70 V
Negative input voltage	$-V_1$	max. 16 V
External resistance	R_{ext}	min. 820 Ω

DUAL ACTIVE SWITCH FILTER

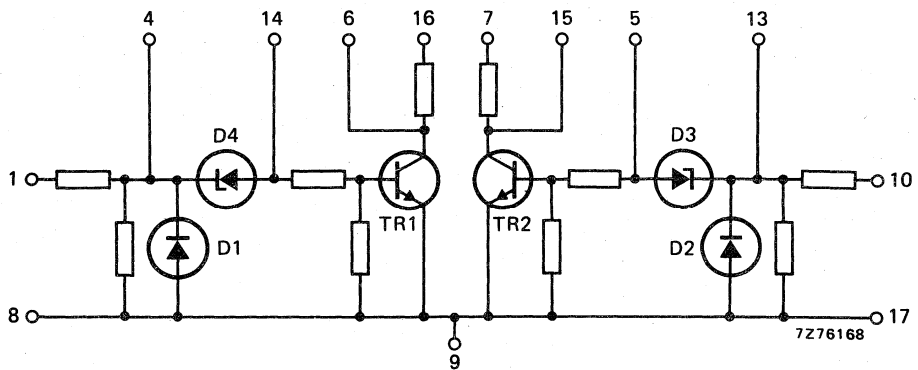
Function

For suppression of interference and to eliminate the effects of contact bounce occurring on mechanical switches.

Case

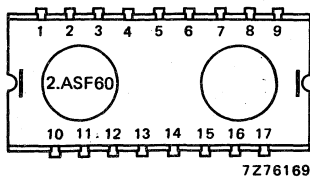
size : A ; colour : black.

CIRCUIT DATA

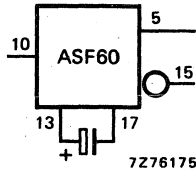
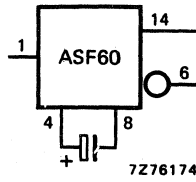


The unit consists of two identical, electrically independent filter circuits, both using an external capacitor. A high voltage is used to break down the contact film resistance of external switches. Non-inverted and inverted outputs are available from each filter, the latter with an increased drive capability.

Terminal location



- | | |
|------------------------------------|-------------------------------------|
| 1 = input ASF1 | 10 = input ASF2 |
| 2, 3 = not connected | 11, 12 = not connected |
| 4 = for external capacitor of ASF1 | 13 = for external capacitor of ASF2 |
| 5 = output ASF2 | 14 = output ASF1 |
| 6 = inverted output ASF1 | 15 = inverted output ASF2 |
| 7 = supply (V_S) ASF2 | 16 = supply (V_S) ASF1 |
| 8 = 0 V for external C | 17 = 0 V for external C |
| 9 = 0 V common | |



Drawing symbols with external capacitor

CHARACTERISTICS (per filter)

Supply voltage (V_S) current	+24 V \pm 25% or +12 V \pm 5% max. 4,8 mA and max. 2,0 mA respectively
Input voltage, logic 1 logic 0	+100 V \pm 25% max. +7,5 V, nom. 0 V
Input current, steady surge peak	max. 3,5 mA max. 4,8 mA
Output capability, - non-inverting outputs (pin 5 or 14) - inverting outputs (pin 15 or 6) pin(s) 7 and/or 16 not connected	2 D.U. 6 D.U. 10 mA sink

The output will switch when the input has been applied for longer than the time shown under "Operation" on next page.

LIMITING VALUES (Destruction may occur if these values are exceeded)

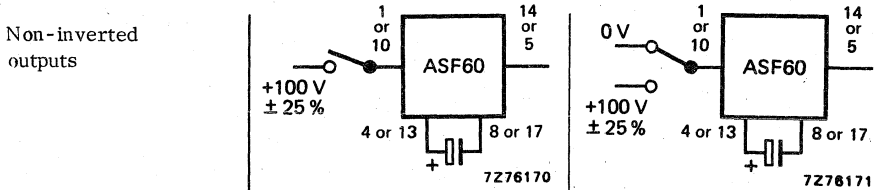
Positive input voltage	+ max. 125 V
Negative input voltage	-max. 125 V

INSTRUCTIONS

- a. Mount the unit as close as possible to the logic system input.
- b. The common 0-volt line (pin 9) must be returned to the central earth point of the system to avoid common impedance coupling.

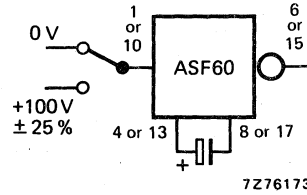
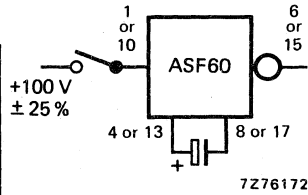
OPERATION

The external capacitor (C) should be connected between the appropriate terminals 4 or 13 and the 0 V terminals 8 or 17. The use of a 100 V electrolytic capacitor is recommended, and its value C in μF may be obtained from the formulae below.



type of contact	single pole/single throw	single pole/double throw
Tolerable contact bounce time	max. $1,4C$ ms	max. $1,4C$ ms
Frequency of operation with 1:1 mark/space ratio	max. $\frac{6,3}{C}$ Hz	max. $\frac{10,6}{C}$ Hz
Time for which input must be at logic '1' to ensure '1' out	min. $42C$ ms	min. $42C$ ms
Time for which input must be disconnected (or at 0 V) to ensure '0' out	min. $26C$ ms	min. $18C$ ms

Inverted outputs



type of contact	single pole/single throw	single pole/double throw
Tolerable contact bounce time	max. 1,4C ms	max. 1,4C ms
Frequency of operation with 1:1 mark/space ratio	max. $\frac{5,7}{C}$ Hz	max. $\frac{10,6}{C}$ Hz
Time for which input must be at logic '1' to ensure '0' out	min. 29C ms	min. 29C ms
Time for which input must be disconnected (or at 0 V) to ensure '1' out	min. 87C ms	min. 45C ms



HIGH POWER AMPLIFIER

Function

Power Amplifier for load switching

Case

Size: B; colour: black

CIRCUIT DATA

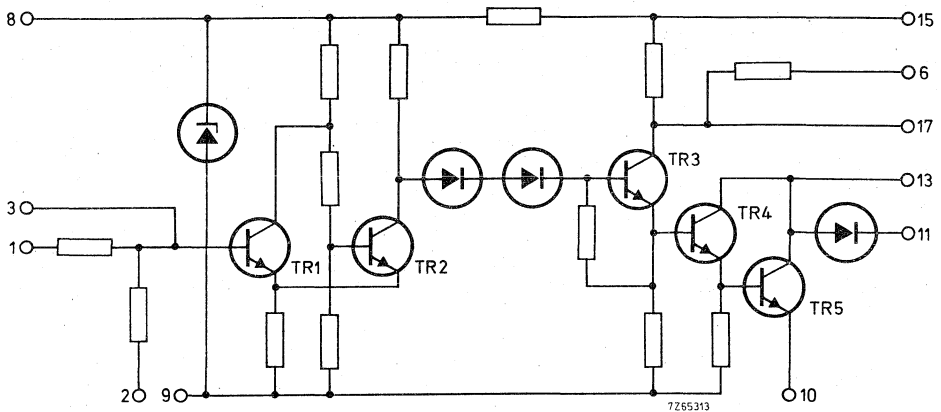


Fig. 1

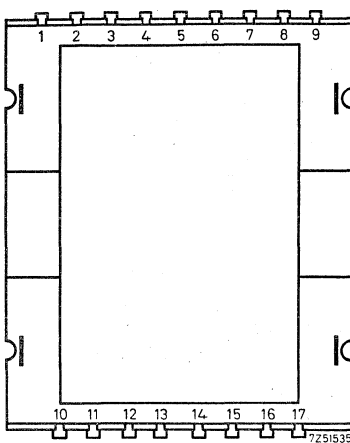
The power amplifier consists of a Schmitt trigger followed by a buffer + driver stage, which provides adequate drive to the power transistor under all conditions of permissible supply voltage and input signal. The load should be connected between pin 13 and + of power supply. A "1" input will switch on the load current.

Notes:

1. Observe rules for $R_{load\ min}$.
2. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from voltage and current so that turning on of a lamp may cause a current surge. It is often advisable to use a preheating quiescent current to eliminate destructive surge currents.
3. Inductive loads will cause large voltage peaks at switching off. To avoid destruction of output transistor the load should be shunted by a damping diode. By connecting terminal 11 to the supply line inductive loads up to a certain value can be handled by the internal diode.

4. Pin 10 serves to make a separate connection between a 0 V load supply line and the power supply unit to avoid common wire impedance with the 0 V logic supply line. Also, if a second supply unit is used for the HPA 60, common impedance with the 0 V logic supply line should be avoided in the interconnection between pins 9 (0 V logic supply) and 10 (0 V output stage).

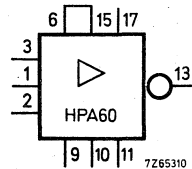
Terminal location



- 1 = input
- 2 = base resistor of input transistor
- 3 = base of input transistor
- 4 = n.c.
- 5 = n.c.
- 6 = + supply, connect to 15
- 7 = n.c.
- 8 = zener diode
- 9 = 0 V logic supply
- 10 = 0 V output stage, see note 4
- 11 = damping diode
- 12 = n.c.
- 13 = output (load between 13 and supply)
- 14 = n.c.
- 15 = + supply, connect to 6
- 16 = n.c.
- 17 = collector of TR3

Fig. 2

Fig. 3
Drawing symbol (one necessary interconnection indicated).



Additional instructions

- a. If the input (pin 1) is driven by a standard "1" level from NOR 60, etc., connect pins 2 and 9.
- b. If the supply voltage is $12\text{ V} \pm 5\%$, connect a resistor of $330\ \Omega$ between pin 6 and 8, and a resistor of $1.5\ \text{k}\Omega$ between 15 and 17; both resistors $\pm 5\%$, $\frac{1}{4}\ \text{W}$.
- c. Wiring to pin 3 must be kept remote from the output circuitry.
- d. When using pin 3 as a second input, the input resistor should be connected direct to the pin.

CHARACTERISTICS

	$V_S = 24 \text{ V} \pm 25\%$	$V_S = 12 \text{ V} \pm 5\%$
Supply current at V_S nom excluding I_{load}	18.8 mA	15.1 mA
Supply current at V_S max excluding I_{load}	< 26.2 mA	< 28.8 mA
Required load resistance at $T_{amb} = 45$ to $70 \text{ }^\circ\text{C}$	> 13.5 Ω	> 6 Ω
at $T_{amb} < 45 \text{ }^\circ\text{C}$	> 12 Ω	> 5 Ω
Required input	1 D.U.	1 D.U.
Voltage on pin 13, TR5 conducting	max. 2.V	max. 2 V
	<u>at pin 1</u>	<u>at pin 3</u>
For switching on load current		
input voltage, 2-9 connected	> 6 V	> 1.6 V ¹⁾
input current, 2-9 connected	75 μA	75 μA
2-9 not connected ²⁾	30 μA	30 μA
For switching off load current		
input voltage, 2-9 not connected ²⁾	< 1.15 V	< 1.15 V
On-off input voltage difference		
2-9 not connected ²⁾	-	> 0.5 V
Switching speed	<u>maximum</u>	<u>typical</u>
Fall time, t_f	0.2 μs	0.05 μs
Rise time, t_r	4.2 μs	0.3 μs

The fall time t_f is defined as the time required for the output voltage to change from 90% to 10% of its full value, after application of a step input, under conditions as shown in Fig. 4 (See also Fig. 5).

The rise time t_r is defined as the time required for the output voltage to change from 10% to 90% of its full value, after application of a step input, under conditions as shown in Fig. 4 (See also Fig. 6).

1) Via min. 500 Ω .2) Source resistance must not exceed 56 k Ω .

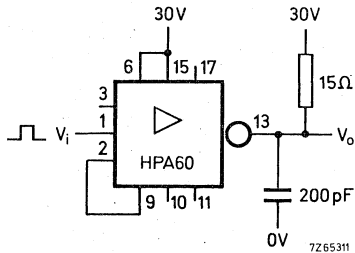


Fig. 4

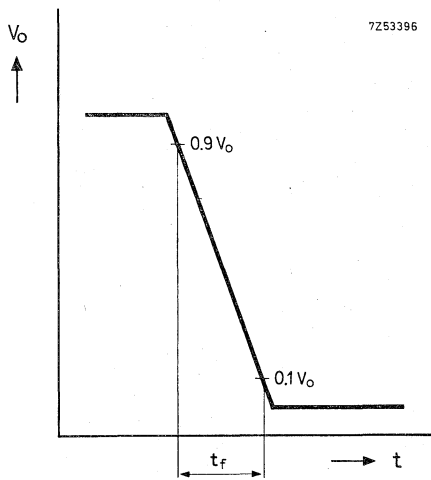


Fig. 5

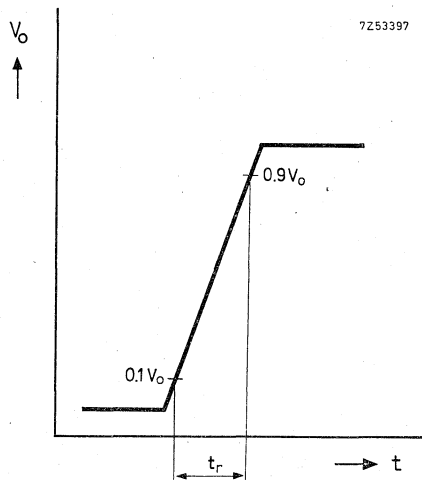


Fig. 6

By connecting terminal 11 to the supply line the following inductive loads can be handled by the internal damping diode:

$$R_L = 15 \Omega$$

$$L_L \leq 10 \text{ H}$$

$$R_L = 20 \Omega$$

$$L_L \leq 14 \text{ H}$$

$$R_L = 30 \Omega$$

no restriction

Switch-off delay time for $R_L = 30 \Omega$ and $L_L = 10 \text{ H}$ is 770 ms.

LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage, V_S	max. 30 V d.c.
Positive transient on driver stage (pin 6 and 15)	max. 10 V for 10 μ s
Positive voltage on power stage, pin 13	max. 55 V
Voltage at pin 1 (2-9 connected)	
positive	max. 100 V
negative	max. 15 V
Voltage at pin 3	
positive	max. 5 V via min. 500 Ω
negative	max. 4.5 V
Output current	5 A for 20 ms

OVERLOAD PROTECTION

Protection measures must be taken in applications in which overloading of the HPA 60 may occur, e.g. short circuiting of the load. The operating time of a fuse is far too slow to provide adequate protection in such cases, therefore another method must be used. The protection circuit described here uses a 2.IA 60 connected as a memory element, and serves well in many HPA 60 applications.

It will operate at a load current of 3 A. Removing one of two series-connected diodes will bring the "fault" condition of load current down to 2 A. Finer control of the load current level at which the protection circuit will operate may be achieved by replacing the resistor R by a wire-wound potentiometer.

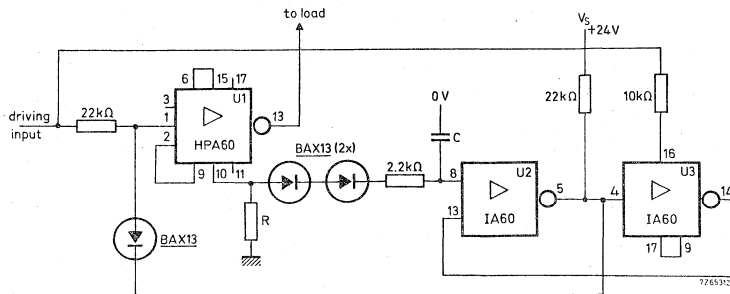


Fig. 7

$$R = 0,39 \Omega (2 W)$$

$$C = 100 \text{ nF}$$

Load current information is provided by resistor R, and is fed to U2 (pin 8) via the series-connected diodes.

The capacitor C prevents the circuit from operating on transient currents of up to 5 A. If the load current is too high for the HPA 60, the output of U2, at pin 5, goes LOW. This LOW is fed back to U1, pin 1, via the BAX13 diode. A LOW at the input of the HPA 60 switches it off.

When the overload is removed, the protection circuit remains in the fault condition because the memory element is still "set". The protection circuit can only be "reset" by removing the logic signal from the driving input, since U3 is fed with the HPA 60 driving input via pin 16.

The circuit shown here requires 6 D.U.

GROUNDING LOAD DRIVER

Function: - a 2 input power amplifier for switching d.c. loads, connected with one side to ground (GLD)
 - a 2 input NOR gate
 - monitor circuit for twin channel logic systems with fault display.

Case: Norbit block size A, colour black.

CIRCUIT DATA

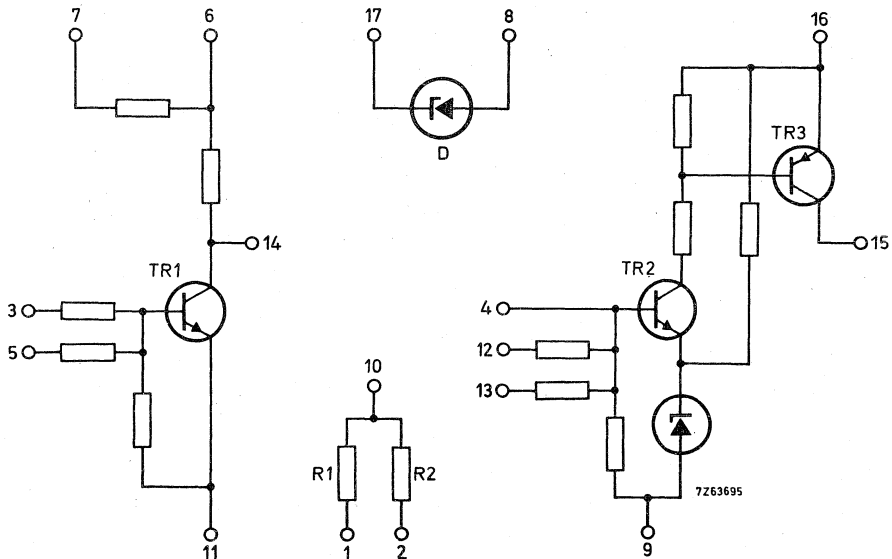


Fig. 1

The unit comprises two main circuits and auxiliary networks:

- A NOR gate with two inputs each requiring 1 D.U.. The output capability is 6 D.U..
- A grounded load driver (GLD) consisting of an input stage with two inputs and a PNP output stage. The load should be connected between the output terminal and 0 V common. A "1" input signal will switch on the load current.
- A voltage regulator diode (D) to couple the NOR to the GLD, or to isolate the load of the GLD from the resistance network (R1 and R2) when the complete unit is applied as a monitor circuit for twin channel logic systems with fault display.

Terminal location

- | | |
|------------------------------------|---------------------------------------|
| 1 = R1 | 10 = R1, R2 |
| 2 = R2 | 11 = emitter TR1, 0 V if used as NOR |
| 3 = input NOR | 12 = input GLD |
| 4 = auxiliary input GLD | 13 = input GLD |
| 5 = input NOR | 14 = output NOR |
| 6 = positive supply V_S for NOR | 15 = output GLD |
| 7 = auxiliary supply | 16 = positive supply V_S for GLD |
| 8 = voltage regulator diode, anode | 17 = voltage regulator diode, cathode |
| 9 = 0 V common GLD | |

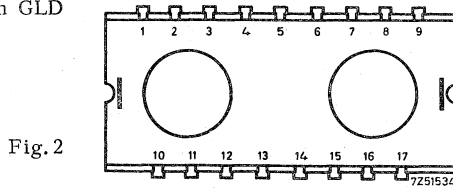


Fig. 2

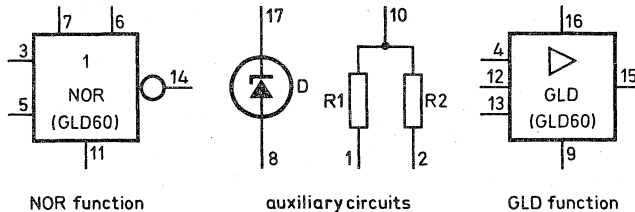
Drawing symbols

Fig. 3 NOR function

auxiliary circuits

GLD function

CHARACTERISTICS

7263686

	NOR (supply to pin 6)	GLD
Power supply voltage (V_S) current	+24 V \pm 25 % nom. 3, 2 mA max. 4, 1 mA	+24 V \pm 25 % nom. 14, 2 mA + I_{load} max. 19, 1 mA + I_{load}
Input requirements, per terminal	1 D.U.	2 D.U.
Output capability at maximum load resistance	6 D.U.	900 D.U. 3 k Ω
Minimum load resistance, - driven by signal on pins 12 and 13		75 Ω *) at $T_{amb} = 45$ $^{\circ}$ C 86 Ω *) at $T_{amb} = 70$ $^{\circ}$ C
- driven by NOR via D on pin 4 (supply to pins 7 and 16, connect pin 8 to 4, pin 14 to 17, pin 11 to 10, pin 12 or 13 to 0 V)		120 Ω *)

- *) For use with incandescent lamps, series and/or bleed resistors might be required to avoid high inrush currents in connection with their "cold" resistance.
To limit large voltage peaks at switching of inductive loads these loads should be shunted by a damping diode, e. g. BAX12 (cathode to pin 15).

Resistor network

R1	3010 Ω
R2	1500 Ω

Voltage regulator diode

V_D	12 V
-------	------

LIMITING VALUES (Destruction may occur if these values are exceeded)

Supply voltage V_S	max. +30 V d.c. min. 0 V d.c.
Positive transient on V_S	max. +10 V for 10 μ s
Input voltage NOR (pins 3, 5)	max. +70 V min. -15 V
GLD (pins 12, 13)	max. +70 V min. -4 V
Input current GLD (pin 4)	max. +20 mA *
Output surge current	max. 1 A for 20 ms

APPLICATION INFORMATIONA. GLD60 as a grounded load amplifier

1. The GLD 60 makes it possible to drive loads (relays, magnetic valves etc.) of which one side has been connected to ground, Fig. 4 illustrates also the suitability of the unit for systems which from the point of safety require that the load is not activated in case of short circuit to ground of the output.

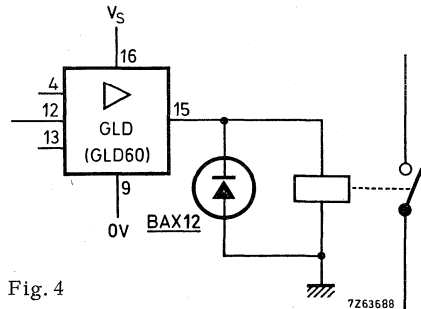


Fig. 4

2. High power grounded load drive.
Fig. 5 shows how higher loads can be driven. This circuit permits load resistances down to 8,6 Ω (corresponding to a load current of 3,5 A at $V_S = 30$ V).
The BDY60 is mounted on an aluminium heatsink of 150 cm², thickness 2 mm.
For inductive loads a flywheel diode D (BYX30/50) is required.

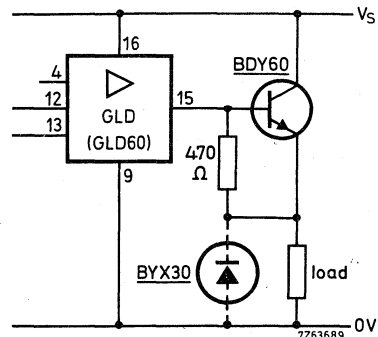


Fig. 5

*) Care should be taken not to apply a voltage > 1 V without current limiting resistance.

3. Short circuit protection of the GLD60.

If the load is short-circuited, the output transistor of the GLD60 can be damaged. This is prevented if the circuit depicted in Fig.6 is applied. Too high a load current starts the BRY39 conducting. Consequently the input of the NOR goes "high" and its output "low", biasing input 4 of the GLD "low", in this way overruling the existing "high" on the system inputs. Once the BRY39 has started conducting, it will continue to do so until the push button is pressed.

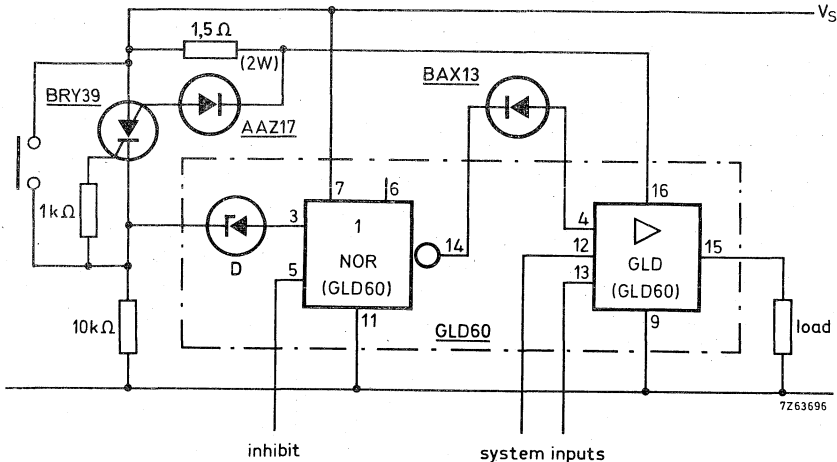


Fig. 6

B Monitoring and safeguarding twin channel systems

Fig. 7 shows the circuit build-up of a process control in which malfunctioning of one of the parallel identical logic systems or of the monitoring/safeguarding circuit causes an indication or switching to safe condition of the process to be controlled. When the identical logic systems function properly their outputs are equal because their input conditions are identical. The equality of the outputs is monitored by the combination "2 x GLD60". Where parts of this monitoring combination are used in the channels before the point of comparison, they should be completely independent so that malfunction of one part in one channel cannot cause malfunction of the other part in the other channel. Consequently malfunction in this part of the monitoring combination will occur in one channel only and will have the same effect as malfunction of one of the logic systems. Similar considerations apply to the input connections of both logic systems.

Output V_{OA} can be used for power switching, and as an input condition for additional twin-channels (e. g. B_1 and B_2) in case the total control system comprises more twin channels.

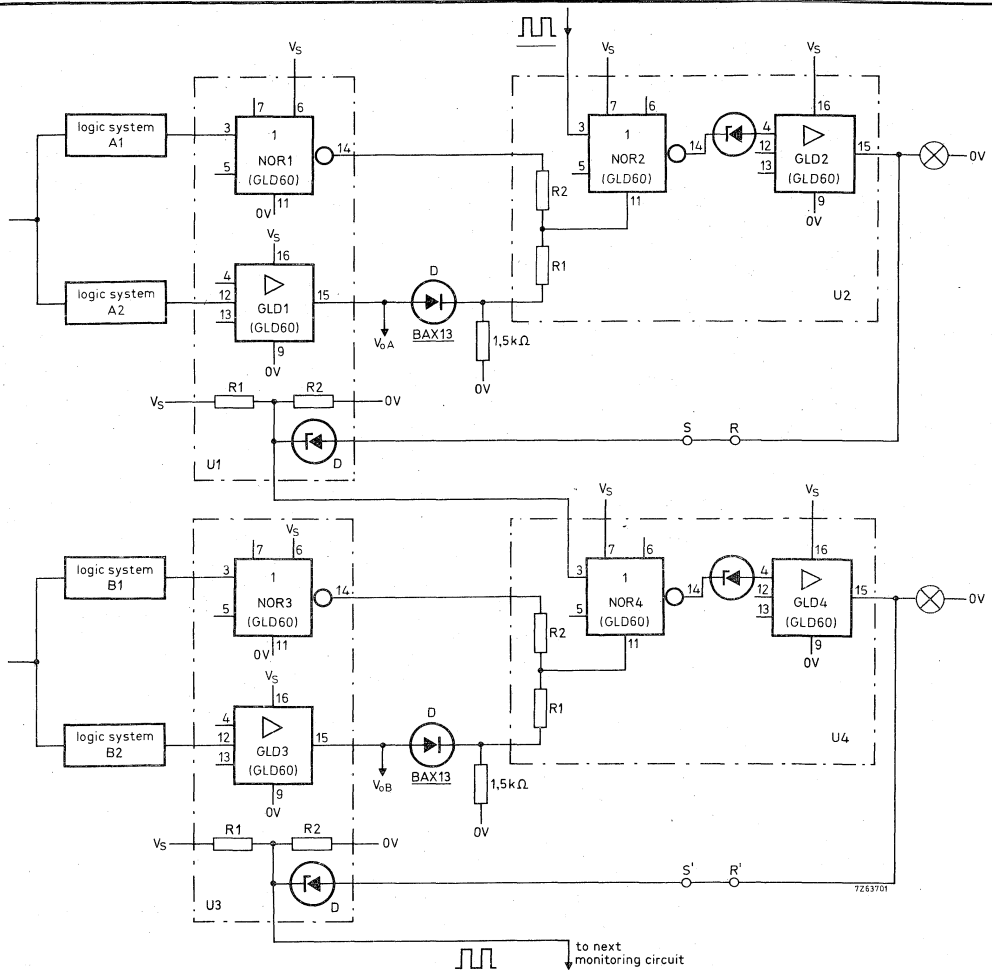


Fig. 7

The actual circuit for comparing the outputs should be self-safeguarding which means that a malfunction should cause a fault indication, i.e. the part of the monitoring circuit between comparison circuit and pilot lamp has also to be monitored for malfunction. This is done by feeding a square wave to the input of this part, which is therefore monitored in a dynamic way. The output will alternate between on and off at the frequency of the square wave.

Malfunction of one of the components will cause a continuous on or off at the output. This also means that the pilot lamp is continuously monitored. Correct functioning of the whole system causes the pilot lamp to flicker (low square wave frequency e.g. 2 Hz) or to burn dimly (high square wave frequency e.g. 10 kHz).

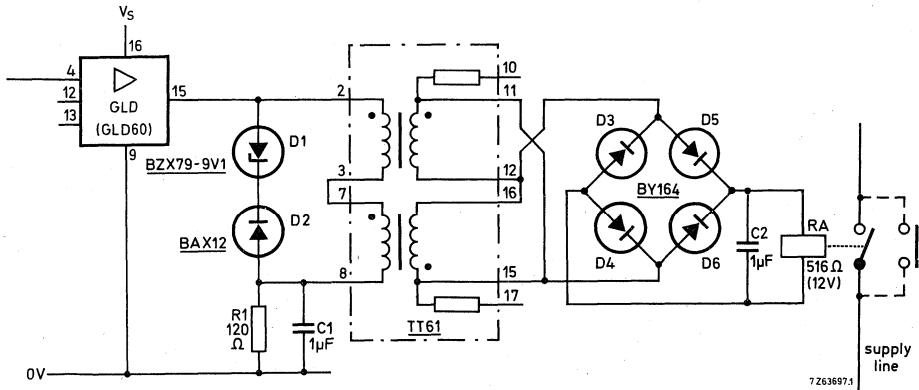


Fig. 8

The high frequency wave output can also be fed via a transformer to a rectifier, see Fig. 8. Thus only a square wave output will cause a d.c. voltage which can be used to activate a relay. Any malfunction in the whole system will cause the relay to fall off and thereby switch the system to be controlled to a safe condition.

Note that if only one twin channel system has to be monitored or safeguarded the resistor of 1,5 kΩ and external diode BAX13 (Fig. 7) can be replaced by R2 and the voltage regulator diode inside unit U1.

The square wave interrogating signal fed to the monitor circuit should be symmetrical and vary between $V_s/3$ and V_s . Fig. 9 shows a suitable generator. The symmetry and the frequency are adjusted by means of the 10 kΩ potentiometer and the capacitor C respectively. Cycle time $T = 1,5 C$ ms approximately (C in μF).

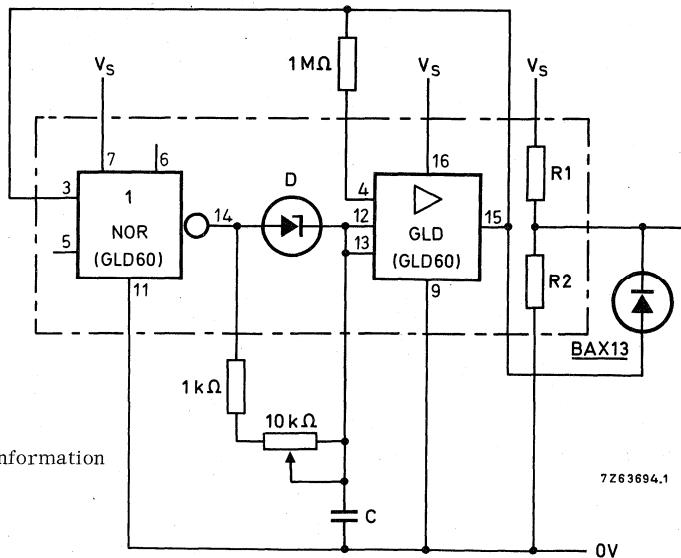


Fig. 9
Extended application information is given in A.I. 348.

7Z63694.1

UNIVERSAL POWER AMPLIFIER

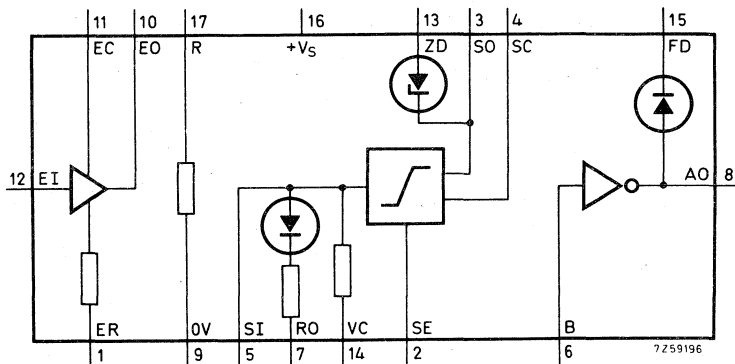
Function

1. D.C. switching amplifier.
2. Power oscillator for driving thyristor trigger transformers.
3. Phase shift module.
4. Current source for linear capacitor discharging.

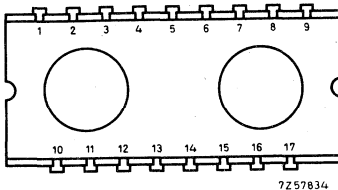
Case

Size: A; Colour: black.

CIRCUIT DATA



Quick reference circuit diagram

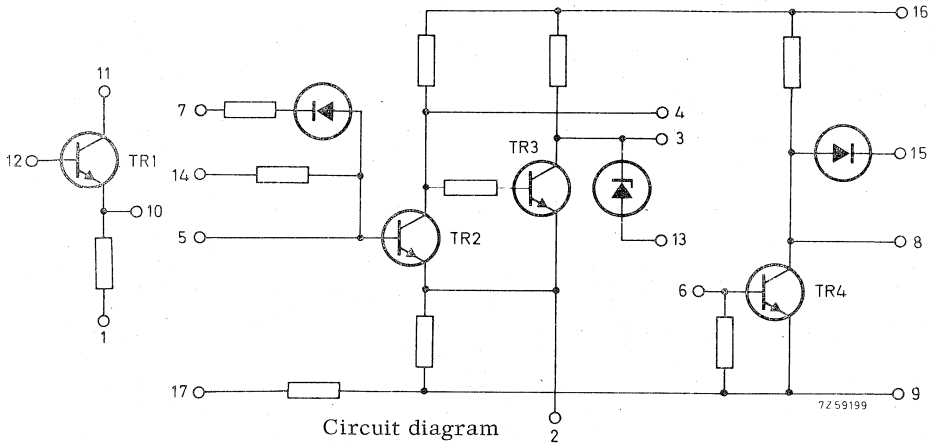


Terminal location

- 1 = emitter resistance follower
- 2 = emitter output Schmitt trigger
- 3 = output Schmitt trigger
- 4 = complementary output Schmitt trigger
- 5 = Schmitt trigger base input
- 6 = power stage base input
- 7 = oscillator feedback input
- 8 = power stage output
- 9 = 0 V common
- 10 = output emitter follower
- 11 = collector emitter follower
- 12 = base emitter follower
- 13 = restored "0" output Schmitt trigger
- 14 = input Schmitt trigger
- 15 = damping diode power stage
- 16 = supply voltage $+V_S$
- 17 = auxiliary resistor

Notes

1. For applications as a power amplifier with a min. permissible load resistance of 90Ω , connect pin 13 to pin 6. A "1" at pin 14 will switch on the load between pins 8 and 16.
2. For applications as a power amplifier with a min. permissible load resistance of 30Ω , connect pin 12, 13, 17 and 1 together, connect pin 10 to 6, and connect pin 11 to V_S via a resistor of 330Ω , (2, 5 W).
A "1" at pin 14 will switch on the load between pin 8 and 16.
3. The load should be connected between pins 8 and 16. To avoid destruction resulting from large voltage peaks occurring at switching off of inductive loads, the damping diode in the circuit block has to be connected across the load (15 to 16).
4. Incandescent lamps have a "cold" resistance that is only a fraction of the value calculated from nominal voltage and current, so that turning on of the lamp may cause a surge current. It is advisable to use a pre-heating quiescent current to eliminate destructive surge currents.



CHARACTERISTICS

Pins 6 and 13 connected, unless otherwise specified.

Supply

Supply current at
 $I_{load} = 0 \text{ mA}$

Supply current at
"1" input (pin 14) *)

$V_S = 30 \text{ V}$, $R_{load} = 30 \Omega$

	at $V_S = +24 \text{ V} \pm 25\%$	at $V_S = +12 \text{ V} \pm 5\%$
Supply current at $I_{load} = 0 \text{ mA}$	$\leq 110 \text{ mA}$	$\leq 9 \text{ mA}$
Supply current at "1" input (pin 14) *) $V_S = 30 \text{ V}$, $R_{load} = 30 \Omega$	1100 mA	

*) Connections as in Note 2 above.

Input	at $V_S = +24 \text{ V} \pm 25\%$	at $V_S = +12 \text{ V} \pm 5\%$
Drive at pin 14 for switching on load current	2 D.U.	2 D.U.
Input impedance at pin 14	92 k Ω	92 k Ω
Input voltage for switching on load current at pin 5 **)	$\geq 8.2 \text{ V}$	$\geq 4 \text{ V}$
at pin 14	$\geq 11.4 \text{ V}$	$\geq 5.3 \text{ V}$
Input voltage for switching off load current at pin 5 **)	$\leq 1.6 \text{ V}$	$\leq 1 \text{ V}$
at pin 14	$\leq 1.8 \text{ V}$	$\leq 1.2 \text{ V}$
On-off input voltage difference, $R_{\text{source}} = 2200 \Omega$, at pin 5	$\leq 4.8 \text{ V}$	$\leq 2.0 \text{ V}$
at pin 14	$\leq 4.9 \text{ V}$	$\leq 2.1 \text{ V}$
Max. source resistance for pin 5	250 k Ω	
for pin 14	200 k Ω	
Output		
Min. load resistance		
- connections Note 1	90 Ω	
- connections Note 2	30 Ω	
Output voltage at "1" input at min. load resistance		
- connections Note 1	$\leq 0.3 \text{ V}$	
- connections Note 2	$\leq 1.3 \text{ V}$	
Switching speed.		
Switch off delay at 625 mA and 10 H with pin 15 connected to 16	t_d	480 ms
Fall time) connected as in Note 2	t_f	$\leq 0.5 \mu\text{s}$
Rise time) $R_L = 30 \Omega$, $V_S = 30 \text{ V}$	t_r	$\leq 10 \mu\text{s}$

LIMITING VALUES

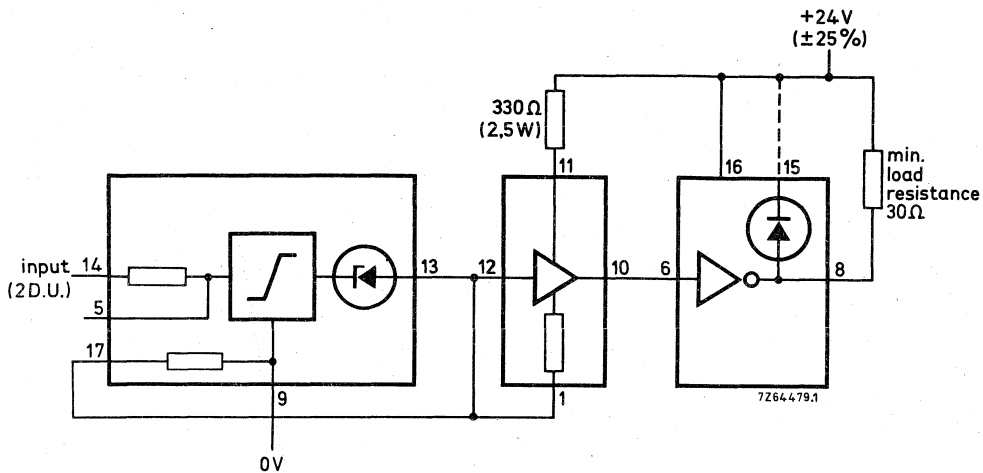
Supply voltage	V_S	max. 30 V
		min. 0 V
Positive transient on V_S , for 10 μs		max. 10 V
Input voltage at pin 14	+V ₁₄	max. 70 V
	-V ₁₄	min. 0 V
Input voltage at pin 5 via min. 2200 Ω	+V ₅	max. 30 V
	-V ₅	min. 0 V
Output current for 20 ms		max. 5 A
for 20 ms each second		max. 2 A

*) Connections as in Note 2

**) Via min. 2200 Ω

APPLICATION INFORMATION

UPA61 as 30 ohms load power amplifier.



DUAL TRIGGER TRANSFORMER

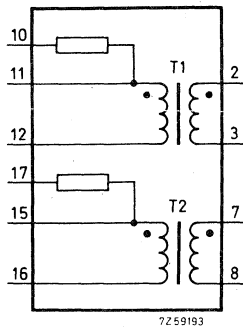
Function

Matching the pulse output from a power amplifier (e.g. UPA61) to thyristor gates.

Case

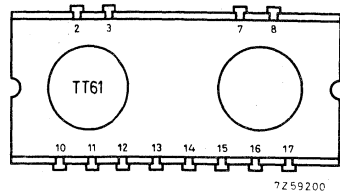
Size A; colour: black.

CIRCUIT DATA



Circuit diagram

- 2. Secondary winding T₁ (cathode thyristor)
- 3. Secondary winding T₁ (gate thyristor)
- 7. Secondary winding T₂ (cathode thyristor)
- 8. Secondary winding T₂ (gate thyristor)
- 10. Resistance connected to primary winding T₁
- 11. Primary winding T₁ (driving source)
- 12. Primary winding T₁ (+V_S)
- 13. Not connected
- 14. Not connected
- 15. Primary winding T₂ (driving source)
- 16. Primary winding T₂ (+V_S)
- 17. Resistance connected to primary winding T₂



Terminal location

CHARACTERISTICS

Frequency range	3 to 50 kHz ¹⁾
Turns ratio primary: secondary	3 : 1
Inductance of primary winding	≥ 2, 2 mH
Leakage inductance referred to primary (secondary short-circuited)	≤ 65 μH
Primary winding resistance at T _{amb} = 25 °C	≤ 4 Ω
Primary series resistor	82 Ω
Secondary winding resistance at T _{amb} = 25 °C	≤ 0, 6 Ω
Output pulse in response to step input, circuit of Fig. 3, R _{eq} = 15 Ω: rise time (from 0, 3 to 3 V) pulse duration, V _{pulse} = 3 V ¹⁾	≤ 0, 6 μs ≥ 20 μs
Output current ²⁾ at pins 2/3 (7/8) at T _{amb} = 25 °C in response to step input at pins 10/12 (16/17) (see Fig. 3): V _S = 18 V, R _{eq} = 15 Ω R _{eq} = 22 Ω	≥ 200 mA ≥ 135 mA
V _S = 30 V, R _{eq} = 10 Ω R _{eq} = 15 Ω	≥ 425 mA ≥ 320 mA

LIMITING VALUES

Primary switched voltage across pins 10/12 (17/16)	max. 30 V ³⁾
Primary switched current no series resistor, duty cycle 1 : 3 max. 82 Ω internal, duty cycle 1 : 3 max. 39 Ω external, duty cycle 1 : 2 max.	max. 800 mA max. 170 mA max. 200 mA
ET product per transformer primary at pins 11, 12 or 15, 16	600 Vμs
Peak pulse power per transformer for duty cycle 1:3, and T _{amb} = 25 °C ¹⁾	17 W
D.C. test voltage between any pair of windings for 1 minute	4 kV
Continuous r.m.s. working voltage	max. 500 V

1) The minimum frequency has been specified with a view to core losses.

2) Minimum mean pulse magnitude over 20 μs.

3) If the UPA61 ceases to oscillate with the output transistor conducting, the primary series resistor may be damaged; circuit design must safeguard against this condition.

APPLICATION INFORMATION

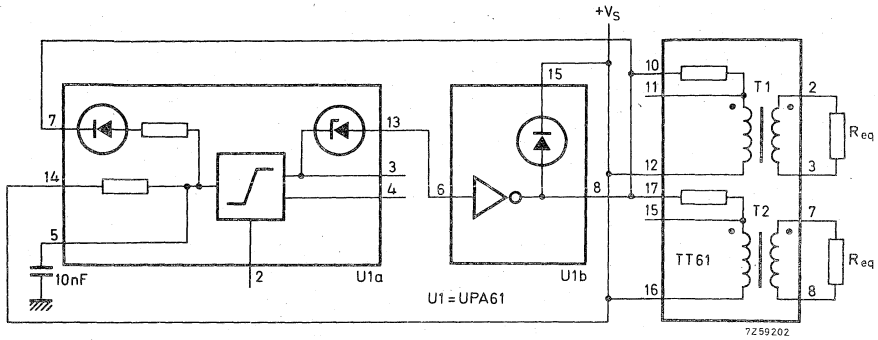


Fig. 3 Low power relaxation oscillator circuit (10 kHz)

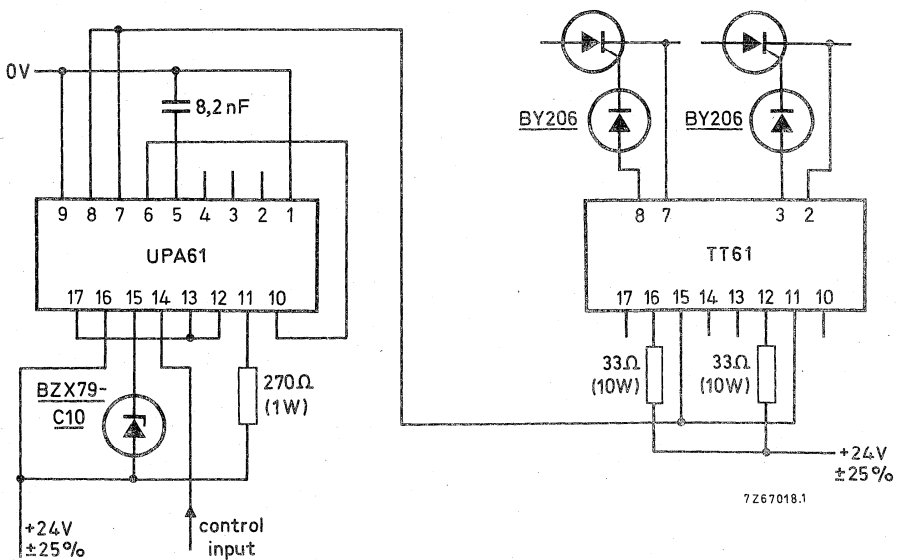


Fig. 4a High power relaxation oscillator circuit (10 kHz)

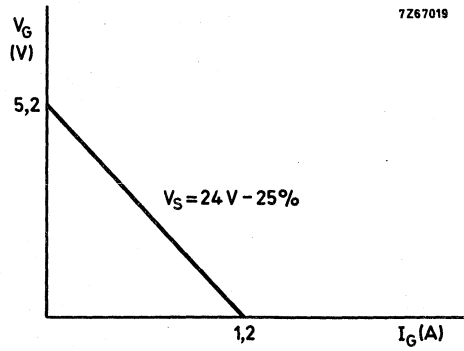


Fig. 4b Gate cathode thyristor voltage versus gate thyristor current

RECTIFIER AND SYNCHRONIZATION ASSEMBLY

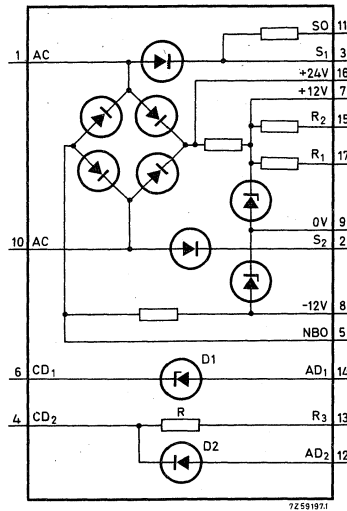
Function

- To provide an unregulated voltage of +24 V for Norbit systems
- To provide synchronization signals.
- To provide +12 V and -12 V (zener stabilized) for servo amplifiers.

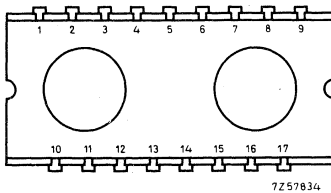
Size: A; colour: black

Case

CIRCUIT DATA



Circuit diagram



Terminal location

- 1 = A.C. input from supply transformer
- 2 = Synchronization voltage
- 3 = Synchronization voltage
- 4 = Cathode D₂

- 5 = Output rectifier bridge
- 6 = Cathode D₁
- 7 = +12 V output voltage
- 8 = -12 V output voltage
- 9 = 0 V from common supply
- 10 = A.C. input from supply transformer
- 11 = Synchronizing resistor output
- 12 = Anode D₂
- 13 = Resistor output cathode D₂
- 14 = Anode D₁
- 15 = +12 V, 150 kΩ source
- 16 = +24 V output voltage
- 17 = +12 V, 100 kΩ source

CHARACTERISTICS

Input

A.C. input voltage (r.m.s.)	2 x 20 V (+10, -15%)
A.C. input current	375 mA max.
Frequency	50 - 60 Hz
Source resistance	1 Ω min. 4 Ω max.

Outputs

Pin number (9 connected to c.t. transformer)	Voltage	Current
16	+18 to +30 V	\leq 220 mA
7	+11 to +15 V	\leq 8 mA
8	-11 to -15 V	\leq 4 mA

In order to obtain the outputs specified, smoothing capacitors are required:

1. a 680 μ F (-10, +50%), 40 V, capacitor connected between pins 16 and 9 to smooth the +24 V and +12 V.
2. a 100 μ F (-10, +50%), 40 V, capacitor connected between pins 5 and 9 to smooth the -12 V.

Additional components

R : 2.2 k Ω ; max. voltage 30 V r.m.s.

D2 : max. reverse voltage 30 V;
max. forward current 200 mA

D1 : nom. zener voltage 6.8 V;
max. dissipation 60 mW

LIMITING VALUES

Input voltage 2 x 22 V r.m.s.

APPLICATION INFORMATION

1. The output current of the -12 V output can be increased to 7 mA by connecting pin 4 to 5 and pin 8 to 13.
2. A mains synchronization signal is available at pin 11 when pins 3 and 2 are joined. The output at pins 2 and 3 takes the form of a zero voltage when the a.c. driving voltage passes through zero. At all other times a positive voltage is present on pins 2 and 3.

DUAL NOR-GATE WITH DIODE-RESISTOR NETWORKS

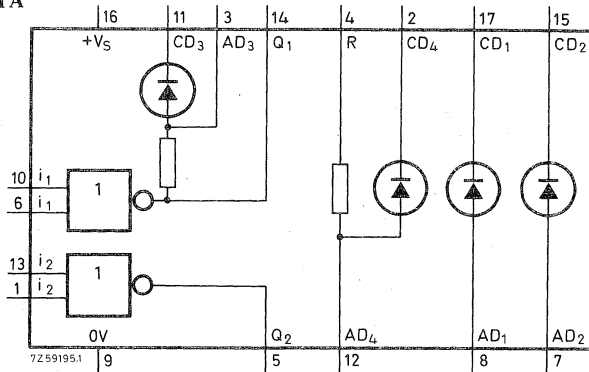
Function

Dual two-input transistor-resistor NOR-gate with diode gating facilities incorporated; specifically applicable as a d.c. counting/shifting stage.

Case

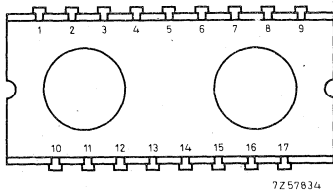
Size: A; colour: black.

CIRCUIT DATA

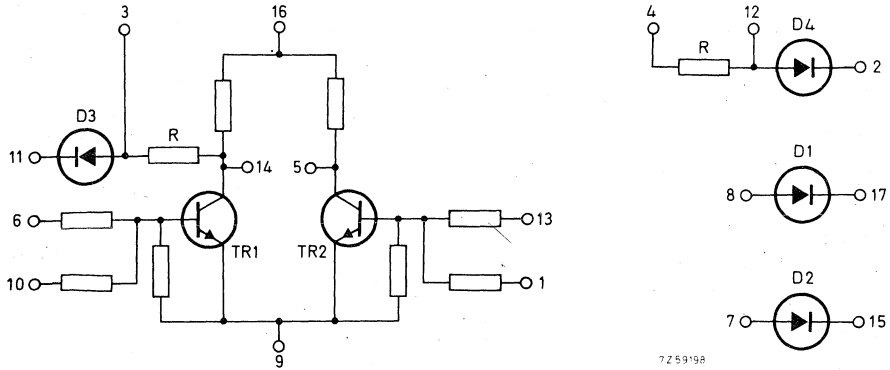


Quick reference circuit diagram

- 1 = Input NOR 2
- 2 = Cathode diode D₄
- 3 = Anode diode D₃
- 4 = Gate resistor
- 5 = Output NOR 2
- 6 = Input NOR 1
- 7 = Anode diode D₂
- 8 = Anode diode D₁
- 9 = 0 V common supply
- 10 = Input NOR 1
- 11 = Cathode diode D₃
- 12 = Anode diode D₄
- 13 = Input NOR 2
- 14 = Output NOR 1
- 15 = Cathode diode D₂
- 16 = +V_S supply for NOR 1 and NOR 2
- 17 = Cathode diode D₁



Terminal location



Circuit diagram

CHARACTERISTICS

NOR-gate

Supply current at V_S nom

at V_S max

Input requirement

Output capability

	at $V_S = 24\text{ V} \pm 25\%$	at $V_S = 12\text{ V} \pm 5\%$
Supply current at V_S nom	5.6 mA	2.8 mA
Supply current at V_S max	7.2 mA	3.1 mA
Input requirement	2 D.U.	2 D.U.
Output capability	10 D.U.	6 D.U.

Input impedance ¹⁾

Input current for "0" output ^{1) 2)}

Switching speed

Fall time

Fall delay time

pins 6, 13	pins 10, 1	pins 6, 10 and 13, 1 in parallel
63 k Ω	47 k Ω	32 k Ω
92 μA	86 μA	75 μA

$$t_f \leq 1.5 \mu\text{s}$$

$$t_{fd} \leq 6 \mu\text{s}$$

Diode-resistor networks

Resistors R (22 k Ω) can be used as a load of 4 D.U. in a logic Norbit system.

¹⁾ Not used inputs returned to 0-volt line .

²⁾ At $V_S = 30\text{ V}$

LIMITING VALUES

Supply voltage	V_S	max.	+30 V
		min.	0 V
Positive transient on V_S		max.	10 V for 10 μ s
Positive input voltage	$+V_i$	max.	70 V
Negative input voltage	$-V_i$	max.	15 V
Reverse voltage of diodes		max.	50 V
Forward current of diodes		max.	75 mA
Repetitive peak forward current of diodes		max.	150 mA
Dissipation of resistor R		max.	50 mW

FLIP-FLOP

QUICK REFERENCE DATA

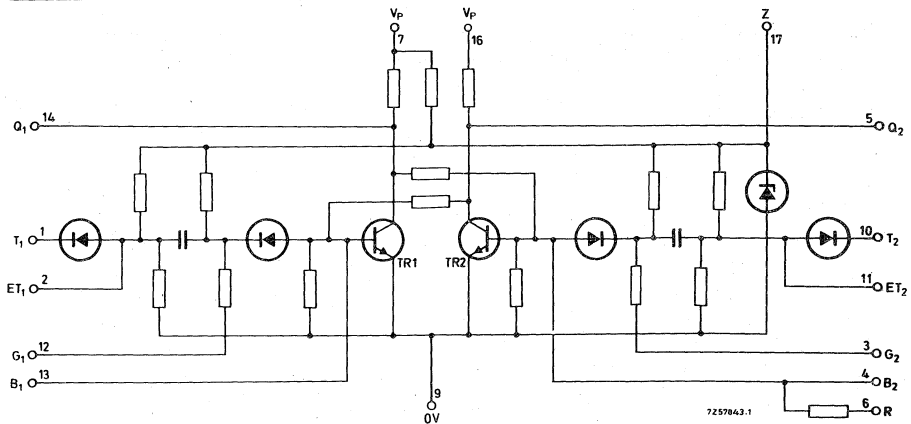
Function	set-reset bistable multivibrator with trigger gates
Encapsulation	size: A block; colour: red
Max. counting speed (worst case)	5 kHz
Output capability	5 D.U., 7 Z.U.
Trigger input requirement	"1"-"0" edge of max. 3 μ s; 2 Z.U.

APPLICATION

The FF90 has been intended to be used in counters, shift registers, etc.

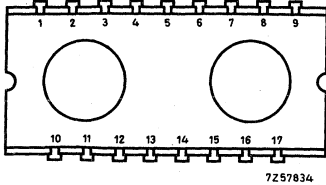
DESCRIPTION

Circuit

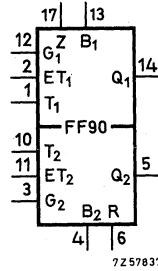


The unit comprises a set-reset bistable multivibrator which incorporates trigger gates. Switching is performed by applying a "1"-"0" edge of max. 3 μ s at the trigger terminals (T1 and T2) which are controlled by gates (G1 and G2). The trigger inputs may be extended by the addition of external diodes to the extension terminals (ET1 and ET2) to provide an OR or inhibit facility. In addition, the circuit may be reset by applying a "1" level to the reset terminal (R) and may be set by applying a "1" level to the base of transistor 1 (B1) via a resistor.

Terminal location



Drawing symbol



- 1 = T₁ = Trigger input 1
- 2 = ET₁ = Extension trigger input 1
- 3 = G₂ = Gate input 2
- 4 = B₂ = Transistor TR₂ base
- 5 = Q₂ = Output 2
- 6 = R = Reset
- 7 = V_p = For positive supply (connect to pin 16)
- 8 = Not connected
- 9 = 0 V = 0 V common

- 10 = T₂ = Trigger input 2
- 11 = ET₂ = Extension trigger input 2
- 12 = G₁ = Gate input 1
- 13 = B₁ = Transistor TR₁ base
- 14 = Q₁ = Output 1
- 15 = Not connected
- 16 = V_p = For positive supply (connect to pin 7)
- 17 = Z = Zener diode*

* Caution: With the supplies connected ensure that pin 16 is not accidentally connected to pin 17, otherwise the zener diode will be damaged.

ELECTRICAL DATA

Power supply

- Voltage +24 V ± 25%
- Current < 21 mA

Input requirements (see also "Switching times")

function	input terminal	input requirement		notes and instructions
		'1' level (D.U.)	'0' level (Z.U.)	
reset (put Q1 to '1')	R	1	0	The Set and Reset inputs may be expanded by using up to 3 suitable diodes at each input. Ensure that the cathode of each diode is connected to the input. If the Set or Reset facilities are used, inputs must be held at '0' (and not left open-circuited) except during the command period.
set (put Q2 to '1')	B1 via 82 k Ω resistor 2)	1	0	
gate	G ₁ , G ₂	2	1	'1' or open-circuit closes gate. '0' opens gate.
gate	G ₁ , G ₂ via a diode 1) 2)	0	1	'1' or open-circuit closes gate. '0' opens gate. Ensure that the anode of the diode is connected to the input.
trigger	T ₁ , T ₂	0	2	Only a '1'-'0' edge occurring within 3 μ s triggers the flip-flop. If T ₁ and T ₂ are interconnected, 4 Z.U. are required.
trigger	ET ₁ , ET ₂ via a diode 1) 2)	0	2	Only a '1'-'0' edge occurring within 3 μ s triggers the flip-flop. If ET ₁ and ET ₂ are interconnected, 4 Z.U. are required. Ensure that the anode of each diode is connected to the input.

1) Diodes type BAX 13, BAX 16 or BAX 78 can be used.

2) If external components are used, ensure that they are mounted as close as possible to the appropriate input.

Output data

Output capability

5 D.U. and 7 Z.U.

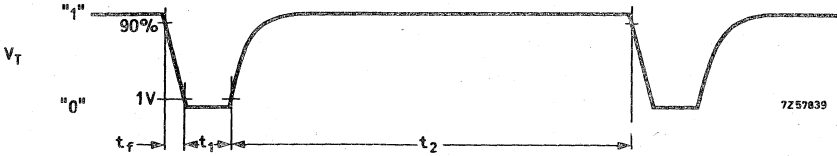
Max. capacitive load

200 pF

Account must be taken of the load imposed by the gates when they are connected to the output terminals (Q1, Q2).

Switching times

Trigger



Max. fall time

t_{fmax} 3 μs

Min. pulse duration

t_{1min} 5 μs

Trigger recovery time

t_2 max. 99 μs

typ. 73 μs

Gate

Gate recovery time

max. 137 μs

typ. 100 μs

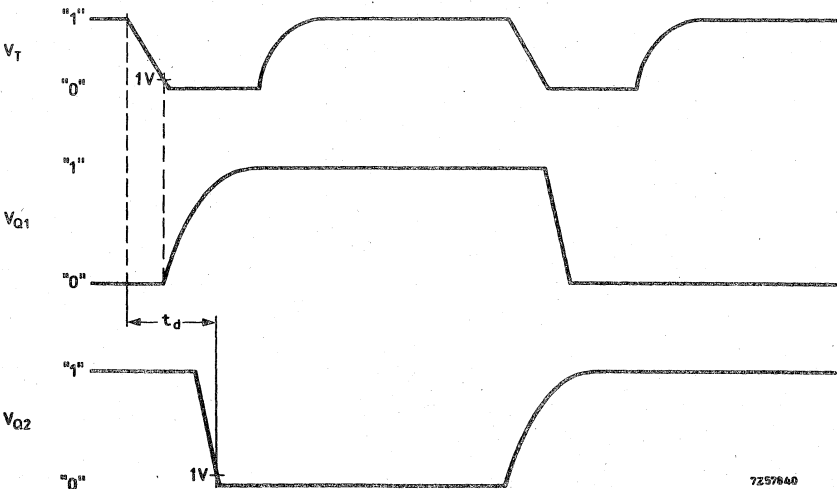
The signal at the gate must be present at least 137 μs (worst case) before the triggering edge is applied to T1 or T2. It is permitted to change the gate signal simultaneously with the triggering edge.

Switching delay

Delay between triggering edge and negative-going output.

t_d max. 8 μs

typ. 3 μs



Reset of Set: The appropriate terminal should be at a logical '1' for a minimum of 50 μ s to reset or set the flip-flop.

Maximum Counting Speed (1:1 mark: space ratio) 5 kHz (worst case)

The worst case figure is related to the most disadvantageous connection or input condition that can be made.

APPLICATION INFORMATION

For connection as a divider of two connect pin 3 to pin 5 and pin 12 to pin 14.

More information is given in "Application Information 849, Counting and Shifting with 90-Series Modules."



TWIN-TRIGGER GATE

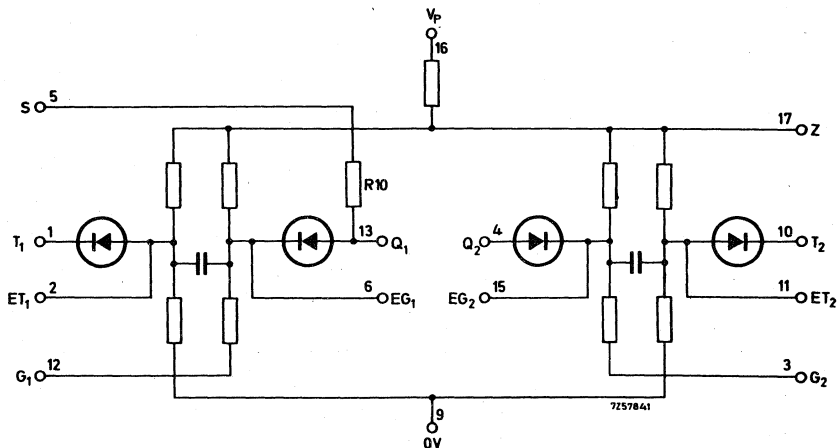
QUICK REFERENCE DATA	
Function	two trigger gates for use with FF90 only
Encapsulation	size: A block; colour: red
Output signal	suitable for triggering direct on transistor base of FF90 (B ₁ and B ₂)
Trigger input requirement	'1'-'0' edge of max. 3 μ s; 2 Z.U.

APPLICATION

The 2.TG90 has been intended to provide two extra independent trigger gates for the FF90.

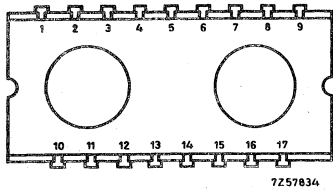
DESCRIPTION

Circuit

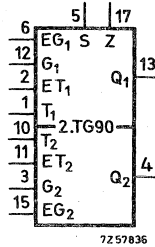


The unit comprises two gating circuits to perform extra independent trigger functions. The mode of operation is the same as for the trigger functions of the FF90. Switching is performed by applying a '1'-'0' edge of max. 3 μ s at the trigger terminals (T₁ and T₂) which are controlled by gates (G₁ and G₂). The trigger inputs may be expanded by the addition of external diodes to the extension terminals (ET₁ and ET₂) to provide an OR or inhibit facility. The extra resistor (R₁₀), connected to terminal Q₁, provides the 'set' facility for the FF90.

Terminal location



Drawing symbol



- 1 = T₁ = Trigger input
- 2 = ET₁ = Extension trigger input 1
- 3 = G₂ = Gate input 2
- 4 = Q₂ = Output to B₂ (pin 4) of FF90
- 5 = S = Set terminal
- 6 = EG₁ = Extension gate input
- 8 = Not connected
- 9 = Not connected
- 9 = 0 V = 0 V common

- 10 = T₂ = Trigger input 2
- 11 = ET₂ = Extension trigger input 2
- 12 = G₁ = Gate input 1
- 13 = Q₁ = Output to B₁ (pin 13) of FF90
- 14 = Not connected
- 15 = EG₂ = Extension gate input
- 16 = V_P = For positive supply
- 17 = Z = Voltage reference terminal, connect to Z (pin 17) on FF90

ELECTRICAL DATA

Power supply

- Voltage +24 V ± 25%
- Current 7.5 mA


Input requirements

function	input terminal	input requirement		notes and instructions
		'1' level (D.U.)	'0' level (Z.U.)	
set (put Q ₂ of associated FF90 to '1')	S	1	0	The Set input may be expanded by using up to 3 suitable diodes on each input. Ensure that the cathode of each diode is connected to the input. If the Set facility is used, the input must be held at '0' (and not left open-circuited), except during the input period.
gate	G ₁ , G ₂	2	1	'1' or open-circuit closes gate. '0' opens gate
gate	G ₁ , G ₂ via diode 1) 2)	0	1	'1' or open-circuit closes gate. '0' opens gate. Ensure that the anode of the diode is connected to the input.
trigger	T ₁ , T ₂	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop ³⁾ . If T ₁ and T ₂ are interconnected, 4 Z.U. are required.
trigger	ET ₁ , ET ₂ via diode 1) 2)	0	2	Only a '1'-'0' edge occurring within 3 μs triggers the flip-flop ³⁾ . If ET ₁ and ET ₂ are interconnected, 4 Z.U. are required. A maximum of two diodes may be connected to each ET terminal. Ensure that the anode of each diode is connected to the input.

For notes see page 4.

Output data

The outputs Q₁, Q₂ are suitable only for use with one FF90; Q₁, Q₂ and Z of the 2.TG90 should be connected to B₁, B₂ and Z respectively of the FF90. The inter-wiring capacitance should be limited at 50 pF (maximum). This capacitance will not be exceeded when a 2.TG90 is mounted next to an FF90.

- 
- 1) Diodes type BAX 13, BAX 16 or BAX 78 can be used. Max. 2 diodes may be added.
 - 2) If external components are used, ensure that they are mounted as close as possible to the appropriate input.
 - 3) Switching times of the triggering signal are the same as for the FF90.

PULSE SHAPER

QUICK REFERENCE DATA

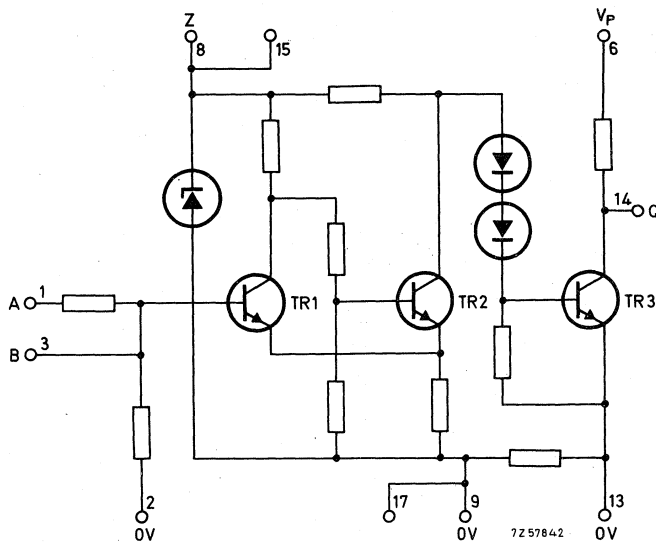
Function	a. Driving the trigger inputs of one or more FF90 or 2.TG90 units b. Shaping signals to produce NORBIT 60 drive levels
Encapsulation	size: A block; colour: green
Output capability	6 D.U.; 40 Z.U.

APPLICATION

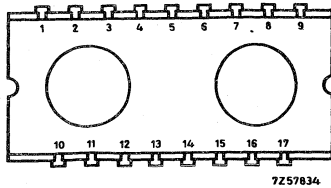
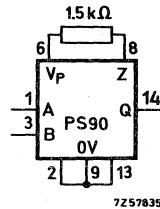
The PS90 has been intended to produce the triggering edge required for the FF90. The output levels are conforming to '1' and '0' of 60-Series logic.

DESCRIPTION

Circuit



The unit contains a Schmitt trigger circuit followed by an inverting amplifier.

Terminal locationDrawing symbol

- | | | | |
|--------------------|--|----------|---|
| 1 = A | = Input via resistor | 9 = 0 V | = 0 V common, internal connection to pin 17 (connect also to pins 2 and 13) |
| 2 = 0 V | = 0 V common (connect to pins 9 and 13) | 10 | = Not connected |
| 3 = B | = Input direct to base | 11 | = Not connected |
| 4 | = Not connected | 12 | = Not connected |
| 5 | = Not connected | 13 = 0 V | = 0 V common (connect also to pins 2 and 9) |
| 6 = V _p | = For positive supply (connect also to pin 8 via 1.5 kΩ resistor*) | 14 = Q | = Output |
| 7 | = Not connected | 15 = Z | = Internally connected to pin 8 |
| 8 = Z | = Zener diode ** internally connected to pin 15 (connect to pin 6 via 1.5 kΩ resistor *) | 16 | = Not connected |
| | | 17 = 0 V | = Internally connected to pin 9. |

* The 1.5 kΩ ± 10% resistor connected between pins 6 and 8 (15) has a dissipation of 0.35 W maximum.

** When the PS90 is mounted on PWB60 or PWB61, pins 7 and 16 are connected to the positive supply V_p. Ensure therefore, that neither pins 7 and 8 nor pins 15 and 16 are interconnected. Otherwise, the Zener diode will be damaged.

ELECTRICAL DATA

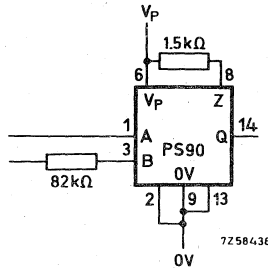
Power supply

Voltage	+24 V ± 25%
Current	< 21 mA

Input Data

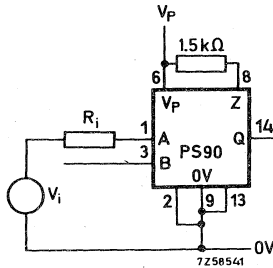
1. Unit driven by circuit block of 60 Series or 90 Series

The input requirement at pin 1 (pin 3 not connected) for '0' output is 1 D.U. One input may be added, namely an 82 kΩ resistor connected to pin 3 (input requirement is 1 D.U.). The circuit then performs as a 2-input NOR function. The 82 kΩ resistor should be mounted as close as possible to the unit.



2. Unit driven by any other circuit at pin 1 with pin 3 not connected.

	Operating	Limiting value
Input voltage to give '0' output	min. +6 V	+30 V
Input voltage to give '1' output	max. +1.5 V	-15 V



Hysteresis

$$\Delta V_i \text{ min.} = 0.55 + 0.003 R_i \text{ V} \quad (R_i \text{ in } k\Omega)$$

$$\Delta V_i \text{ max.} = 1.5 + 0.012 R_i \text{ V} \quad (R_i \text{ in } k\Omega)$$

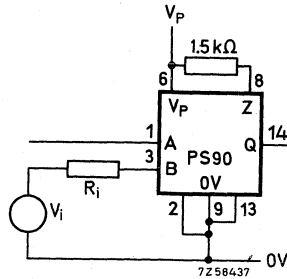
See also "Switching speed".

3. Unit driven by any other circuit at pin 3 with pin 1 not connected

	Operating	Limiting values
Input current to give '0' output	min. 50 μA	5 mA
Input current to give '1' output	max. 15 μA	0 mA

If driven by a voltage source, the source resistance should be minimum 500Ω.

Max. positive voltage with $R_i = 500 \Omega$ +5 V
 Max. positive voltage with $R_i = 6,8 \text{ k}\Omega$ +30 V
 With pin 2 not connected the max. source resistance is $50 \text{ k}\Omega$ and the max. negative voltage is 4 V.



Hysteresis

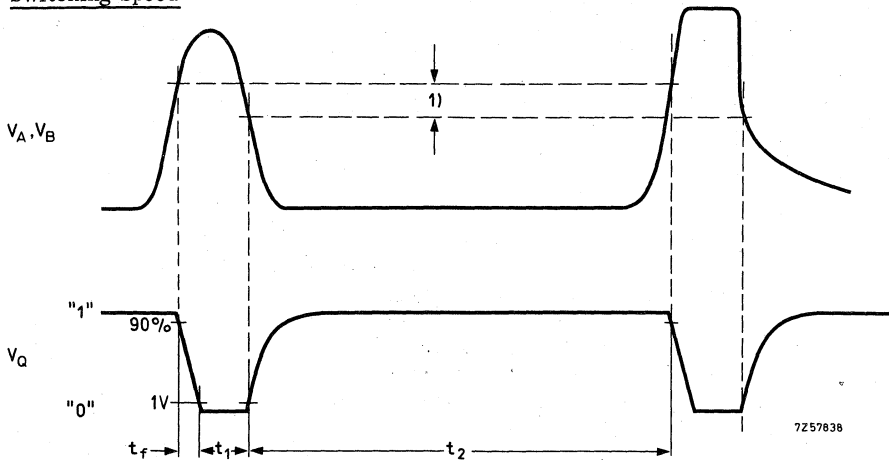
$\Delta V_i \text{ min.} = 0,32 + 0,003 R_i \text{ V}$ (R_i in $\text{k}\Omega$)
 $\Delta V_i \text{ max.} = 0,45 + 0,012 R_i \text{ V}$ (R_i in $\text{k}\Omega$)

See also "Switching speed".

Output Data

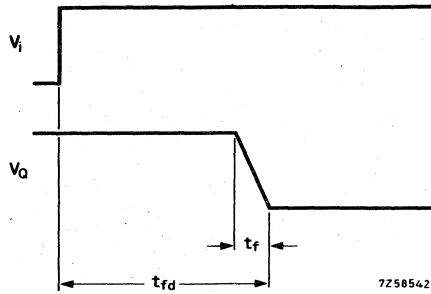
Output capability 6 D.U.
 40 Z.U.
 Max. capacitive load 200 pF

Switching Speed



$t_f \leq 3 \mu\text{s}$
 t_1 and t_2 depend on input waveforms.
 1) Hysteresis ΔV_A or ΔV_B

If a step function is applied to the input and the output is loaded with 200 pF the output signal is given by:



Fall time
Fall delay time

$t_f < 0.25 \mu\text{s}$
 $t_{fd} < 2.5 \mu\text{s}$

Accessories for NORbits



SURVEY

MODULES

TT60 2722 032 00051	Dual thyristor trigger transformer for producing, in conjunction with a UPA60, two pulse currents of up to 400 mA. Turns ratio pr. : sec. : sec. 3 : 1 : 1 Dimensions (incl. pins) 34 x 34 x 49 mm
SIM60 4322 026 38301	Logic simulator for 60-Series NORbits. Supply voltage 117/220/240 V; 50 or 60 Hz Housing attaché case, 415 x 310 x 95 mm

POWER SUPPLY UNITS

LSU60 4322 000 01000 4322 000 01010	Power supply unit for small logic systems with 60-Series NORbits, to be built in chassis UMC60. Input 01000 version 220 V, 45-400 Hz Input 01010 version 110 V, 45-400 Hz Output (d. c.) 150 mA, >18 V; 0 mA, <30 V Board dimensions 90 x 83 mm
PSU60 2722 151 00041	Power supply units for 60-Series NORbits. Input 240 V, 47-440 Hz Output (d. c.) 500 mA, >18 V; 0 mA, <30 V
PSU61 2722 151 00051	Extra d. c. output PSU61 100 V, 25 mA Dimensions 146 x 76 x 77 mm

MAINS FILTERS

MF 0,5 A 9390 213 00002	Mains filter for control systems consuming less than 0,5 A a. c. Attenuation 0,1 - 10 MHz 50 dB A. C. limits 250 V, 0,5 A Dimensions 88 x 38 x 39 mm
MF 2,4 A 9390 253 30142	Mains filter for control systems consuming less than 2,4 A a. c. Attenuation 0,5 - 10 MHz 40 dB A. C. limits 250 V, 2,4 A Dimensions 105 x 62 x 44 mm



CHASSIS AND HOLDERS

BB60 9390 198 00002	Breadboard block to hold 1 size A unit and to interlock with other BB60 blocks for easy assembly of circuits for teaching purposes. Dimensions 56 x 38 x 14 mm
UMC60 4322 026 38330	Universal mounting chassis for 6 size A or 3 size B blocks or combination. Material plastic Dimensions 245 x 95 x 28 mm

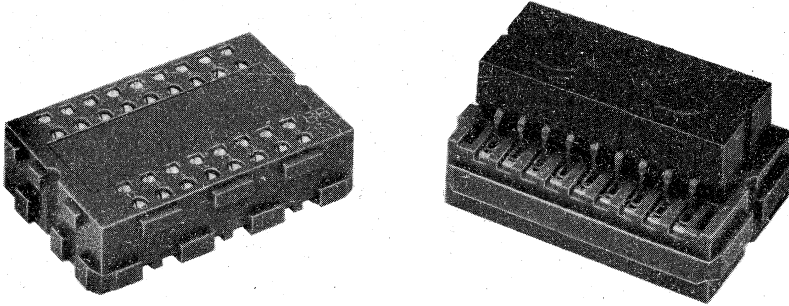
PRINTED-WIRING BOARDS

GPB60 4322 026 38600	Experimenters' printed-wiring boards
GPB60/P 4322 026 38610	Material GPB60 glass-epoxy Material GPB60/P phenol paper Accommodation 10 size A or 4 size B blocks Mating connector F045 (0.2")
PWB60 4322 026 38790	Experimenters' printed-wiring board provided with 0 V tracks
PWB60/P 4322 026 38800	Material PWB60 glass-epoxy Material PWB60/P phenol paper Accommodation 10 size A blocks Mating connector F047, F050, F053 (0.156")
PWB61 4322 026 38810	Experimenters' printed-wiring board provided with 0 V tracks Material PWB61 glass-epoxy Material PWB61/P phenol paper Accommodation 10 size A blocks Mating connector F045 (0.2")
PWB62 4322 026 38780	Printed-wiring board with complete F054 connector, with 0 V and + tracks. Material glass-epoxy Accommodation 4 size A or 2 size B blocks
PWB63 4322 026 73750	Printed-wiring board for use in UMC60. Material glass-epoxy Accommodation 6 size A or 3 size B blocks

STICKERS (drawing symbols on self-adhesive transparent material)

4322 026 36481	50 sheets of stickers for 60-Series Norbits (without 4.NOR60).
4322 026 71941	50 sheets of stickers for 60-Series Norbits (without 4.NOR60).
4322 026 71961	50 sheets of stickers for 60-Series Norbits (incl. TT60).
4322 026 71971	50 sheets of wiring layout stickers for 60-Series Norbits. Actual-size pin distances.
4322 026 71981	50 sheets of wiring layout stickers for 61-Series Norbits. Actual-size pin distances.

BREADBOARD BLOCK for 60-series NORBITS

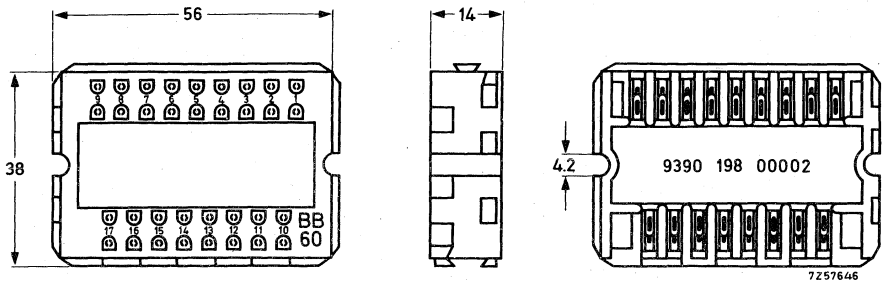
*RZ 27447-18*

APPLICATION

The "Breadboard Block", BB60, has been produced as an aid to 60-Series logic system design. Each block takes one size A unit from the 60-Series, and each block can be firmly locked on any of its edges to another BB60 block, thus a breadboard base can be built up to accommodate any size and complexity of logic circuit, interconnections being simply made with hook-up wire plugged into cup-shaped contacts. The BB60 blocks are ideal as experimenting and teaching aids. For instance, with four units 4. NOR60, one unit TU60 and one unit 2. LPA60 mounted on a base of six blocks BB60, it is easy to realize a large number of instructive logic circuits. Such a base of six blocks can be mounted in the Universal Mounting Chassis UMC60.



DESCRIPTION



(Dimensions in mm)

The right figure shows the underneath of the block with the 2 x 17 soldering lugs; the 60-Series units can be soldered directly onto these lugs. In the top view the cup-shaped contacts are visible; interconnecting wires or discrete components such as resistors can be plugged in on this side. There are two contacts for each terminal of a 60-Series unit, which facilitates multiple connections.

Body material

rigid grey plastic

Contacts

cup shaped, silver plated, suited for wires up to 1 mm diameter

Weight

20 g

Delivery

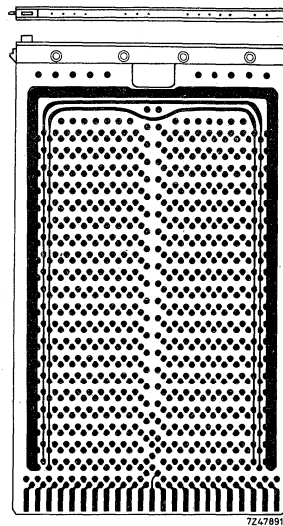
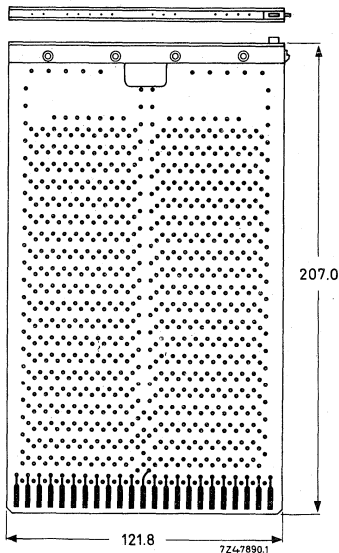
in packs of six, plus six sheets of wiring lay-out stickers for the 60-Series units.

The stickers are drawing symbols on self-adhesive transparent material, and they can be stuck to the top side of the breadboard blocks or be used for circuit drawings. The catalogue No. of a sheet is 9399 269 15301.



EXPERIMENTERS' PRINTED-WIRING BOARD

Experimenters' printed-wiring board (with extractor) with plated-through holes suitable for 60-Series NORbits.



Accommodation of NORbits

size A + size B (HPA60)

10	0
8	1
6	2
3	3
0	4

Material of version GPB 60
of version GPB 60/P

glass-epoxy
phenol paper

Hole diameter

1,2 mm

Contacts

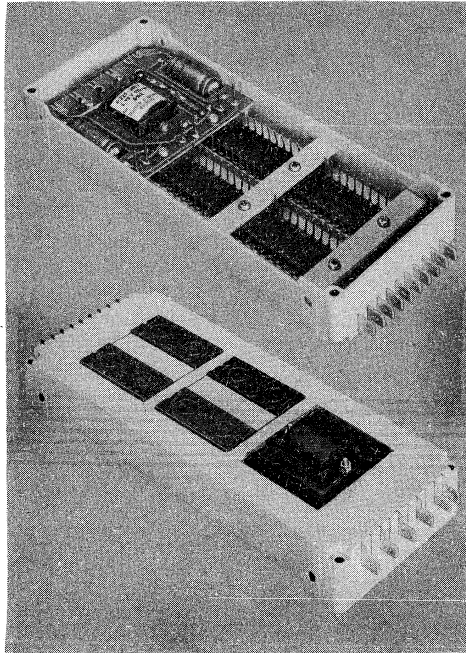
2x23, gold plated, pitch 0,2"

Mating connector

2422 020 52591 (type F045)

For more information, see Application Note "Printed-wiring boards for 60-Series Norbit Assemblies", No. 32/522/BE.

LOGIC SUPPLY UNIT



RZ 27077-11
RZ 27077-8

LSU60 mounted in UMC60

APPLICATION

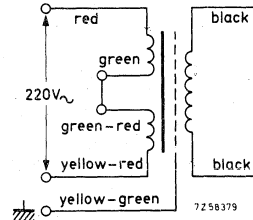
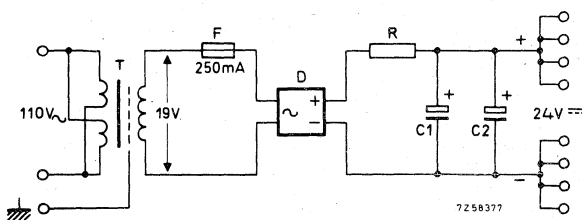
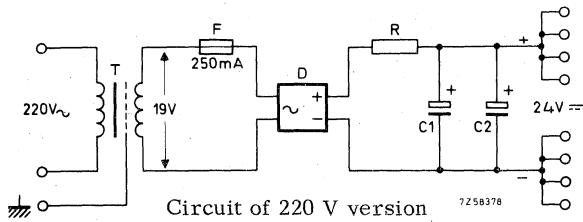
The LSU60 is a power supply unit for small systems with 60-series NORbits. It is intended to be mounted in the universal mounting chassis UMC60. There is a version for 220 V mains (4332 000 01000) and one for 110 V mains (4332 000 01010).

DESCRIPTION

The unit takes the same place as a size B Norbit block (HPA60). To mount the unit in the UMC60, the material between the two adjacent size A holes in the chassis should be removed, after which the unit can be fixed with 4 self-tapping screws.

Slots in the board of the LSU60 facilitate the connection of the input voltage and the output voltage to the Fastons of the UMC60, for external connection to the chassis. The other three pairs of output terminals are soldering tags intended for connection to Norbit blocks on the chassis. A 250 mA fuse (F) is inserted in the secondary part of the circuit. Its catalogue number is 4822 253 20011.

Circuit



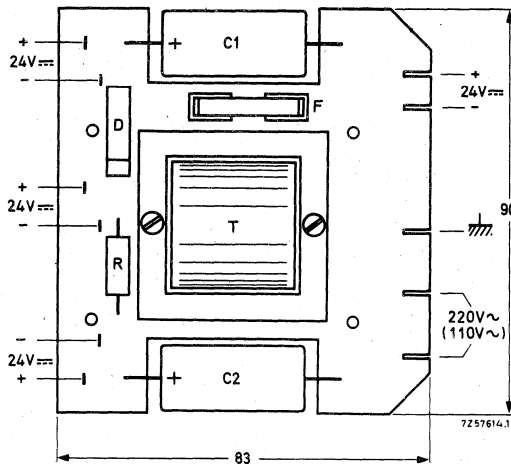
Circuit of 110 V version

Transformer of 110 V version changed for 220 V.

Outline and connections

Dimensions in mm

Weight approx 250 g



ELECTRICAL DATA

Input voltage

version 4332 000 01000
version 4332 000 01010

220 V a.c., +10%, -15%
110 V a.c., +10%, -15%

Input frequency

45 to 400 Hz

Output voltage at 0 mA
at 150 mA

< 30 V d.c.
> 18 V d.c.

Temperature range

-10 to +70 °C

Test voltage for 1 min,
across input terminals and earth
across output terminals and earth

2 kV r.m.s.
2 kV r.m.s.

0,5 A MAINS FILTER

APPLICATION

This mains filter can be used:

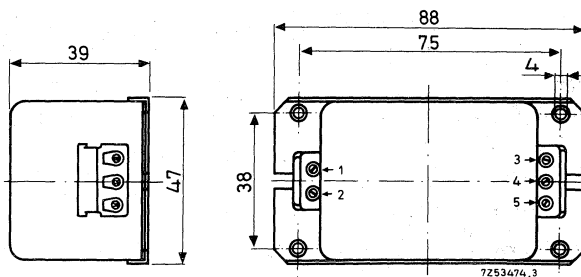
- either between mains supply connection terminals and the mains inputs of control systems, to suppress malfunctioning by transients,
- or between transient-generating equipment and its supply, to prevent high-frequency interference entering into the mains.

The attenuation for frequencies between 0,1 and 10 MHz, at 0,5 A supply current is 50 dB.

CONSTRUCTION

Unit is potted in a metal housing.

Dimensions in mm



Weight: 280 g

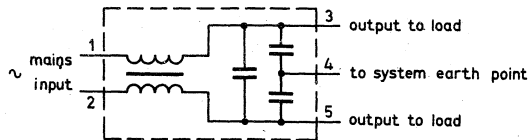
ELECTRICAL DATA

Maximum input voltage	250 V a. c.
Maximum current at $T_{amb} = 40\text{ }^{\circ}\text{C}$	0,75 A a. c.
at $T_{amb} = 70\text{ }^{\circ}\text{C}$	0,5 A a. c.
Repetitive peak current, 50 Hz	$\leq 2,5\text{ A}$
Non-repetitive peak current for 2 s	$\leq 2,5\text{ A}$
Insulation resistance between terminals and case	$> 5\text{ M}\Omega$

Test voltages

a) for 1 min, across terminals and case	2000 V, 50 Hz
b) for 2 s across terminals 1 and 2, or 3 and 5	1625 V d. c.
c) for 2 s across terminals 3 and 4, or 4 and 5	1800 V, 50 Hz

Attenuation between 0, 1 and 10 MHz $> 50\text{ dB}$

Circuit diagram

7253846.3

Operating temperature range $-25\text{ to }+70\text{ }^{\circ}\text{C}$

Storage temperature range $-25\text{ to }+85\text{ }^{\circ}\text{C}$

TEST SPECIFICATIONS

The filter meets the tests of MIL-STD-202E

1. Thermal shock test according to method 107D, 5 cycles from $-25\text{ to }+85\text{ }^{\circ}\text{C}$
2. Moisture resistance test according to method 106D
3. Humidity test according to method 103B, condition D40 $^{\circ}\text{C}$, 90 to 95% R. H.

2,4 A MAINS FILTER

APPLICATION

This mains filter can be used:

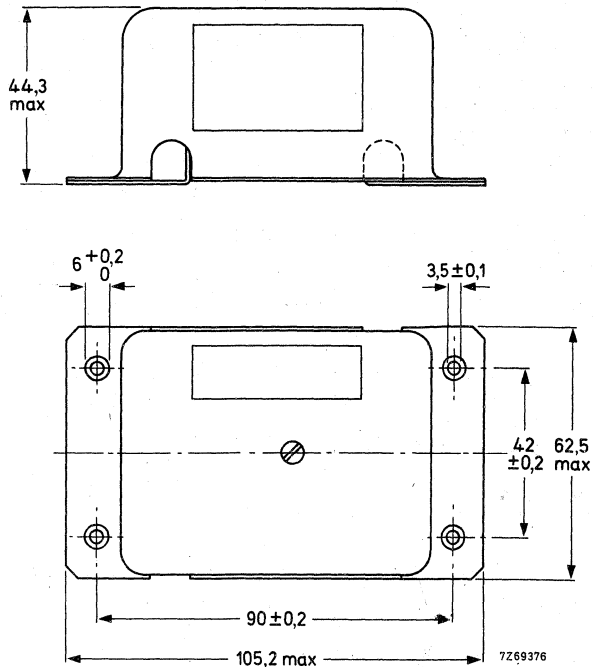
- either between mains supply connection terminals and the mains inputs of control systems, to suppress malfunctioning by transients,
- or between transient-generating equipment and its supply, to prevent high-frequency interference entering into the mains.

The attenuation for frequencies between 0,5 and 10 MHz, at 2,4 A supply current is 40 dB.

CONSTRUCTION

The unit is encapsulated in a metal housing.

Dimensions in mm

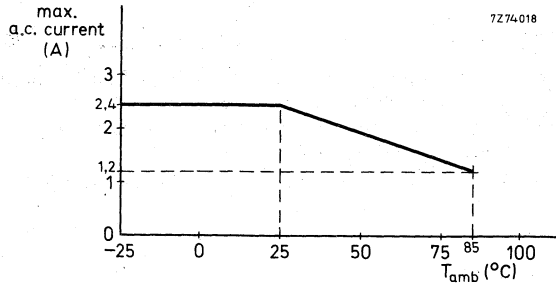


Weight: 275 g

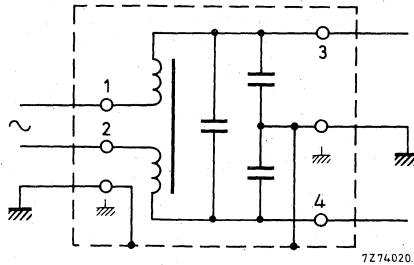
ELECTRICAL DATA

The values given below apply only to filters which are used in earthed installations.

Maximum input voltage	250 V a.c.
Maximum current at $T_{amb} = 25\text{ }^{\circ}\text{C}$	2,4 A a.c.
at $T_{amb} = 85\text{ }^{\circ}\text{C}$	1,2 A a.c.



Repetitive peak current, 50 Hz	$\leq 10\text{ A}$
Non-repetitive peak current for 2 s	$\leq 10\text{ A}$
Impedance at 2, 4 A	$0,925\ \Omega$
Insulation resistance between terminals and case	$> 5\text{ M}\Omega$
Test voltage	
for 2 s between terminals and case	2700 V d.c.
for 2 s between input or output terminals	1625 V d.c.
Attenuation between 0,5 and 10 MHz	$> 40\text{ dB}$
Circuit diagram	



Operating and storage temperature range	-25 to +85 °C
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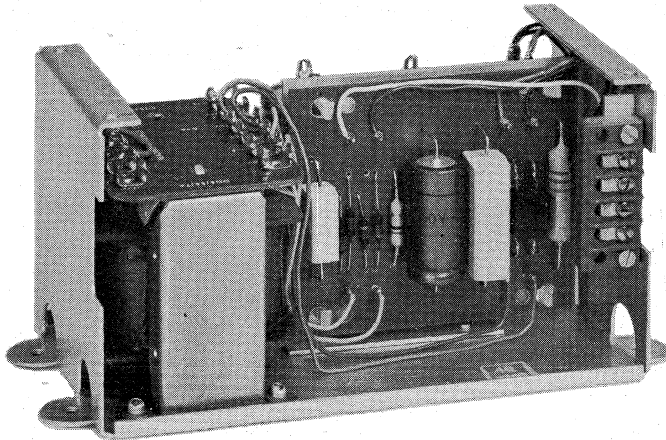
TEST SPECIFICATIONS

The filter meets the tests of MIL-STD-202E:

- thermal shock test according to method 107D, 5 cycles from -25 to +85 °C
- moisture resistance test according to method 106D

The capacitor used meets the requirements of VDE 0560-7.

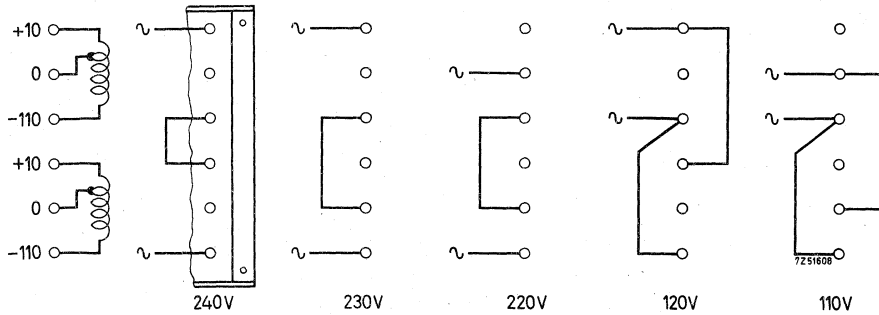
POWER SUPPLY UNITS for 60-series NORBITS



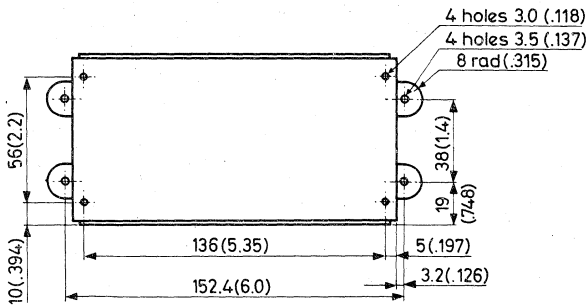
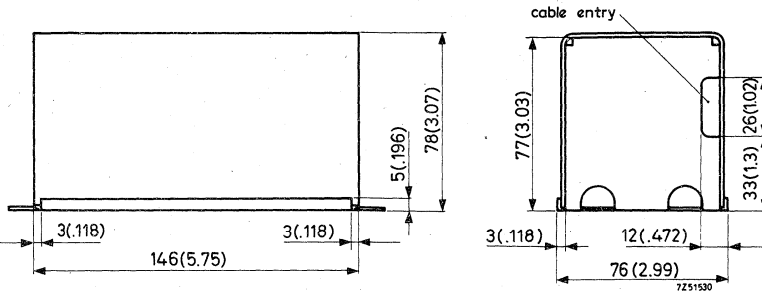
(Cap removed from unit.)

RZ 23469-1

Input voltage	240, 230, 220, 120 or 100 V _{ac} , +10%, -15%
Input frequency	47 to 440 Hz
Output	< 30 V at 0 mA, > 18 V at 500 mA (for logic supply)
Additional output PSU 61	+100 V \pm 25% at 0 to 25 mA (for Switch Filters)
Operating ambient temperature	-10 to +60 °C
Test voltage between windings	2 kV



Input facilities of mains transformer



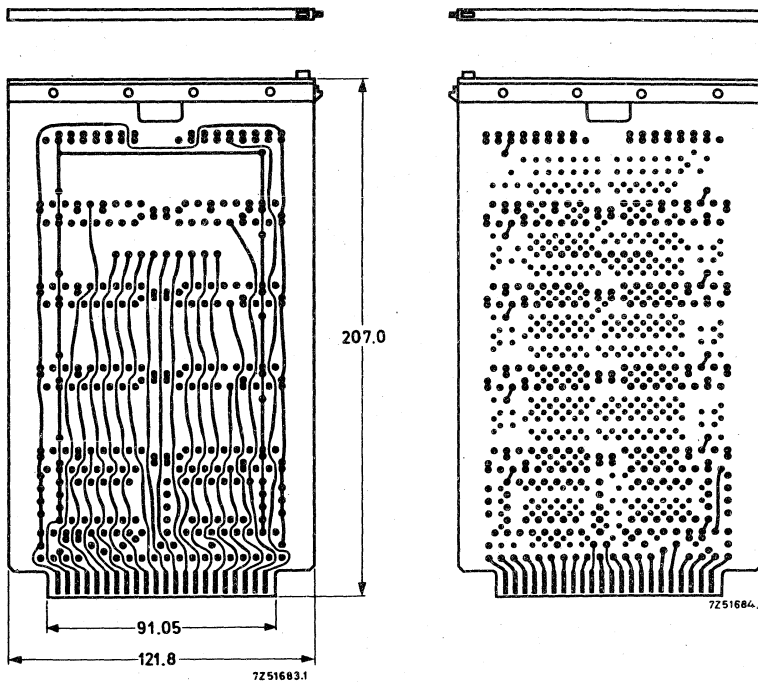
Dimensions in mm, inch values between brackets.

Case: aluminium

Weight: approx. 1000 g

EXPERIMENTERS' PRINTED-WIRING BOARDS for 60-series NORBITS

Experimenters' printed-wiring boards (with extractor) with plated-through holes, and 0-volt supply line tracks for pins 9 and 16.



Accommodation

Material of version 4322 026 38790
of version 4322 026 38800

Hole diameter

Contacts

Mating connector

For more information, see Application Note "Printed-wiring boards for 60-series Norbit Assemblies", No. 32/522/BE.

ten blocks size A

glass-epoxy (PWB 60)
phenol paper (PWB 60/P)

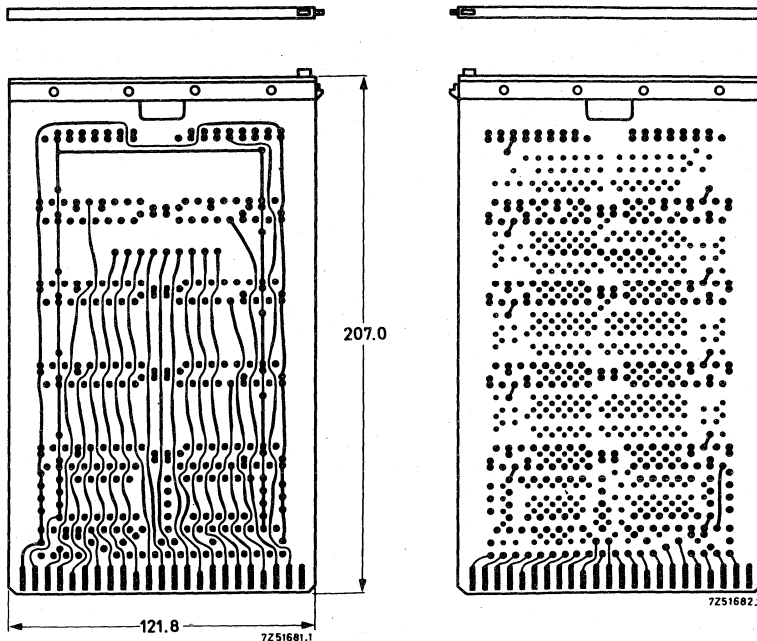
1.3 mm

2x22, gold plated, pitch 0.156"

types F047, F050, F053

EXPERIMENTERS' PRINTED-WIRING BOARDS for 60-series NORBITS

Experimenters' printed-wiring boards (with extractor) with plated-through holes, and 0-volt supply line tracks for pins 9 and 16.



Accommodation

Material of version 4322 026 38810
of version 4322 026 38820

Hole diameter

Contacts

Mating connector

For more information, see Application Note "Printed-wiring boards for 60-series Norbit Assemblies", No. 32/522/BE.

ten blocks size A

glass-epoxy (PWB 61)
phenol paper (PWB 61/P)

1.3 mm

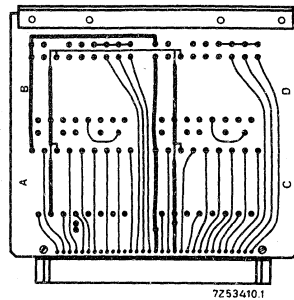
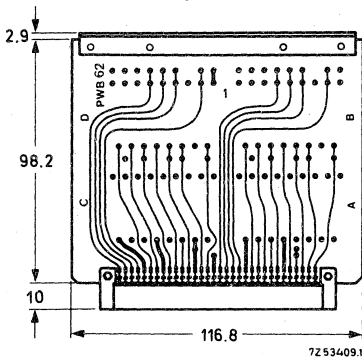
2x23, gold plated, pitch 0.2"

2422 020 52591 (type F045)

PRINTED-WIRING BOARD for 60-series NORBITS

Printed-wiring board with plated-through holes, extractor and complete F054 connector, of which the female part has been soldered to the board. All terminals of any Norbit mounted on the board are brought out. The 0-volt pins and the positive supply pins have been tracked together for all Norbits.

The board is especially useful for systems where a small number of types (board + blocks) is essential with a view to replacement.



Accommodation

size A + size B (HPA60)

4	0
2	1
0	2

Material

glass-epoxy

Hole diameter

1.2 mm

Connector

type
contacts
contact pitch
terminations

F054 (2422 025 89082)

2 x 32

2,54 mm (0,1")

suitable for mini wire-wrapping

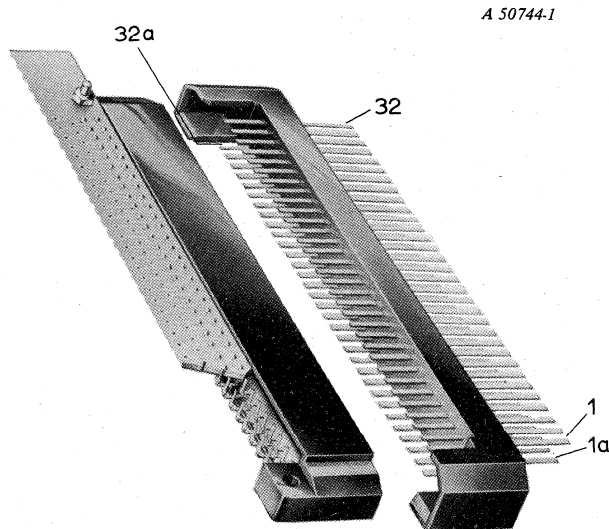
INTERCONNECTION DIAGRAM

The designer of an electronic circuit with Norbits mounted on PWB62 boards, can easily derive the necessary connecting instructions from the diagram depicted on the next page. With this diagram he can indicate the connections that are to be made. The diagram gives the numbers of the terminals of the circuit block, its position on the PWB62 and the numbers of the connector terminals (see photograph below). The thin lines in the diagram represent the tracks of the printed circuit on the PWB62, so they indicate the interconnections between the Norbit terminals, and the connector pins.

All the designer has to do is to draw the connections which should be made by the wire man (see thick lines on the second diagram).

As an example we give an alarm circuit of which the designer has drawn the diagram in the upper part, and has indicated for the wire man on the lower part the external interconnections to be made. Moreover, outside the diagram the necessary connections to be made the supply with unit, the oscillator, switches, and so on, are indicated by the arrows.

In this way the design engineer can draw the electronic circuit and the associated assembly instructions in one diagram.



Connector pin numbering as used in Interconnection Diagram.

Interconnection diagram (containing track data)

See example next page.

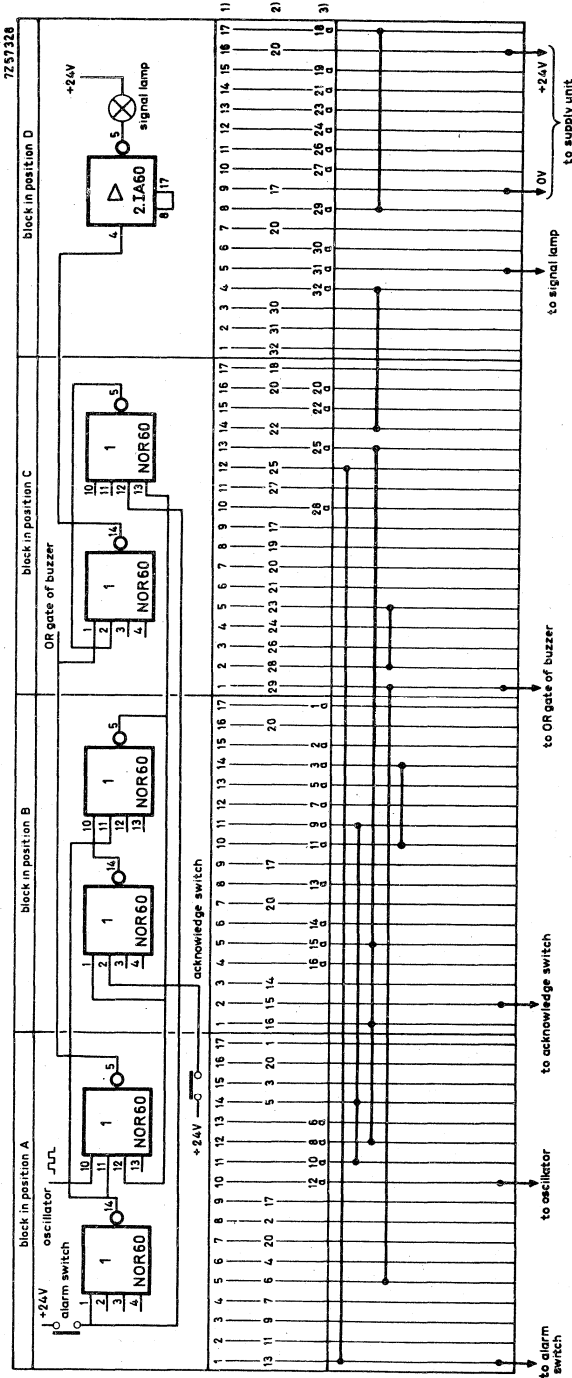
7257329

block in position A																	block in position B																	block in position C																	block in position D																
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
13	11	9	7	6	4	20	2	17			5	3	20	1	16	15	14	20	19	28	26	24	23	21	20	19	17			27	25	22	20	18	32	31	30	20	17			29	27	26	24	23	21	19	18	8																	
12	10	8	6										16	15	14		13	12	11	10	9	8	7	6	5	4	3	2						16	15	14	13	12	11	10	9	8	7	6	5	4	3	2																			

- 1) Terminal number of circuit block inserted in PWB62
- 2) Pin number of male F054 connector (see photograph) to which track on the "solder side" (bearing no type number) is connected.
- 3) Pin number of male F054 connector (see photograph) to which track on the "components side" (bearing type number) is connected.

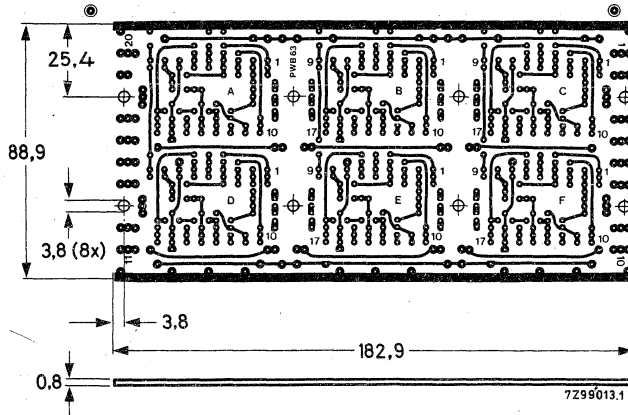


Example



- 1) Terminal number of circuit block inserted in PWB62
- 2) Pin number of male F054 connector (see photograph) to which track on the "solder side" (bearing no type number) is connected
- 3) Pin number of male F054 connector (see photograph) to which track on the "components side" (bearing type number) is connected.

PRINTED-WIRING BOARD for UMC60



Single-sided printed-wiring board (with holes) intended for use in a Universal Mounting Chassis UMC 60.

Tracks have been laid such that only short jumpers need be used to obtain all kinds of logic functions with Norbits.

Accommodation (60-series blocks)

6 size A
or 4 size A + 1 size B (HPA60)
or 2 size A + 2 size B
or 3 size B

Material

glass-epoxy

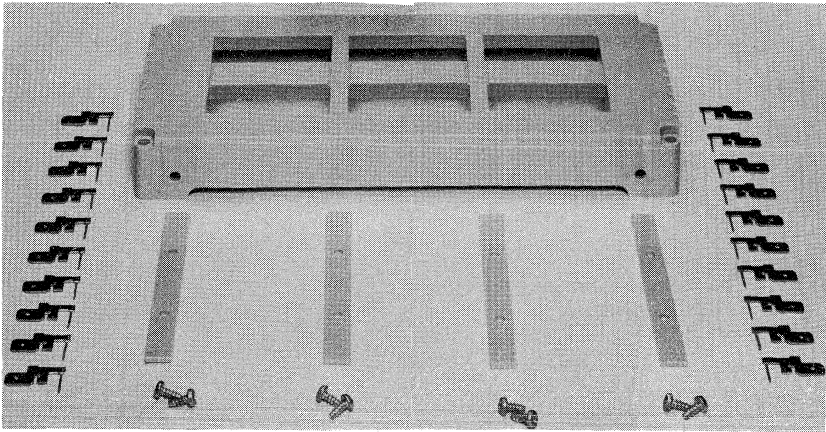
Board thickness

0,8 mm

Hole diameter

1,2 mm

UNIVERSAL MOUNTING CHASSIS for 60-series NORBITS



RZ 26441-7

APPLICATION

Low cost mounting facility for:

- 6 size A blocks,
- or 4 size A blocks and 1 size B block (HPA60)
- or 2 size A blocks and 2 size B blocks
- or 3 size B blocks.

The chassis provides an alternative for mounting 60-series blocks on a printed-wiring board with connector.

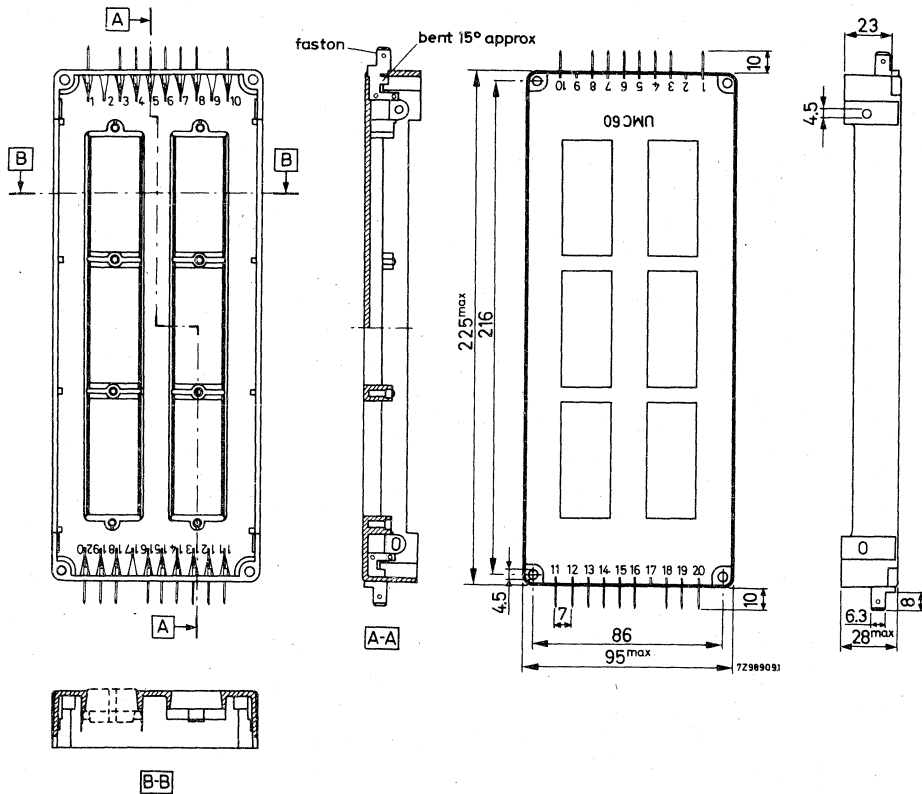
Chassis can be bolted together side by side (Fig.4); they may also be stacked (Fig.5 and Fig.6) or hinged.

DESCRIPTION

The delivery includes a moulded polycarbonate chassis body, 4 moulded polycarbonate strips, 8 self-tapping screws and 20 standard 0.25 inch Fastons. Strips and screws are for clamping the circuit blocks into the holes in the chassis. The Fastons are for connections to the circuitry in the chassis.

To accommodate a size B block, it is necessary to remove the material between two size A holes, see Fig.1.

Interconnections between the terminal pins of the circuit blocks can be made by means of hand soldering or mini wire-wrapping; it is also feasible to use printed-wiring board PWB63 (catal. No. 4322 026 73750) in the chassis (see Fig.3).



Colour: grey

Dimensions in mm

Weight: 150 g approx.

ASSEMBLY AND USE

The Fastons are brought in from the outside of a chassis and then fixed by bending the slotted part on the inside over about 15°

The blocks are clamped into the chassis with the strips and the self-tapping screws.

For fixing two or more chassis together, 4 mm bolts and nuts may be used.

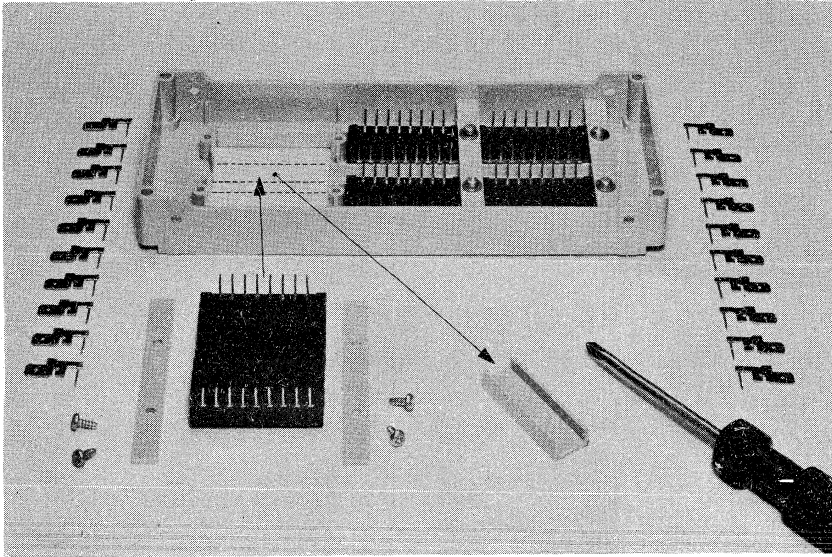


Fig.1

RZ 26441-6

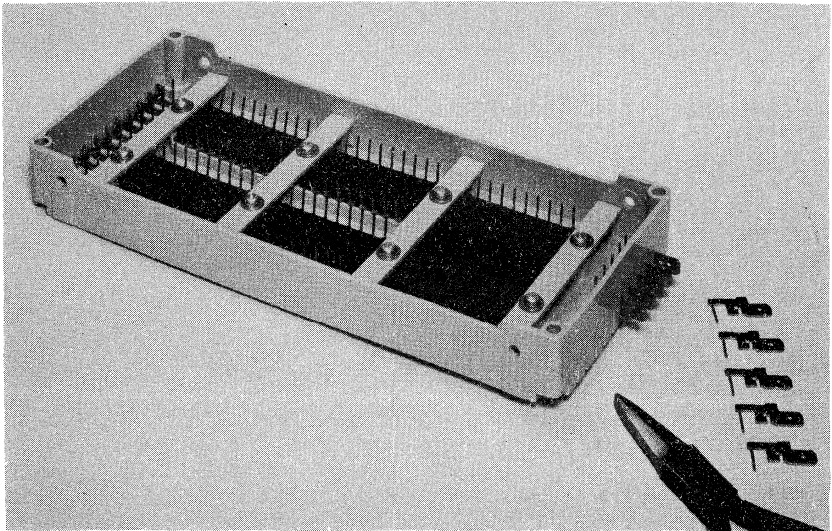


Fig.2

RZ 26441-5

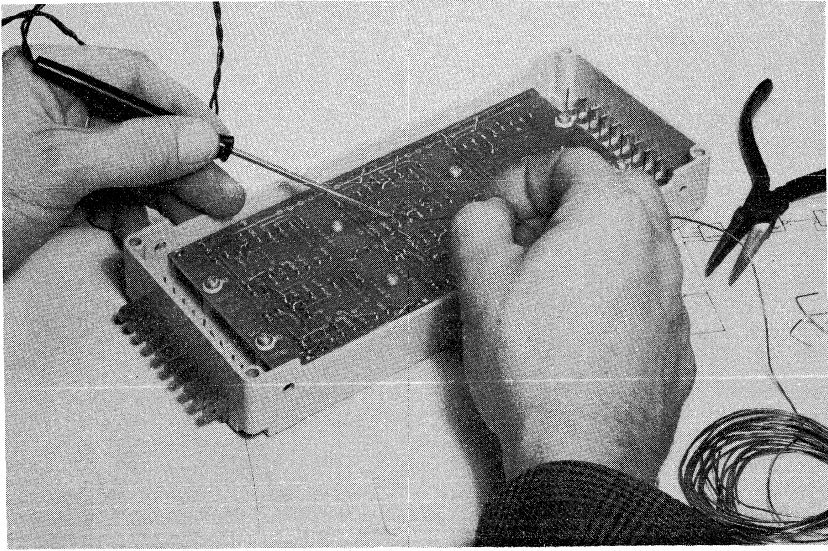


Fig.3

RZ 26441-8

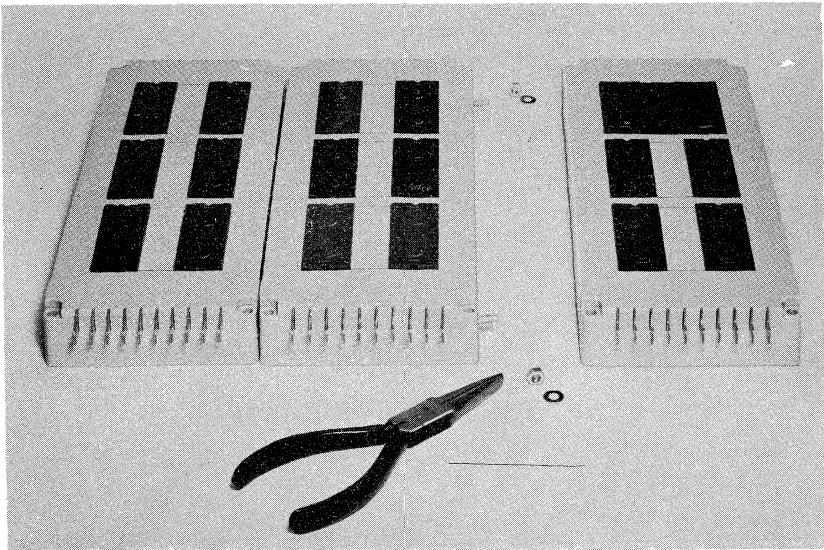


Fig.4

RZ 26441-4

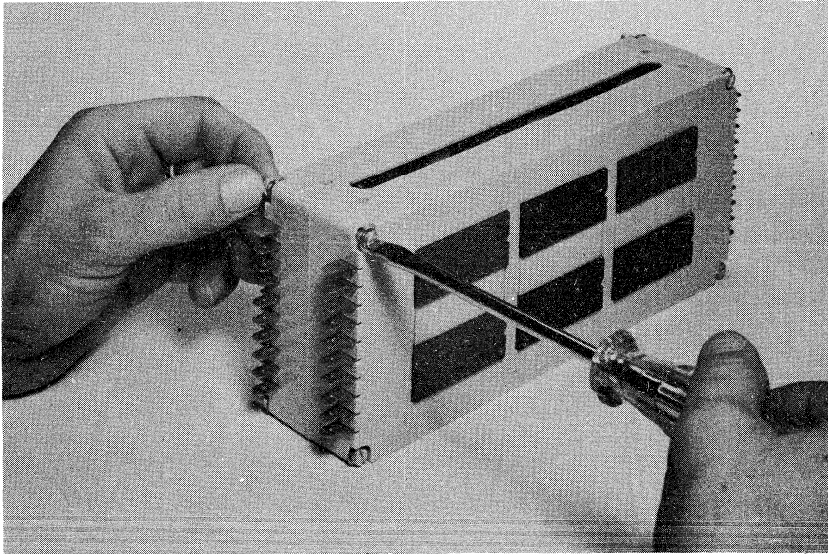


Fig.5

RZ 26441-9

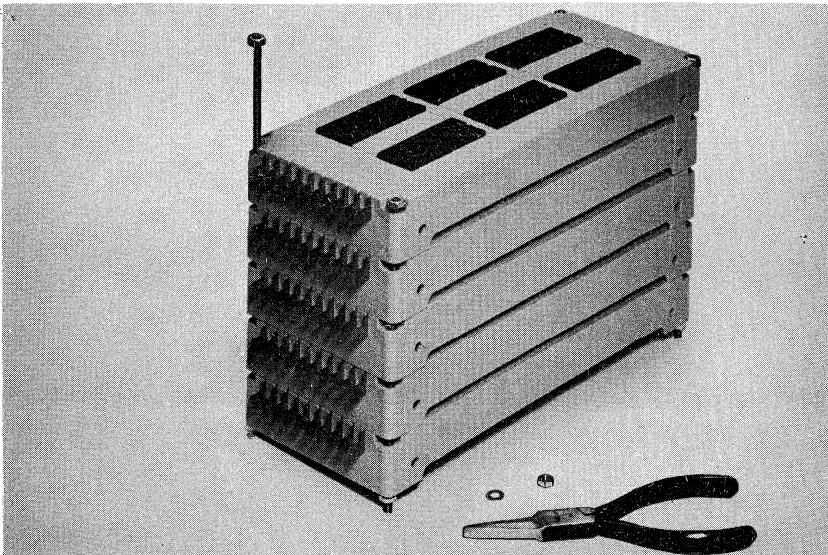
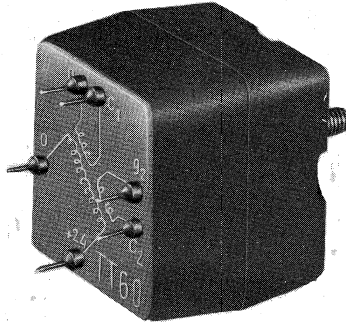


Fig.6

RZ 26441-10

THYRISTOR TRIGGER TRANSFORMER



A 51993

APPLICATION

The TT60 can produce, in conjunction with the power amplifier UPA61, two pulse currents of up to 400 mA. This is sufficient gate current to trigger a pair of practically any type of thyristor.

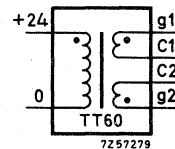
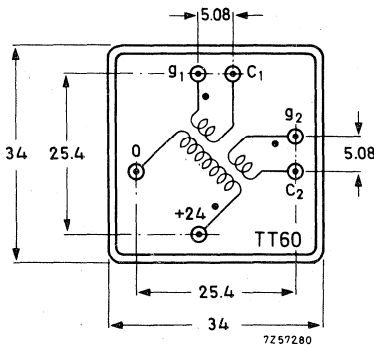
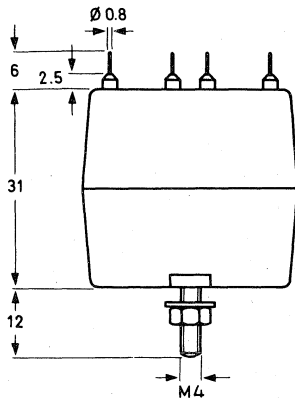
DESCRIPTION

The transformer has been encapsulated in a mould.

A threaded stud permits the unit to be fixed to a support (This may be the thyristor heat sink, to obtain short gate and cathode leads).

For the hand soldering of wires to the pins 7 wire spirals, catal.No. 4022 220 64781, are packed with the transformer.

Dimensions in mm



Drawing symbol

Weight: 80 g approx.

TECHNICAL PERFORMANCE

Turns ratio

primary : sec₁ : sec₂ 3 : 1 : 1

Inductance of primary winding ≥ 6 mH

Leakage inductance referred to primary (both secondaries short-circuited) ≤ 18 μH

Primary winding resistance at T_{amb} = 25 °C ≤ 0.5 Ω

Secondary winding resistance at T_{amb} = 25 °C ≤ 0.1 Ω

Test voltage between the windings for 1 minute 5 kV

Output pulse in response to step input, circuit of Fig. A, $R_{eq} = 13 \Omega$:	
rise time	$\leq 0,75 \mu s$
pulse duration	$\geq 20 \mu s$
Primary current (r. m. s.)	max. 600 mA
Primary switched current, duty cycle 1:4	max. 1800 mA
ET product primary	900 μVs
Operating ambient temperature	-10 to +85 °C
Storage temperature	-40 to +85 °C

APPLICATION INFORMATION

Pulse amplifier circuit

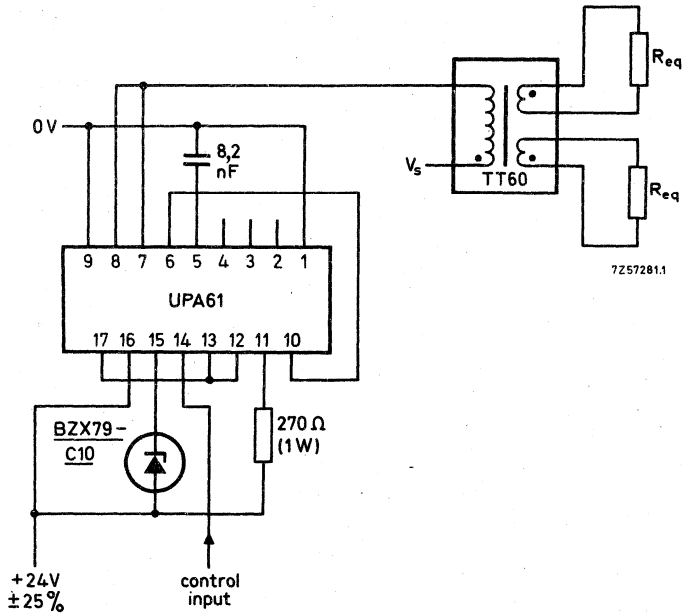


Fig. A

Power oscillator circuit

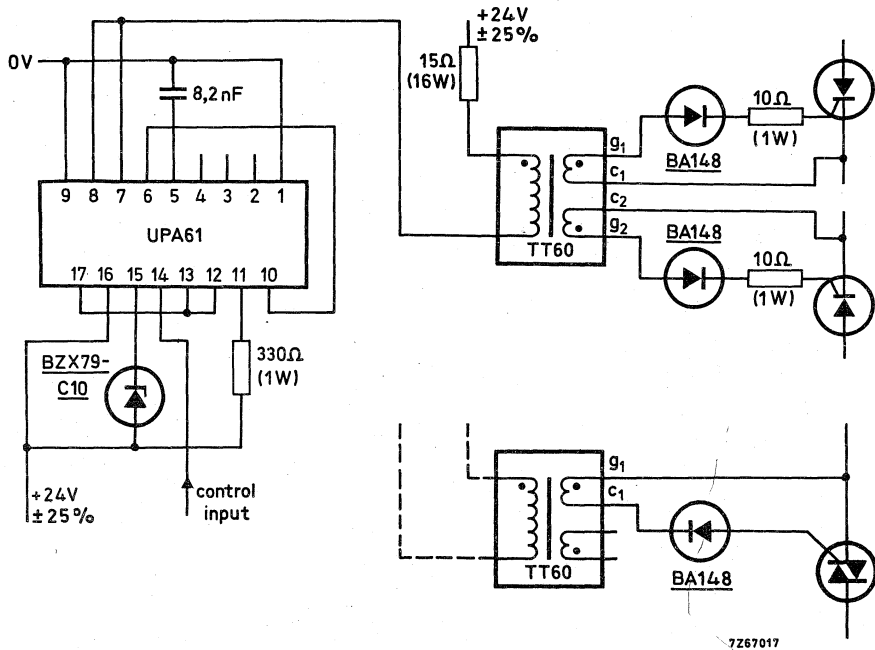
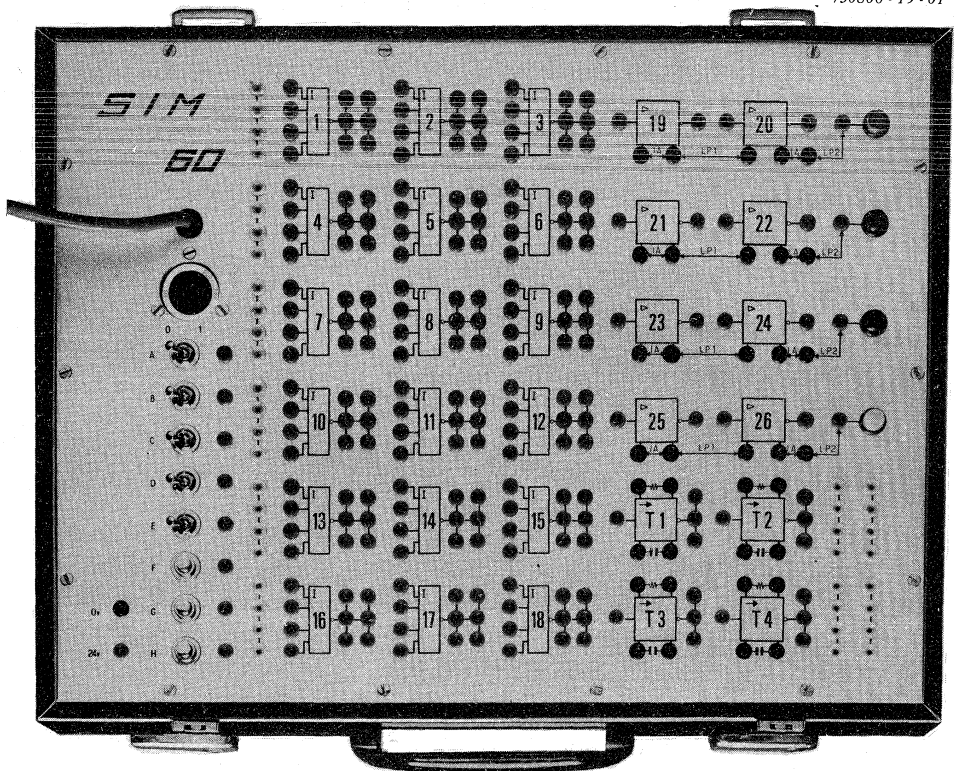


Fig. B shows the UPA61 as a 10 kHz power oscillator to trigger via TT60 a pair of thyristors or a triac. Oscillation commences with a "high" (+ 12 V) on the control input (terminal 14 of the UPA61) ceasing when it becomes "low" (0 V).

LOGIC SIMULATOR for 60-Series NORbits

Purpose	logic system design simulation (breadboarding) and instruction
Supply voltage	117/220/240 V, 50 or 60 Hz
Housing	attaché case 415 x 310 x 95 mm
Weight	5,5 kg

730806 - 19 - 01



DESCRIPTION

The SIM60 is a self-contained portable logic simulator, housed in a small light-weight attaché case, containing the following parts:

9 x 2. NOR60	5 x toggle switch
4 x 2. IA60	3 x push button
4 x TU60	302 x socket
1 x power supply	10 x patchcord, length 50 cm
4 x indicator lamp	20 x patchcord, length 30 cm
	10 x patchcord, length 20 cm

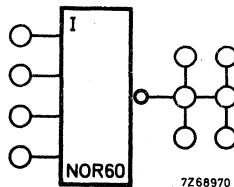
The circuit blocks are symbolized by rectangles and squares with adjoining input, output and auxiliary terminal sockets for patchcords. The fan-out of each block corresponds to the number of output sockets provided. Six groups of four auxiliary sockets (yellow) at the left and four groups at the right of the panel provide for concurrent application of signals to various control inputs.

Part description

2. NOR60 (see also relevant data sheet)

Units 1 to 18

18 NOR functions, each with 4 identical inputs and 6 paralleled output sockets.

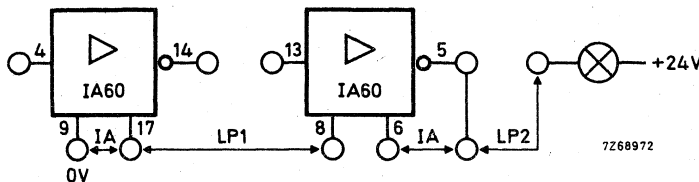


2. IA60 (see also relevant data sheet)

Units 19 to 26

8 inverting amplifiers;

Each 2. IA60 can be connected as an LPA60 to drive a load of 3 W at 24 V.

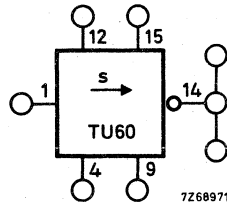


- To use the 2. IA60 as two inverting amplifiers, make the connections indicated by the arrows IA.
- To use the 2. IA60 as a single LPA60, make the connections indicated by the arrows LP1 and LP2.

TU 60 (see also relevant data sheet)

Units T1 to T4

Timer unit with 1 input and 3 paralleled output sockets. The time constant is determined by the resistance and capacitance connected externally between terminals 12-15 and 4-9, respectively.



Power supply (0 V, 24 V)

Suitable for operation from 117 V, 220 V or 240 V, 50 or 60 Hz, mains. Includes input cable and plug. Provides system 0 V and 24 V d.c. supply rails.

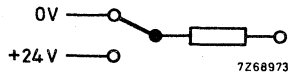
Indicator lamps

1 red
1 yellow
1 white
1 green

can be used as output indicators for LPA60, one side connected to +24 V

Toggle switches (A to E) and push buttons (F to H)

To simulate 1 or 0 input conditions and temporary 1 input signals, respectively.



output via internal current limiting resistance of 12 k Ω

Sockets

Colour indicates function:

Green = inputs

Red = outputs and 24 V

Black = other unit terminals and 0 V

Yellow = auxiliary sockets to multiply various signals

Note: The terminal socket marked '24 V' on the panel is connected directly to the +24 V supply rail, without current limiting resistor.

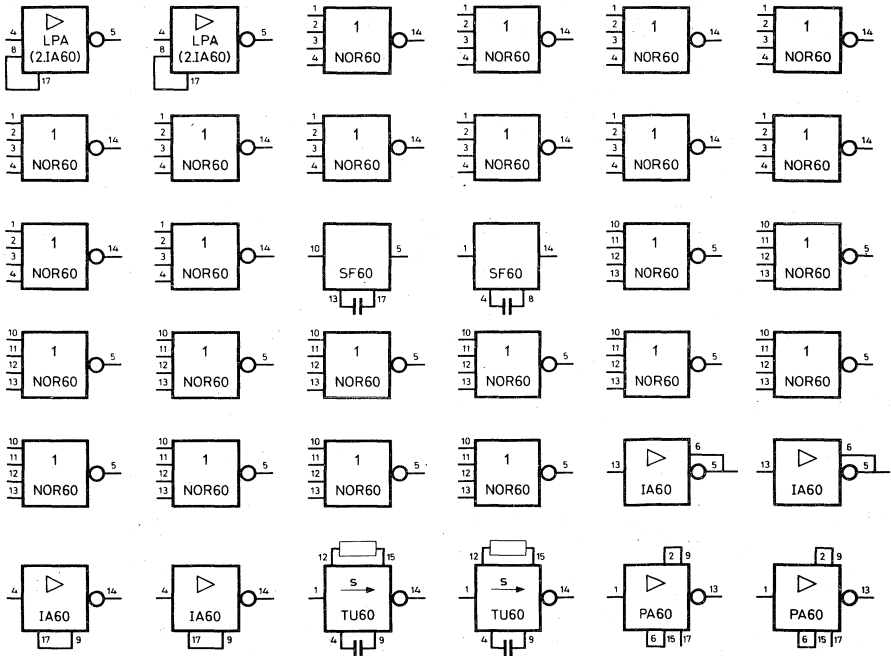
Application

Circuits for training purposes are given in Application Book "Control System Design Manual for 60-Series NORbits" under various headings.

CAUTION: Before plugging the SIM60 into the mains, be sure that the mains voltage selector on the panel is turned to the appropriate voltage.

STICKERS FOR THE 60-SERIES NORBITS

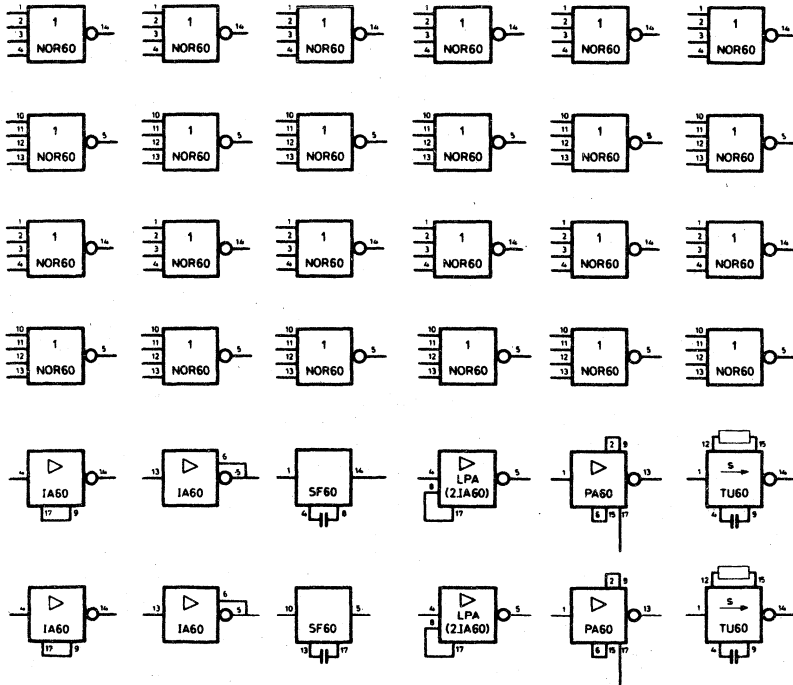
These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings. The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number of 50 sheets: 4322 026 36481.



Sticker sheet without 4.NOR60 or TT60

STICKERS FOR THE 60-SERIES NORBITS

These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings. The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71941.

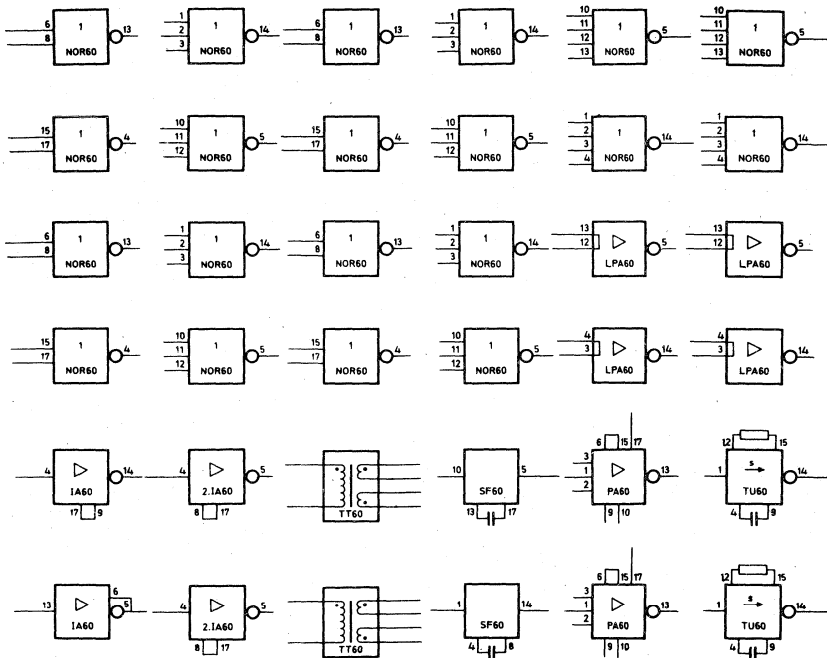


4322 026 71941

Sticker sheet without 4.NOR60 or TT60

STICKERS FOR THE 60-SERIES NORBITS

These are drawing symbols of NORBITS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings. The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71961.



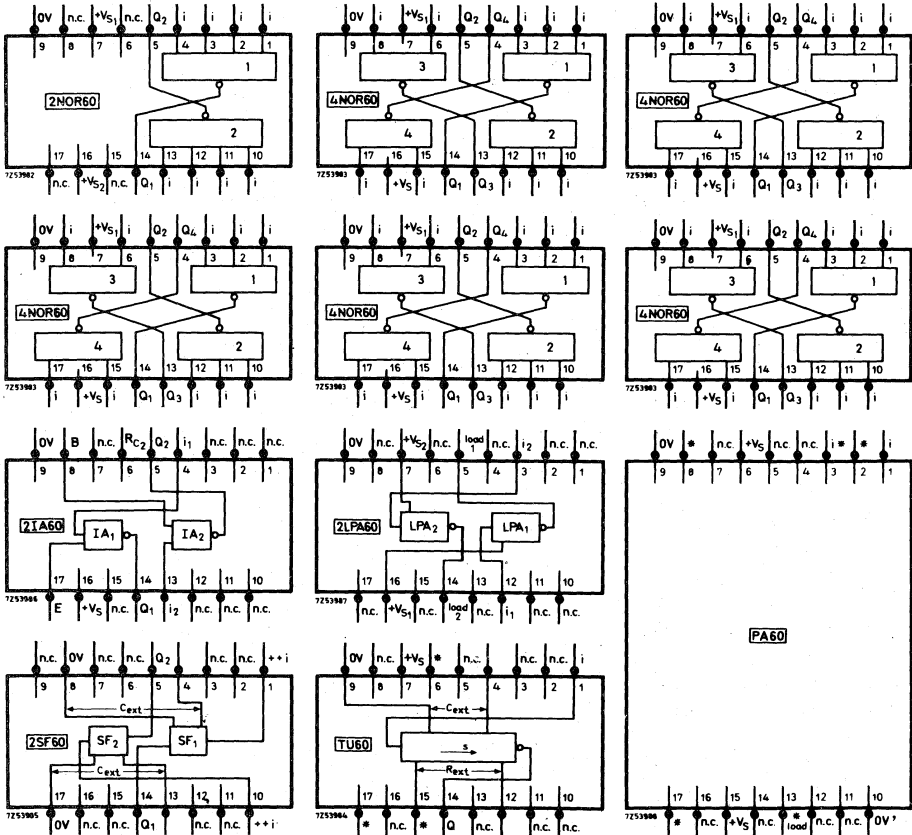
4322 026 71961

Sticker sheet with 4.NOR60 and TT60

WIRING LAYOUT STICKERS for the 60-series NORBITS

These are drawing symbols of 60-series blocks printed on self-adhesive, transparent material. They can be used for fast preparation of wiring layouts. All pin distances are actual size.

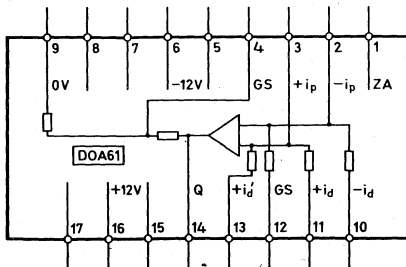
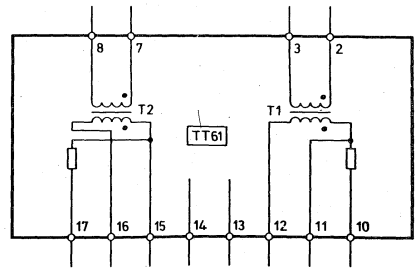
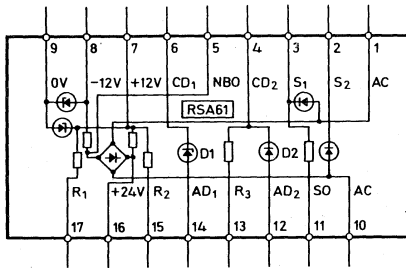
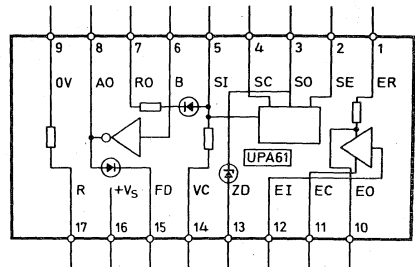
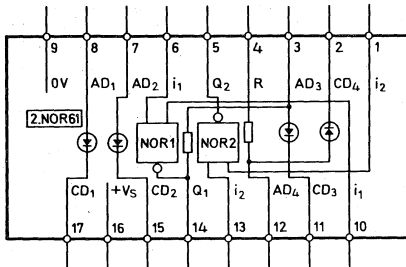
The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71971.



WIRING LAYOUT STICKERS for the 61-Series NORBITS

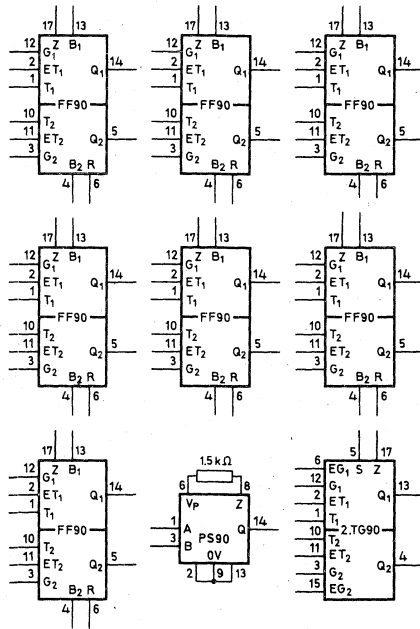
These are drawing symbols of 61-series blocks printed on self-adhesive, transparent material. They can be used for fast preparation of wiring layouts. All pin distances are actual size.

The stickers are available in sheets, each containing the five drawings shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 71981.



STICKERS FOR THE 90-SERIES CIRCUIT BLOCKS

These are drawing symbols of CIRCUIT BLOCKS printed on self-adhesive, transparent material. They can be used for fast preparation of system drawings. The stickers are available in sheets, each containing the arrangement of drawing symbols shown below. Each sticker can be separately detached from the sheet, without cutting. Catalogue number for 50 sheets: 4322 026 75541.



4322 026 75541

INPUT DEVICES



INTRODUCTION

Industrial control systems require compatible input devices that are capable of deriving signals representative of controlled or otherwise pertinent conditions. Though the information to be dealt with may take a variety of forms - e.g. presence, position, movement, rotation etc. - many different situations can be covered by a comparatively small selection of input devices.

The requirements of each situation determine the physical principle to be employed in the input device. For reasons of speed and reliability it is preferable to avoid mechanical contact in deriving the input signal, and often an all-static method of derivation is required. Experience with input devices has made it clear that skilful use of them can greatly improve machine output and reliability.

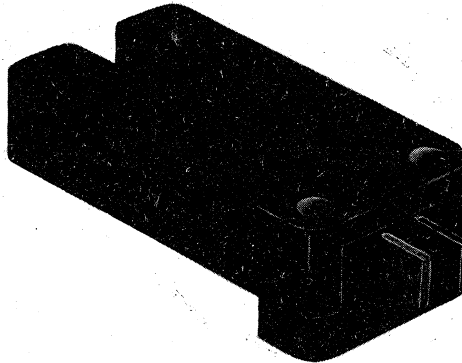
In this series the following units are available:

		page
Iron vane switched reed	IVSR	5
Electronic proximity detector	EPD	9
Proximity switched detector	PSD24	17

Data on input devices, and on output devices which are available for equipment production and for use in existing equipment, but are not recommended for equipment design (status C), are given in handbook CM7a.



IRON VANE SWITCHED REED



RZ21773-3

Maximum switching frequency
Operating-temperature range

100 Hz
-25 to +70 °C

APPLICATION

The iron vane switched reed can be applied as a limit switch, position indicator or as a signal source for low counting speeds.

In conjunction with d.c. amplifiers (UPA61, TT61 or TT60), the IVSR can be used for power switching.

As the IVSR is free from most of the difficulties encountered with mechanical switches, it can successfully replace micro switches.

CONSTRUCTION

The IVSR consists of a magnet and a reed switch encapsulated in an U-shaped plastic housing.

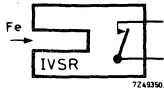
When there is no piece of iron (vane) in the gap between the reed switch and the magnet, the reed switch is closed. Inserting a piece of iron of suitable dimensions in the gap reduces the magnetic flux through the reed to such an extent that the reed switch opens.

In this way it is possible to obtain signals that indicate the position of the iron vane.

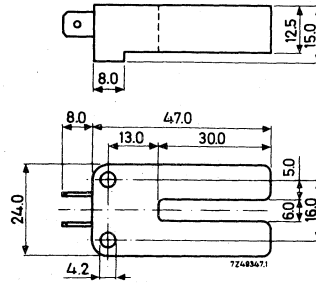
The weight is approximately 20 g.

The IVSR can be mounted in any position. Two mounting holes allow the use of 4 mm bolts. When IVSR's are mounted on a common support, the minimum distance between the housings is 36 mm, to avoid interaction. For mounting IVSR's over each other, this distance is 60 mm.

Connection can be made by means of 0,250" Fastons or by soldering.



Drawing symbol



Dimensions in mm

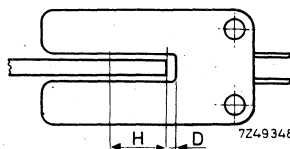
TECHNICAL PERFORMANCE

Load switching capacity (non inductive)	$\leq 1.2 \text{ VA}$
Voltage switching capacity	$\leq 32 \text{ V}_{dc}$
	$\leq 50 \text{ V}_{ac}$
Current switching capacity (non inductive)	$\leq 0.1 \text{ A}_{dc}$
Switching frequency	$\leq 100 \text{ Hz}$
Contact resistance, measured at 10 mV at open circuit	$< 150 \text{ m}\Omega$
Contact capacitance	$\leq 5 \text{ pF}$
Insulation resistance, measured at 250 V_{dc} at open circuit	$\geq 10^8 \Omega$
Test voltage, measured at open circuit for 1 min	500 V_{dc}
Permissible operating-temperature range	$-25 \text{ to } +70 \text{ }^\circ\text{C}$
Permissible storage-temperature range	$-40 \text{ to } +85 \text{ }^\circ\text{C}$

APPLICATION INFORMATION (typical values)

Vane material mild steel

The data given are based upon a movement of a mild steel vane 30 x 10 x 4 mm, placed centrally in the gap, in longitudinal direction.



The operating distance (D) is the distance between the front edge of the vane and the rear of the gap at which the reed switch opens.

The hysteresis (H) is defined as the distance between the vane position at which the reed switch opens and that at which the reed switch closes.

Operating distance 4 ± 3 mm

Hysteresis 10 ± 3 mm

APPLICATION SUGGESTIONS

As the reed switch is normally closed, the following two modes of operation can be distinguished:

- output voltage is present when there is no vane in the gap (Fig.a)
- output voltage is present when there is a vane in the gap (Fig.b)

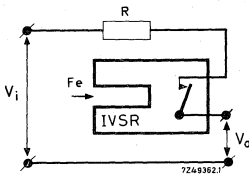


Fig.a

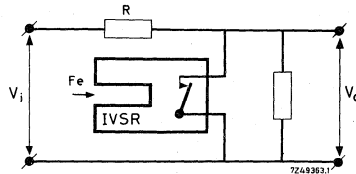


Fig.b

Notes

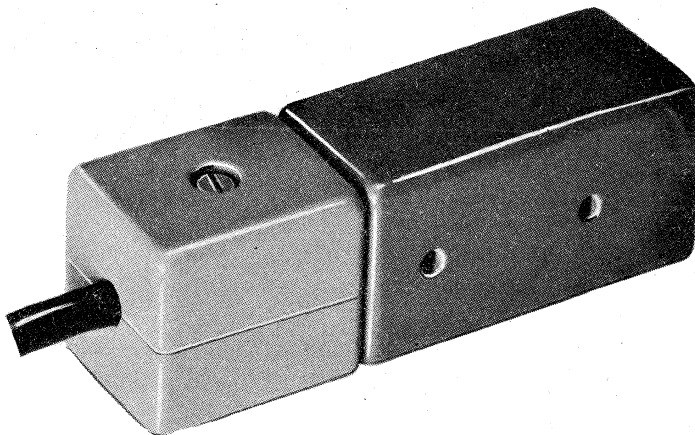
It is obvious that the IVSR should not be used in environments where iron dust or scraps might impair its operation.

It should be realised that capacitance directly across the switch terminals can be the cause of high currents through the switch at the moment of closing the contacts. This should be avoided by having sufficient resistance in the proper contact circuit.

In case the switch is used with electronic circuitry in which bounce might give rise to malfunctioning of the equipment, appropriate circuitry should be added to get rid of the bounce effect. The safe way out is the use of a one shot multivibrator.

Another solution that sometimes can be used, is applying a low pass RC network between the IVSR and the input of the equipment.

ELECTRONIC PROXIMITY DETECTOR



Supply voltage	12 V _{dc}
Maximum detection frequency	1 kHz
Operating-temperature range	-25 to +85 °C

GENERAL

The electronic proximity detector is a static switching device, the switching action being determined by the presence of a metallic object. The metal can be any electrically conducting material of rather arbitrary shape.

It can be applied as a detector for the presence, passage or position of metal parts and is a versatile tool in various industrial automation set-ups.

The EPD contains an oscillator which is link coupled to a detector. The detector is followed by an amplifier.

The oscillator coils and the coupling link are placed in a potcore half. In this way a well-defined field is set up in front of the open side of the potcore, located at the front side of the EPD. Bringing a piece of metal in this field the oscillator output and subsequently the output of the amplifier decreases, due to the loading effect of the eddy current losses in the metal.

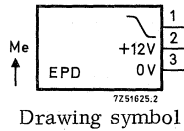
When no piece of metal is near, the output voltage of the EPD is approximately 12 V. It will decrease in proportion to the reduction of the oscillator output, resulting from a metal object coming nearer.

The complete circuit is epoxy encapsulated in a polycarbonate housing.

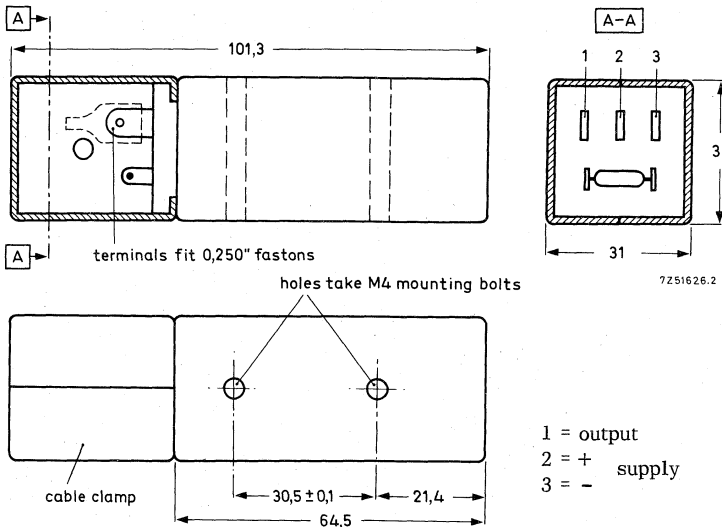
The mass is approximately 120 g.

The unit may be mounted in any position. Two mounting holes allow the use of 4 mm bolts.

Connection can be made by 0,250" Fastons or by soldering. A cable clamp consisting of two equal caps is supplied with each EPD. This clamp permits either end or top entrance of a 3-core cable of 7 mm diameter.



Dimensions in mm



Note

The resistor between the two 0,110" Fastons is an adjustment resistor for the oscillator loop gain; it should not be changed.

TECHNICAL PERFORMANCE

Supply voltage, V_s (d.c.)	12 V \pm 5% or +6 V \pm 5% and -6 V \pm 5% (with common 0 V) or 24 V via series resistor and 12 V zener diode, giving a stabilized supply voltage of 12 V. (See also Application Sug- gestions.)
limiting value	abs. max. 15 V* (destructive at $T_{amb} \geq 40$ °C)
Consumed current	max 17 mA
Output voltage, no object being detected object being detected	approximately $V_s - 0,5$ V max 100 mV
Output resistance no object being detected object being detected	700 Ω 3,4 k Ω
Hysteresis for output voltages of 100 mV - 11 V	0 mm
Output current no object being detected object being detected	max 14 mA max 3,7 mA
Maximum detection frequency, mark to space ratio 1 : 1	1 kHz
Noise (over supply lines)	< 10 mV
Ambient temperature range operating storage	-25 to +85 °C -40 to +85 °C

APPLICATION INFORMATION (typical values)**Detection graphs**

Detection of a rectangular mild steel reference object, 50 x 25 x 1 mm

Sensitive surface	surface of 31 x 31 mm at the opposite end of the EPD to the terminals
Axis	line perpendicular to the centre of the sensitive surface
Operating point	point at which the output voltage of the EPD is reduced to 100 mV (moment of detection)

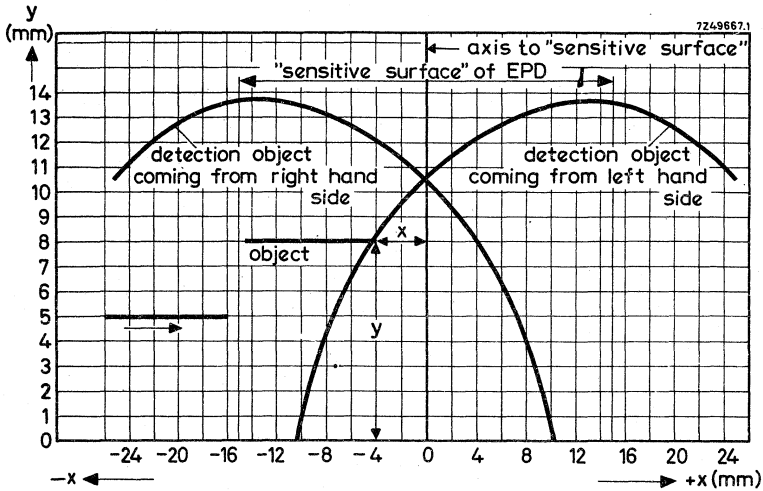
* Reversal of supply voltage will damage the detector.

Operating distance

distance of the leading edge of the reference object to the axis at the operating point (x-operating distance)

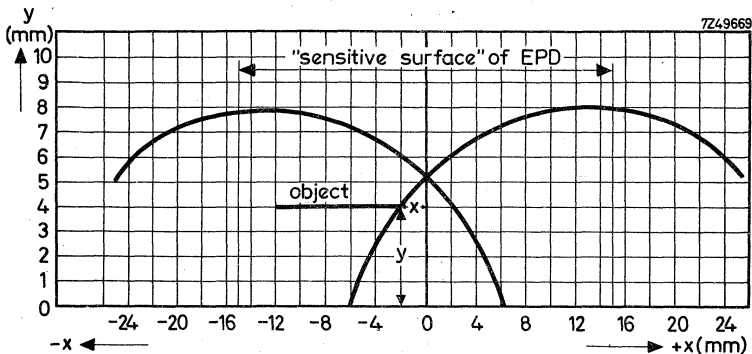
Detection range

distance of the reference object to the sensitive surface (y-operating distance)



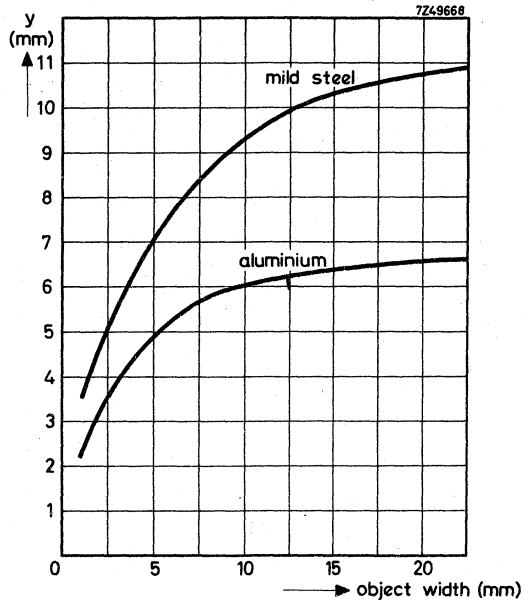
From the graph it can be seen that the object is detected before the axis is reached if it passes at a distance of < 10 mm from the sensitive surface. If it passes at a distance of e.g. 13.5 mm, the object is detected after the axis has been passed.

Detection of a rectangular aluminium reference object, 50 x 25 x 1 mm

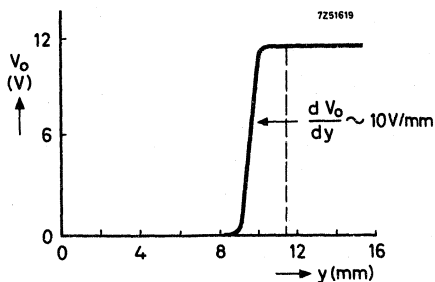


Detection of rectangular mild steel and aluminium reference objects (50 x 1 mm) with different widths

Object approaches the centre of the sensitive surface perpendicularly from in front.



Output voltage as a function of the position of a rectangular mild steel reference object, 50 x 25 x 1 mm



Upon frontal approach of the object to the sensitive surface, the output voltage of the EPD will change from over 11 V to 100 mV within 1 mm from the position in which the output voltage starts to change.

This characteristic is extremely important when the EPD is used as a position detector.

Notes:

The detection graphs may differ slightly from unit to unit.

Quite small objects can be detected when brought close to the sensitive surface. Thickness is relatively unimportant as eddy currents occur in penetration layer only.

Influence of supply voltage variations

A supply voltage variation of $\pm 5\%$ produces a change of ± 0.1 mm in y-operating distance, at 10 mm from the sensitive surface.

Influence of temperature

With the reference object at a y-operating distance of 10 mm (at -25°C) a change in temperature of both EPD and object will cause the y-operating distance to change less than 2 mm over the range from -25° to $+85^{\circ}\text{C}$.

Direction of approach

As the exterior field is rotation symmetrical the path along which the detection position is reached is immaterial.

Distance from metallic surroundings

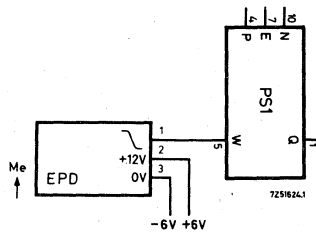
Clearance from metallic surrounding: 30 mm (this applies for sensitive front part of unit).

Spacing required between two detector axes with sensitive surface in the same plane: 60 mm.

Spacing required between two reference objects to give discrete detection: 50 mm. (This property can be put to use in feeder systems, a gap being used to initiate part supply restart.)

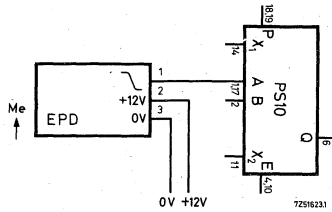
APPLICATION SUGGESTIONS *)

EPD in conjunction with 100 kHz-Series circuit blocks

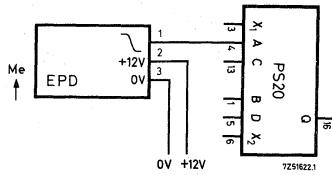


*) With long cables between EPD and subsequent electronics RC decoupling of interference can be employed.

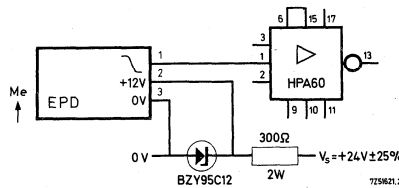
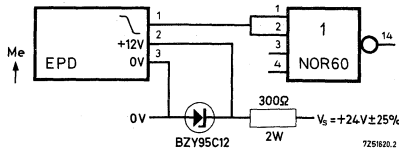
EPD in conjunction with 10-Series circuit blocks



EPD in conjunction with 20-Series circuit blocks

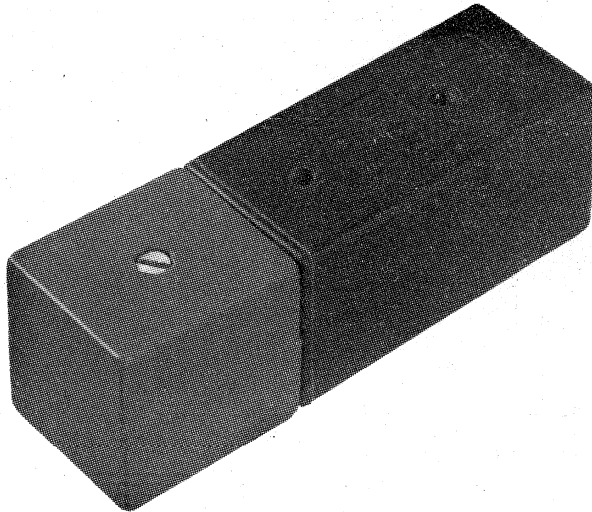


EPD in conjunction with 60-Series Norbits





PROXIMITY SWITCHED DETECTOR



Supply voltage	24 V (d.c.)
Maximum detection frequency	1 kHz
Operating temperature range	-25 to +85 °C

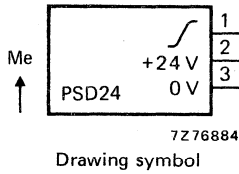
GENERAL

The proximity switched detector is a static switching device, the switching action being determined by the presence of a metallic object. The metal can be any electrically conducting material of rather arbitrary shape. It can be applied as a detector for the presence, passage or position of metal parts and is a versatile tool in various industrial automation set-ups.

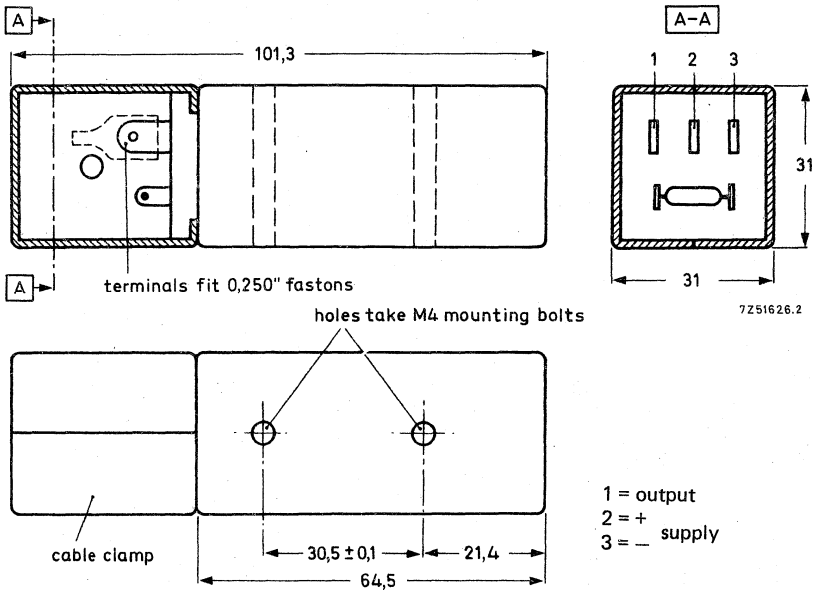
The unit contains an oscillator which is link coupled to a detector. The detector is followed by an amplifier. The oscillator coils and the coupling link are placed in a potcore half. In this way a well-defined field is set up in front of the open side of the potcore, located at the front of the PSD24. Bringing a piece of metal in this field decreases the oscillator output, and subsequently the output of the amplifier, due to the loading effect of the eddy current losses in the metal. When no piece of metal is near, the output voltage of the unit is maximum 300 mV (LOW). It will increase in proportion to the reduction of the oscillator output, resulting from a metal object coming nearer. When the piece of metal is close to the unit, the output voltage will be equal to the supply voltage (HIGH). The complete circuit is epoxy encapsulated in a polycarbonate housing. The mass is approximately 120 g. The unit may be mounted in any position. Two mounting holes allow the use of 4 mm bolts.

PSD24

Connection can be made by 0,250" Fastons or by soldering. A cable clamp consisting of two equal caps is supplied with each PSD24. This clamp permits either end or top entrance of a 3-core cable of 7 mm diameter.



Dimensions in mm



Note

The resistor between the two 0,110" Fastons is an adjustment resistor for the oscillator loop gain; it should not be changed.

TECHNICAL PERFORMANCE

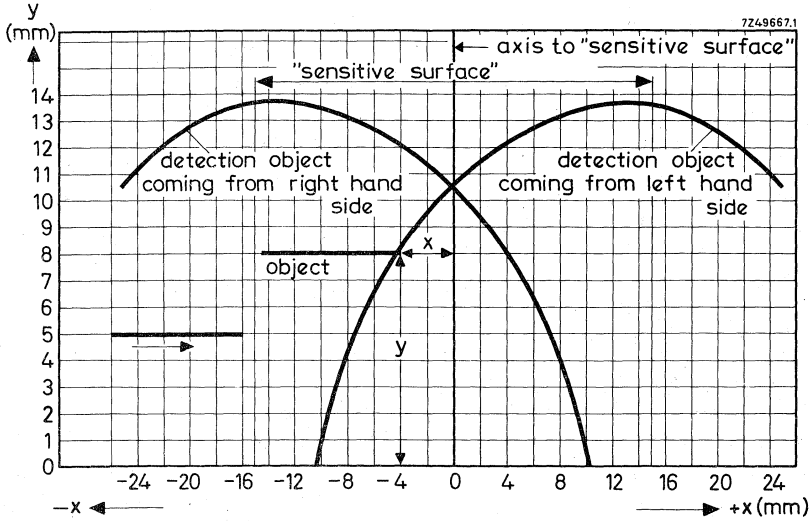
Supply voltage, V_s (d.c.)	24 V \pm 25%
Consumed current	max 24 mA
Output voltage, no object being detected	max 300 mV
object being detected	$\leq V_s$
Output impedance	
no object being detected	400 Ω
object being detected	8 k Ω
Hysteresis	0 mm
Output current	
no object being detected	—max 8 mA
object being detected	3 mA
Maximum detection frequency	
mark to space ratio 1 : 1	1 kHz
Noise (over supply lines)	< 10 mV
Ambient temperature range	
operating	—25 to +85 $^{\circ}\text{C}$
storage	—40 to +85 $^{\circ}\text{C}$

APPLICATION INFORMATION (typical values)**Detection graphs**

Detection of a rectangular mild steel reference object, 50 x 25 x 1 mm

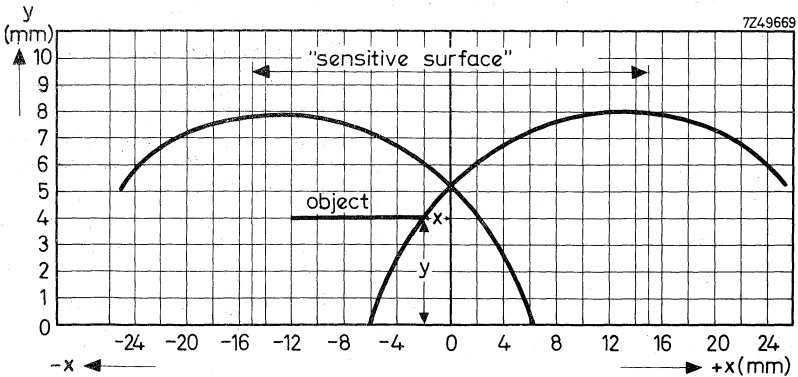
Sensitive surface	surface of 31 x 31 mm at the opposite end of the PSD24 to the terminals
Axis	line perpendicular to the centre of the sensitive surface
Operating point	point at which the open circuit output voltage of the PSD24 is switched to V_s (moment of detection)
Operating distance	distance of the leading edge of the reference object to the axis at the operating point (x-operating distance)
Detection range	distance of the reference object to the sensitive surface (y-operating distance)





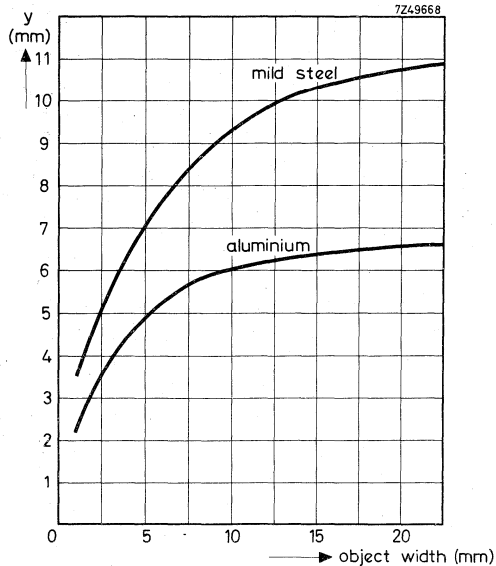
From the graph it can be seen that the object is detected before the axis is reached if it passes at a distance of < 10 mm from the sensitive surface. If it passes at a distance of e.g. 13,5 mm, the object is detected after the axis has been passed.

Detection of a rectangular aluminium reference object, 50 x 25 x 1 mm



Detection of rectangular mild steel and aluminium reference objects (50 x 1 mm) with different widths.

Object approaches the centre of the sensitive surface perpendicularly from in front.



Notes

The detection graphs may differ slightly from unit to unit.

Quite small objects can be detected when brought close to the sensitive surface. Thickness is relatively unimportant as eddy currents occur in penetration layer only.

The unit is sensitive to small movements and vibrations of the object when the output voltage is at an intermediate level.

Influence of supply voltage variations

A supply voltage variation of $\pm 25\%$ produces a change of $\pm 0,1$ mm in y-operating distance, at 10 mm from the sensitive surface.

Influence of temperature

With the reference object at a y-operating distance of 10 mm (at -25 °C) a change in temperature of both PSD24 and object will cause the y-operating distance to change less than 2 mm over the range from -25 ° to $+85$ °C.

Direction of approach

As the exterior field is radially symmetrical the path along which the detection position is reached is immaterial.

Distance from metallic surroundings

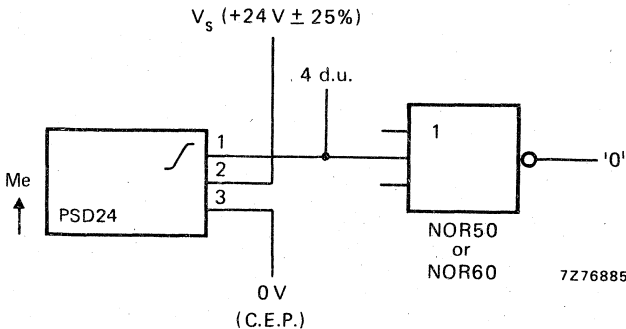
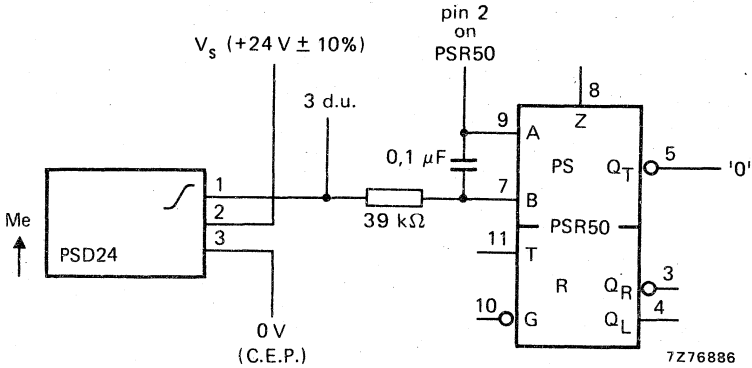
Clearance from metallic surrounding: 30 mm (this applies for sensitive front part of unit).

Spacing required between two detector axes with sensitive surface in the same plane: 60 mm.

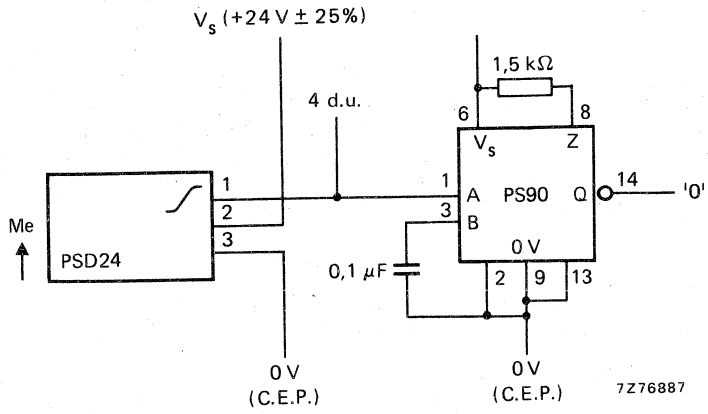
Spacing required between two reference objects to give discrete detection: 50 mm. (This property can be put to use in feeder systems, a gap being used to initiate part supply restart.)

APPLICATION SUGGESTIONS *

PSD24 in conjunction with a PSR50, a NOR50 or NOR 60 and a PS90 respectively. Outputs are shown for object being detected. C.E.P. = central earth point.



* With long cables between PSD24 and subsequent electronics RC decoupling of interference can be employed.



HYBRID INTEGRATED CIRCUITS



HYBRID INTEGRATED CIRCUITS FOR INDUCTIVE PROXIMITY DETECTORS

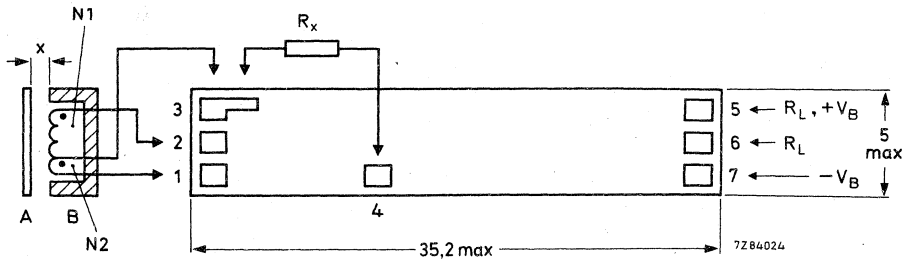
Hybrid integrated circuits intended for inductive proximity detectors in tubular construction, especially the M8 hollow stud. The OM286 is for positive and the OM287 for negative supply voltage. The circuit consists of an oscillator, a rectifier stage, a level switch and an output stage, which is suitable, e.g. for driving the coil of an electromagnetic relay. The output transistor is protected against transients from the inductive load by a voltage regulator diode. The circuit is protected against false polarity connection of the supply voltage. The device is a thick-film circuit deposited on a ceramic substrate. It may be potted, together with the oscillator coil and a resistor (R_x), in a non-magnetic tube.

QUICK REFERENCE DATA

D.C. supply voltage range	V_B	4,5 to 30 V
Output current at $V_B > 24$ V	I_O	max. 250 mA
Switching distance; depends on R_x and oscillator coil	x	typ. 1 to 5 mm
Hysteresis in switching distance	Δx	3 to 10 %
Switching frequency	f	< 5 kHz
Operating ambient temperature range	T_{amb}	-40 to +85 °C*

MECHANICAL DATA

Dimensions in mm



A = metal actuator
B = open potcore or potcore half with coil

Fig. 1 Mechanical outline and connections. Note that the supply polarities to points 5 and 7 are given for the OM286; for OM287 the polarities are, point 5 $-V_B$ and point 7 $+V_B$. x is the switching distance. The maximum height of the circuits including the substrate thickness is 1,7 mm.

* The tube potting material and connection material are the main limiting factors for the operating ambient temperature range of the complete module.

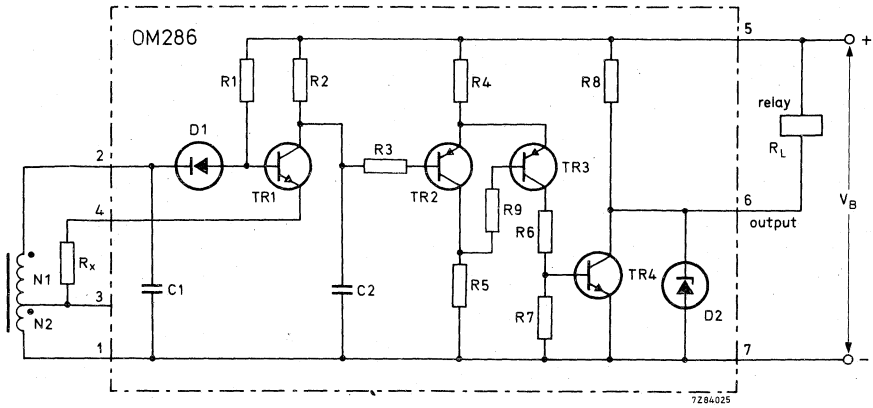


Fig. 2 Circuit diagram of OM286.

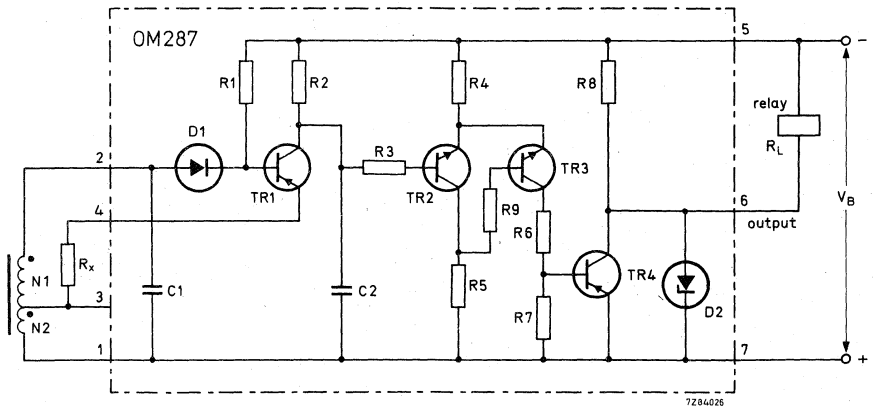


Fig. 3 Circuit diagram of OM287.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

D.C. supply voltage	V_B	max.	30 V
Output current	I_O	max.	250 mA
Storage temperature range	T_{stg}		-40 to + 125 °C
Operating ambient temperature range	T_{amb}		-40 to + 85 °C

CHARACTERISTICS

Conditions (unless otherwise specified)

D.C. supply voltage	V_B	4,5 to 30 V
Output current		see Fig. 4
External resistance of oscillator	R_X	see switching distance below
Operating ambient temperature range (potted)	T_{amb}	-25 to + 65 °C

Performance

Supply current (output current not included)

$V_B = 24 \text{ V}$

I_B	typ.	7 mA
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Output voltage low (attenuated)

$V_B = 24 \text{ V}; R_L = 120 \Omega$

V_{OL}	<	1 V
----------	---	-----

$V_B = 5 \text{ V}; R_L = 500 \Omega$

V_{OL}	<	0,25 V
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Output voltage high (non-attenuated)

V_{OH}	≈	V_B
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Switching distance *

type	oscillator coil number of turns		average switching distance x (mm) at R_X (Ω)			recommended potcore	oscillator frequency kHz
	N1	N2	200	250	300		
M8	32	16	1	1,5	—	ϕ 5,8 mm (Neosid)	≈ 800
M12	40	10	2	3	—	P9-3B7/3H1	≈ 600
M18	46	4	3	4	5	P14-3B7/3H1	≈ 600

Hysteresis in switching distance

Δx		3 to 10 %
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Switching frequency

f	<	5 kHz
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* The switching distance x depends on the oscillator coil, the material of the metal actuator and R_X . For measuring purposes a square steel sheet with dimensions such that a circle with the diameter of the core can be inscribed, and 1 mm thickness can be used. R_X must not be chosen outside the range 180 to 400 Ω . Influence of supply voltage: 1 $\mu\text{m}/\text{V}$.

Temperature coefficient:

M8: 0,2 %/°C

M12: 0,17%/°C

M18: 0,1 %/°C.

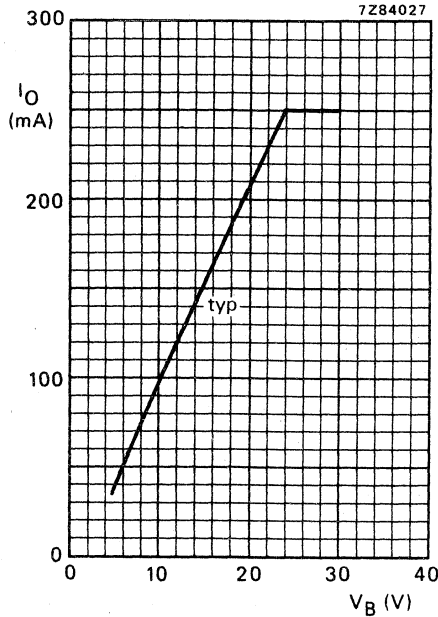
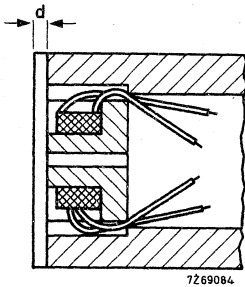


Fig. 4 Maximum allowable output current as a function of supply voltage.

MOUNTING RECOMMENDATIONS



If a protective plastic cap is incorporated, it should be as thin as possible, because its thickness d forms part of the switching distance x .

The brass stud wall should not extend beyond the potcore. If no brass tube is used, the switching distances increase by at least 25%. The exact value with its spread is determined by a number of variables, e.g.

- value of the adjustment resistor R_x
- the oscillator coil
- hysteresis
- the metal of the actuator
- the stud housing (if any).

Fig. 5 Insertion of potcore in brass tube.

Soldering recommendations

Use normal 60/40 solder with 2 to 4% silver; use solder-iron with a fine point; soldering time as short as possible.

Potting recommendations

First cover the hybrid IC with about 0,5 mm of DC3140 (Dow Corning), let it harden and then, when the parts are inserted in the tube, fill up the tube with Stycast 2850 (Emerson and Cuming).

Heat transfer

The module may be used at maximum voltage/current conditions at a substrate temperature of 85 °C. When potted the heat transfer improves slightly.

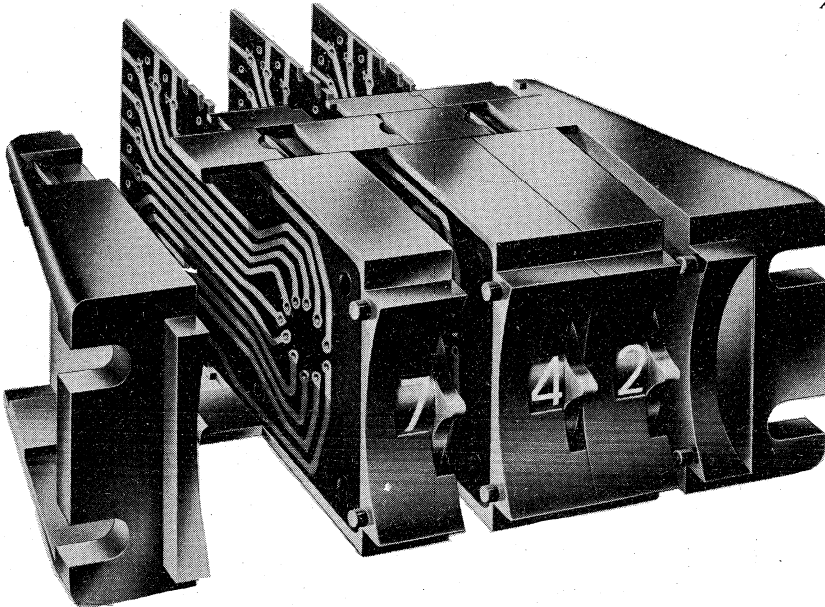
PERIPHERAL DEVICES



THUMBWHEEL SWITCHES M version

QUICK REFERENCE DATA	
Contact resistance	$\leq 100 \text{ m}\Omega$
Operating temperature range	
paper epoxy p. w. board	-25 to +70 °C
glass epoxy p. w. board	-55 to +85 °C
Current switching capability	0,5 A

A 52941 - 2



APPLICATION

These miniature thumbwheel switches have been developed for use as preset devices in digital systems which have to handle numerical data, or as positioning switches.

The dimensions of the M version are smaller than those of the T and the B versions and allow for easy operation.

CONSTRUCTION

Thumbwheel switches

Housing	black shock-resistant polycarbonate
Contact springs	heat-treated phosphor bronze
Contact surface	721 alloy
Terminals	holes or tin-plated pins for wire wrapping
Thumbwheel	black polycarbonate provided with white figures or signs
Thumbwheel detent	steel spring
Printed-wiring board	paper epoxy or glass epoxy, gold-plated tracks on nickel
Stacking	switch housings are provided with "snap-in" hooks to eliminate tie bolts
Type identification	catalogue number suffix (last 5 digits) is given on the rear of the switch

End pieces

Housing	black shock-resistant polycarbonate
Types	for mounting with screws for mounting with brackets (rear mounting)



Outlines

Dimensions in mm

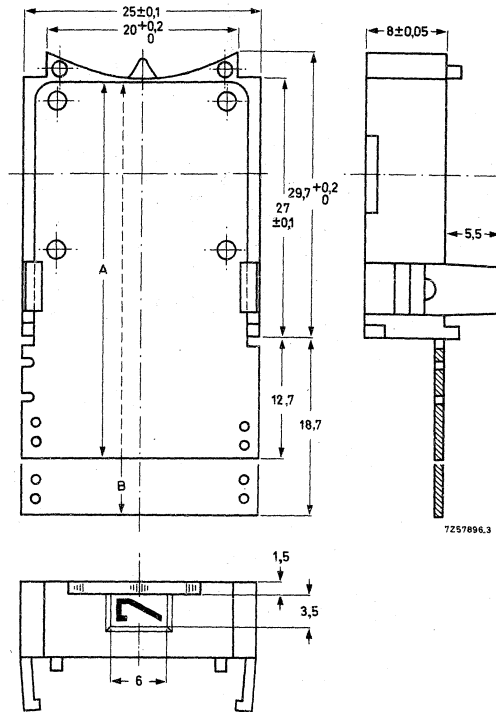


Fig. 1.

Thumbwheel switch,

A : short track plate, used in switches without diodes

B : long track plate, used in switches with diodes, and in type M10P2C.

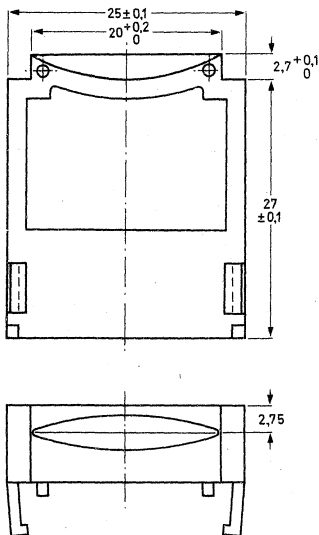


Fig. 2. Spacer.

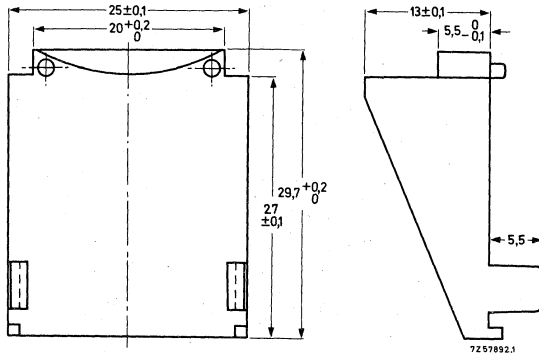


Fig. 3. Male end-piece for mounting with screws to the panel.

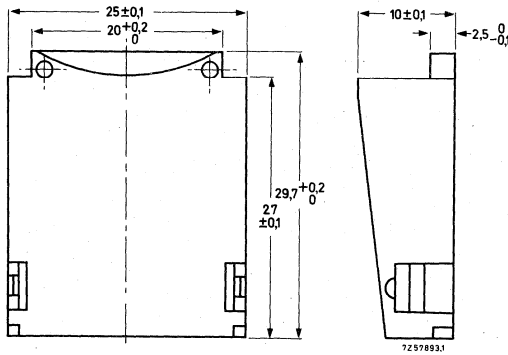


Fig. 4. Female end-piece for mounting with screws to the panel.

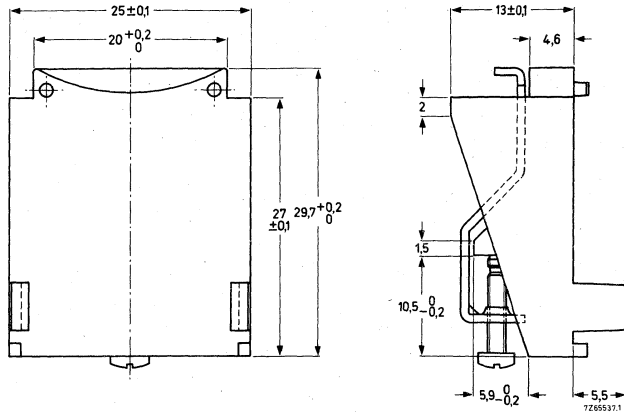


Fig. 5. Male end-piece with brackets.

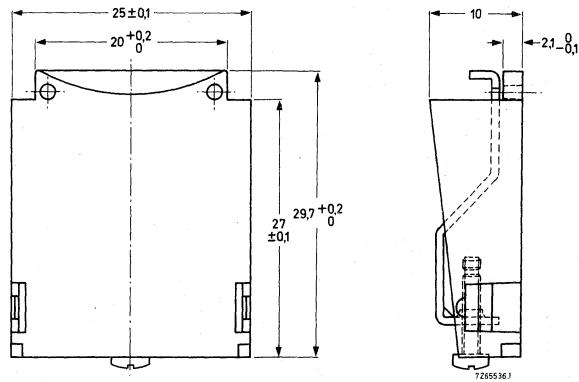


Fig. 6. Female end-piece with brackets.

Terminals

The switches are supplied with holes or with pins (Fig. 7) for connection.

They can be connected:

- a. by soldering to the holes in the printed-wiring board
- b. by wire-wrapping the pins (AWG26)
- c. by reflow soldering the pins to a perpendicular external printed-wiring board ($250 \pm 2 \text{ }^\circ\text{C}$, max. 6 s)

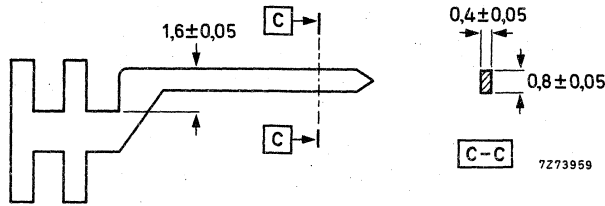


Fig. 7. Outlines of the pins for wire-wrapping.

The pitch of the holes on the p.w. board depends on the number of connections.

- for 10 connections or less (in general switches presenting only binary or only complementary output) the pitch is 2,54 mm or its multiple.
If these switches are provided with pins, these pins are in line in position B as indicated in Fig. 8.

- for more than 10 connections the pitch is 2,3 mm or its multiple.
If the switches are provided with pins, these pins are staggered according to Figs 8 and 9, to allow enough room for wire-wrapping tools.

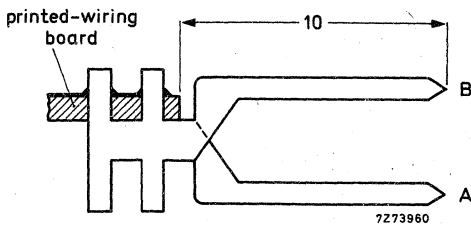


Fig. 8

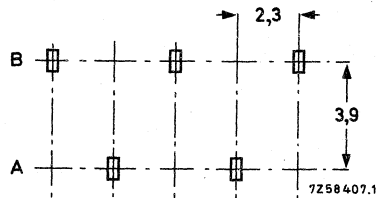


Fig. 9

Mass 10 g approximately

Numerals

	height x width (mm)	line thickness (mm)
10 position switch	5 x 3	0,7
12 position switch, 0 to 9	4 x 2,4	0,7
10	3,8 x 3,1	0,45
11	3,8 x 2,2	0,45

Mounting

The switches are "block mounted" to the panel with M3 screws or with mounting brackets, depending on the end-pieces used. Maximum permissible couple applied to the screws in the brackets 250 mNm.

Panel cut-outs for the two types are shown below. N = number of switches.

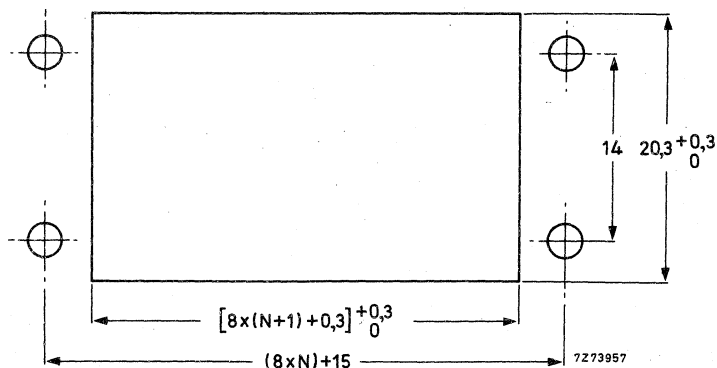


Fig. 10. Panel cut-out for switches and end-pieces for mounting with four M3 screws.

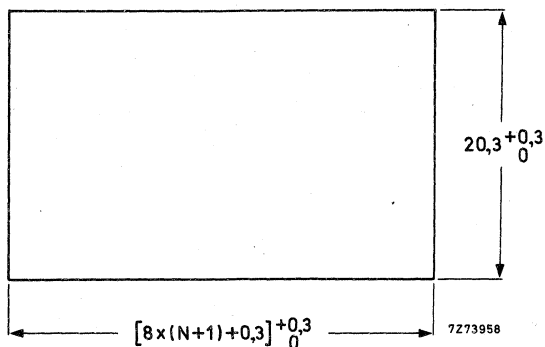


Fig. 11. Panel cut-out for switches and end-pieces with brackets.

TECHNICAL PERFORMANCE

D. C. working voltage	250 V
D. C. test voltage	750 V
Insulation resistance, measured at 100 V (d. c.) ¹⁾	
NM version ²⁾	10 ⁴ MΩ
M version ³⁾	10 ⁵ MΩ
After humidity test	
NM version ²⁾	10 ² MΩ
M version ³⁾	10 ³ MΩ
Power switching capability at resistive load	10 VA
Current switching capacity (d. c.) in purely resistive circuits	0,5 A
Maximum current carrying capacity (d. c.)	3 A
Contact resistance measured at 10 mA	< 100 mΩ
Capacitance measured at 1 MHz between one terminal and all others connected to earth	10 pF
Standard gate resistor	6,8 kΩ
Operating temperature range	
NM version ²⁾	-25 to +70 °C
M version ³⁾	-55 to +85 °C
Storage temperature range	
NM version ²⁾	-40 to +85 °C
M version ³⁾	-65 to +100 °C
Life	in excess of 10 ⁶ commutations at a rate of 1 step/s
Operating torque	10 to 35 mNm
Quality control tests, IEC 68-2:	
test Aa, cold	-55 °C
test Ba, dry heat	100 °C
test C, damp heat	56 days
test F, vibration	10 to 2000 Hz; 1,5 mm; 10g
test Na, temperature cycling	-55 to +100 °C
test Ea, shock	100g
test T, solderability	0 hours and 56 days

¹⁾ Between any pair of terminals and between any terminal and all others connected together.

²⁾ Paper epoxy printed-wiring board.

³⁾ Glass epoxy printed-wiring board.

SURVEY OF TYPES

description	type *)	catalogue number
<u>Decimal switches</u>		
10 position/1 common, engraving 0 to 9	M10P 1C MW 10P 1C NM10P 1C	4311 027 84000 4311 027 84010 4311 027 90130
10 position/2 commons, engraving 0 to 9	M10P2C	4311 027 84040
5 x 2 positions/1 common, engraving + -	M5x2P 1C + - MW5x2P 1C + -	4311 027 84940 4311 027 84950
5 x 2 positions/2 commons, engraving + -	M5x2P2C + - MW5x2P2C + -	4311 027 84920 4311 027 84930
<u>Coding switches 1.2.4.8</u>		
binary output	NM1248 NMW 1248	4311 027 90230 4311 027 90520
binary + complementary output	M1248C MW 1248C	4311 027 84160 4311 027 84290
complementary output	NM1248CS NMW 1248CS	4311 027 90250 4311 027 90360
<u>Decoding switches 1.2.4.8, positive logic</u>		
binary output	NM1248P NMW 1248P	4311 027 90270 4311 027 90220
binary + complementary output	M1248PC MW 1248PC	4311 027 84240 4311 027 84250
complementary output	NM1248PCS NMW 1248PCS	4311 027 90810
<u>Decoding switches 1.2.4.8, negative logic</u>		
binary output	NM1248N NMW 1248N	4311 027 90830 4311 027 90310
binary + complementary output	M1248NC MW 1248NC	4311 027 84200 4311 027 84210
complementary output	NM1248NCS NMW 1248NCS	4311 027 90880

Note: Many types with additional properties mentioned under "Special versions" on next page, are included in our programme and are in current production or available from stock. Please contact the supplier if a version is required which is not present in the "Survey of types".

*) "N" in front of the number indicates that the switch has a paper epoxy printed-wiring board. This material is only used for single-sided boards. Double-sided boards, used in switches with binary and complementary output, are made of glass epoxy. Switches with single-sided glass epoxy printed-wiring boards can be supplied on request. "W" in the number indicates that the switch is provided with pins for wire wrapping.

ACCESSORIES

Set of two end-pieces with screws	4311 027 84440
with brackets	4311 027 88800
Spacer	4311 027 84590
Spacer with decimal point	4311 027 84910

SPECIAL VERSIONS

Internally lit switches

White translucent rotor with black engraving. Lamp max. 5 V. Minimum life time 50 000 h (about 6 years). Lower voltage (applicable in dark room) extends the life time. Type number prefix is extended with an "L", for example LNM1248.

Limit stops

Rotation of the rotor can be limited to any position by means of stop pins (catalogue number 4311 027 84410). These are specially tooled parts which can be fitted by means of a pair of tweezers.

The stop pins can be installed by factory (or by customer).

Sealed switches

Contact chamber is sealed by an elastomer ring for protection against dust and sand. May be used in explosive and aggressive atmospheres. Type number prefix is extended with an "S", for example SNM1248.

Colour of housing/rotor

Rotors also available in red. Type number prefix is extended with an "R", for example RNM1248.

Other colours for rotor and housing can be considered, but only for order quantities in one batch and one colour of 10 000 pieces or more.

Special engraving

Special engraving requirements can be undertaken.

Due to cost of specific tooling, a minimum quantity of 5000 is recommended.

Twelve-position switches

All switches can also be supplied with twelve positions on request. The symbols on the rotor are then smaller, however, the housing and the window are the same.

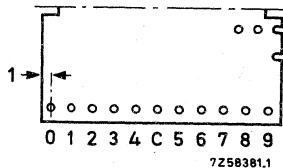
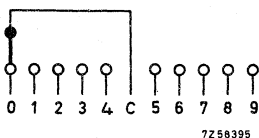
Pins for wire-wrapping

All switches can be equipped with these pins (see under "Terminals"). Type number prefix is extended with a "W", for example NMW1248N.

DIAGRAMS AND TERMINAL LOCATION

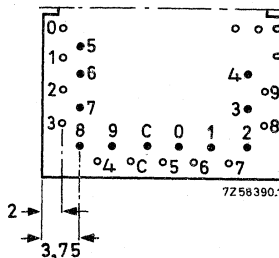
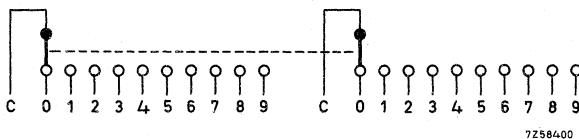
The terminals are shown at the solder side of the printed-wiring board. This is the side facing the housing. Two terminals are reserved for connection of a supply to the lamp in internally lit switches.

M10P1C, MW10P1C, NM10P1C



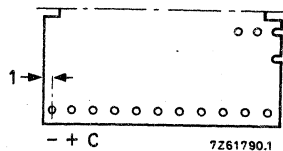
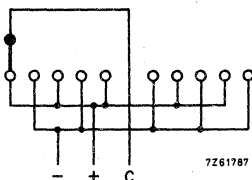
Pitch between holes is 2,30 mm.
Wrapping pins are staggered with the most left in position B (Fig. 8).

M10P2C



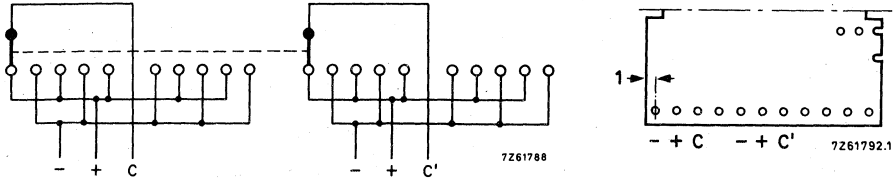
Pitch between holes is 2,30 mm.

M5x2P1C+-, MW5x2P1C+-



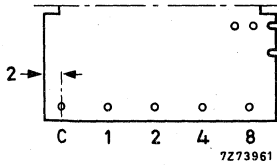
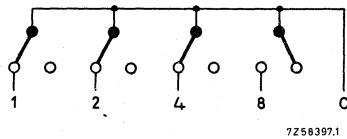
Pitch between holes is 2,30 mm.
Pins are staggered in positions B-A-B successively (Fig. 8).

M 5x2 P2C+-, MW 5x2 P2C+-



Pitch between holes is 2,30 mm.
Pins are staggered in positions
B-A-B (2x) successively (Fig. 8).

NM1248, NMW1248

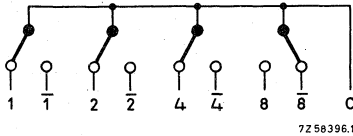


Pitch between holes is 5,08 mm.
Pins are in line in position B (Fig. 8).

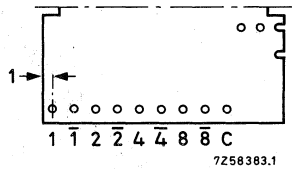
Truth table

Index	1 2 4 8
0	0 0 0 0
1	1 0 0 0
2	0 1 0 0
3	1 1 0 0
4	0 0 1 0
5	1 0 1 0
6	0 1 1 0
7	1 1 1 0
8	0 0 0 1
9	1 0 0 1

M1248C, MW1248C



7258396.1



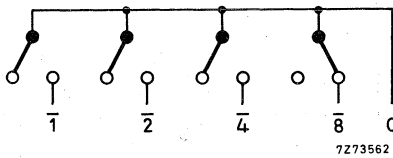
7258383.1

Pitch between holes is 2,30 mm.
Pins are staggered, with the most left in position B (Fig. 8).

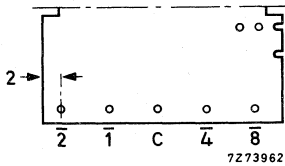
Truth table

Index	1 2 4 8	1̄ 2̄ 4̄ 8̄
0	0 0 0 0	1 1 1 1
1	1 0 0 0	0 1 1 1
2	0 1 0 0	1 0 1 1
3	1 1 0 0	0 0 1 1
4	0 0 1 0	1 1 0 1
5	1 0 1 0	0 1 0 1
6	0 1 1 0	1 0 0 1
7	1 1 1 0	0 0 0 1
8	0 0 0 1	1 1 1 0
9	1 0 0 1	0 1 1 0

NM1248CS, NMW1248CS



7273562



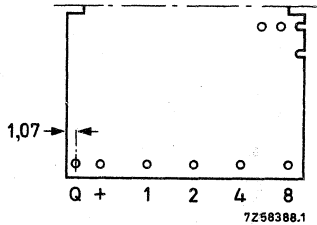
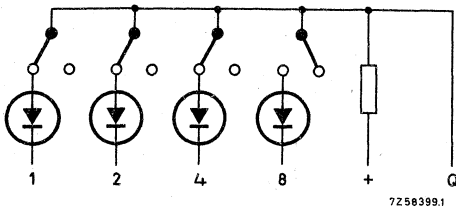
7273962

Pitch between holes is 5,08 mm.
Pins are in line in position B (Fig. 8).

Truth table

Index	2̄ 1̄ 4̄ 8̄
0	1 1 1 1
1	0 1 1 1
2	1 0 1 1
3	0 0 1 1
4	1 1 0 1
5	0 1 0 1
6	1 0 0 1
7	0 0 0 1
8	1 1 1 0
9	0 1 1 0

NM1248P, NMW1248P

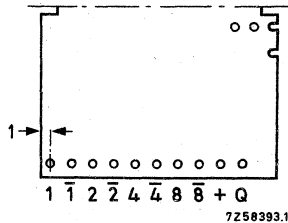
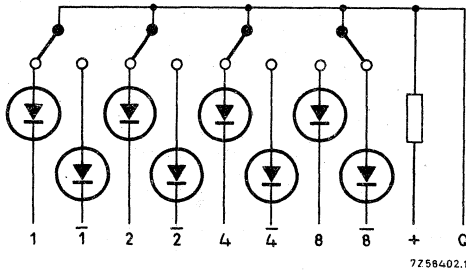


Pitch between holes is 2,54 mm and 5,08 mm.
Pins are in line in position B, except the Q
terminal (Fig. 8).

Truth table

Index	1 2 4 8
0	0 0 0 0
1	1 0 0 0
2	0 1 0 0
3	1 1 0 0
4	0 0 1 0
5	1 0 1 0
6	0 1 1 0
7	1 1 1 0
8	0 0 0 1
9	1 0 0 1

M1248PC, MW1248PC



Pitch between holes is 2,30 mm.
Pins are staggered with the most
left in position B (Fig. 8).

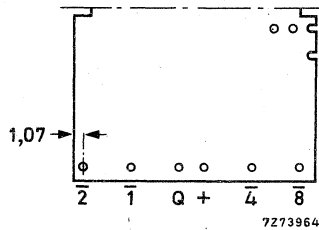
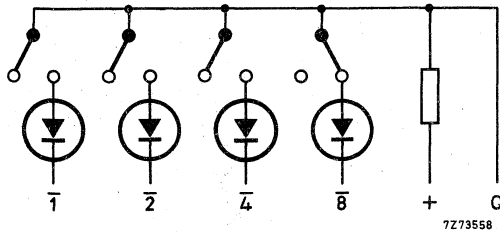
Truth table

Index	1 2 4 8	$\bar{1} \bar{2} \bar{4} \bar{8}$
0	0 0 0 0	1 1 1 1
1	1 0 0 0	0 1 1 1
2	0 1 0 0	1 0 1 1
3	1 1 0 0	0 0 1 1
4	0 0 1 0	1 1 0 1
5	1 0 1 0	0 1 0 1
6	0 1 1 0	1 0 0 1
7	1 1 1 0	0 0 0 1
8	0 0 0 1	1 1 1 0
9	1 0 0 1	0 1 1 0

THUMBWHEEL SWITCHES
M version

4311 027 84...-
4311 027 90...

NM1248PCS, NMW1248PCS

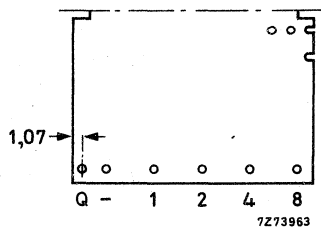
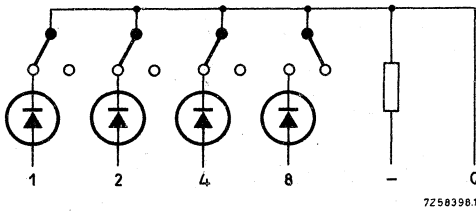


Pitch between holes is 5,08 and 2,54 mm.
Pins are in line in position B (Fig. 8).

Truth table

Index	$\bar{1}$	$\bar{2}$	$\bar{4}$	$\bar{8}$
0	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9	0	1	1	0

NM1248N, NMW1248N

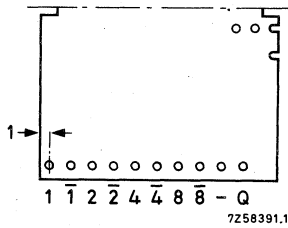
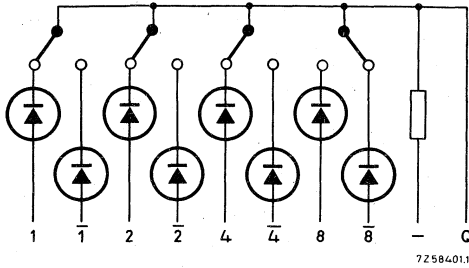


Pitch between holes is 2,54 mm and 5,08 mm.
Pins are in line in position B, except the Q terminal.

Truth table

Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1

M1248NC, MW1248NC

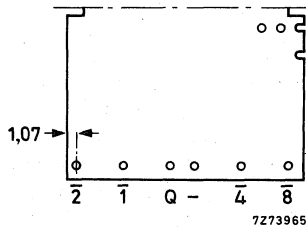
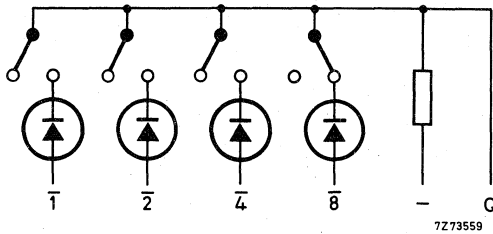


Pitch between holes is 2,30 mm.
Pins are staggered with the most
left in position B (Fig. 8).

Truth table

Index	1 2 4 8	$\bar{1} \bar{2} \bar{4} \bar{8}$
0	0 0 0 0	1 1 1 1
1	1 0 0 0	0 1 1 1
2	0 1 0 0	1 0 1 1
3	1 1 0 0	0 0 1 1
4	0 0 1 0	1 1 0 1
5	1 0 1 0	0 1 0 1
6	0 1 1 0	1 0 0 1
7	1 1 1 0	0 0 0 1
8	0 0 0 1	1 1 1 0
9	1 0 0 1	0 1 1 0

NM1248NCS, NMW1248NCS



Pitch between holes is 5,08 mm and 2,54 mm.
Pins are in line in position B (Fig. 8).

Truth table

Index	$\bar{1} \bar{2} \bar{4} \bar{8}$
0	1 1 1 1
1	0 1 1 1
2	1 0 1 1
3	0 0 1 1
4	1 1 0 1
5	0 1 0 1
6	1 0 0 1
7	0 0 0 1
8	1 1 1 0
9	0 1 1 0

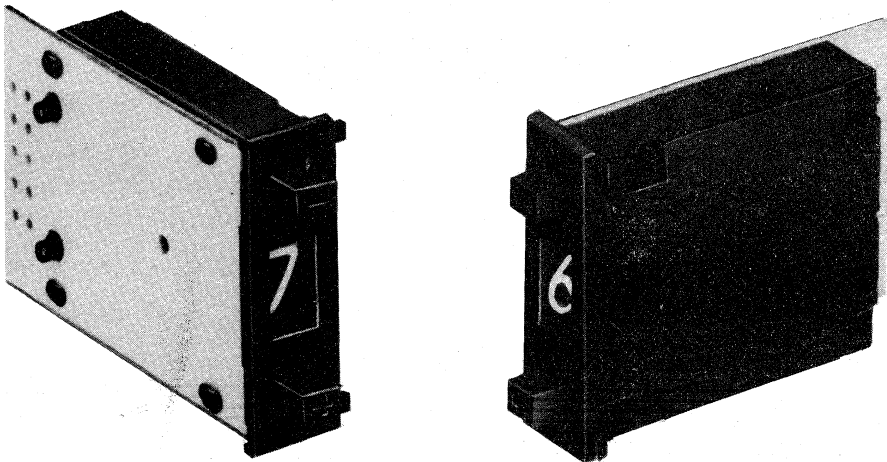
THUMBWHEEL SWITCHES

F version

QUICK REFERENCE DATA

Contact resistance	$\leq 100 \text{ m}\Omega$
Temperature range operating	-25 to +70 °C
storage	-25 to +85 °C
Current switching capability	0,5 A

780602-18-01



APPLICATION

These miniature thumbwheel switches have been developed for use as preset devices in digital systems which have to handle numerical data, or as positioning switches. They are operated by means of push buttons marked + (below) and - (above). Two versions are available: a version with 10 positions, and one with 16 positions, both for front mounting.

CONSTRUCTION**Thumbwheel switches**

Housing

black shock-resistant polycarbonate, face satined,
figures behind transparent window

Contact springs

phosphor-bronze

Contact surface

721 alloy

Terminals

holes in printed-wiring pads

Thumbwheel

black polyamide provided with white figures
(or letters above 10th position)

Thumbwheel detent

stainless steel spring

Printed-wiring board

glass epoxy in two lengths, nickel tracks, terminals are
marked

Stacking

switch housings are snapped together side by side

Type identification

catalogue number suffix (last 5 digits) is given on
the rear of the switch**End pieces**

Material

black sprung plastic, self-locking

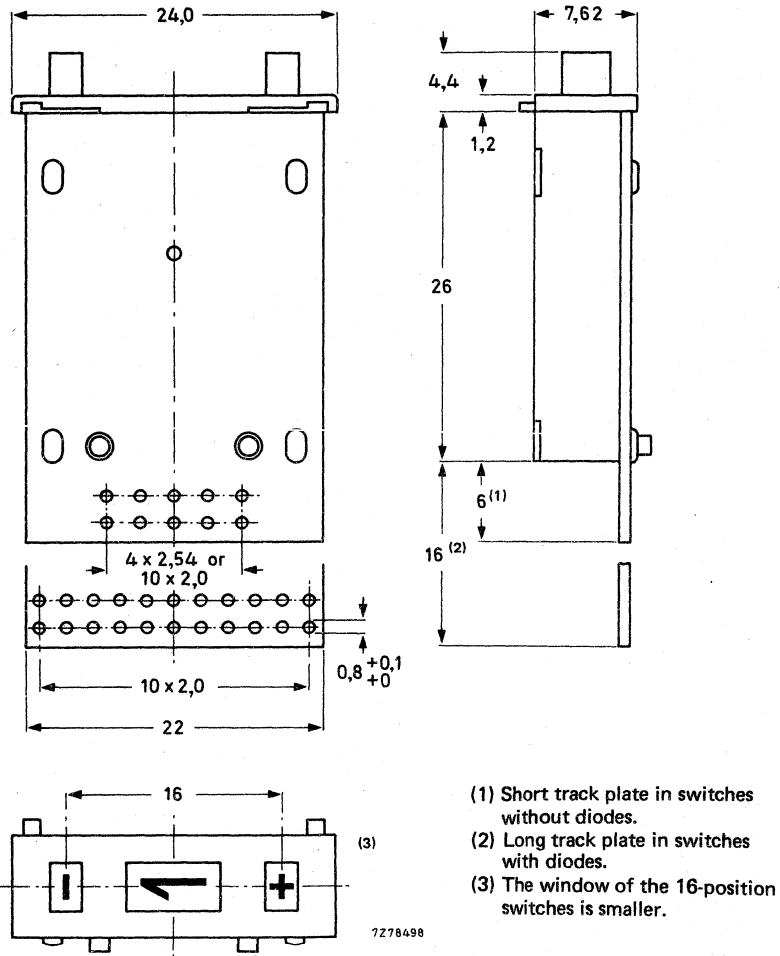
Types

left-hand and right-hand models



Outlines

Dimensions in mm



- (1) Short track plate in switches without diodes.
- (2) Long track plate in switches with diodes.
- (3) The window of the 16-position switches is smaller.

Fig. 1.

Numerals

	height	width
10-position switch	5	3
16-position switch	3	1,9

Fig. 2 End-piece for mounting at the left.

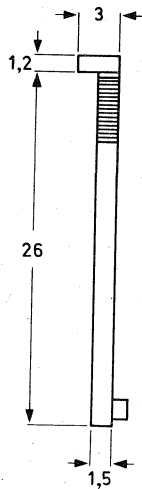
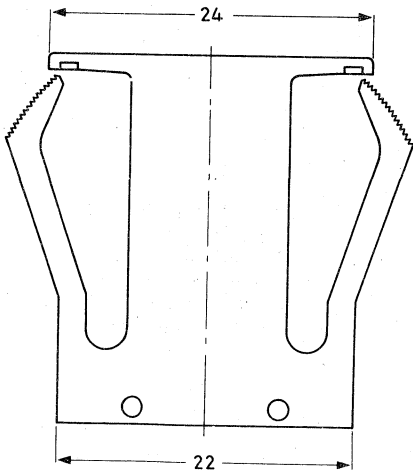
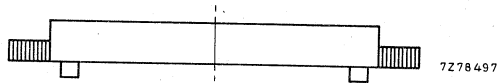
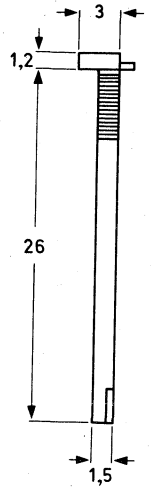
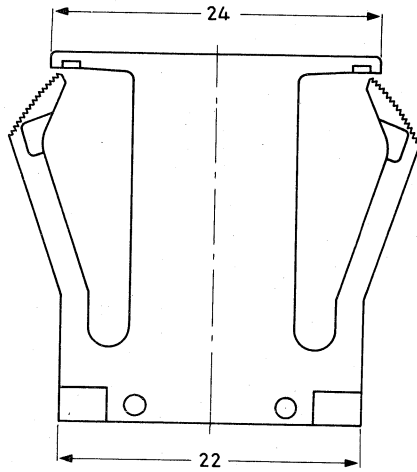
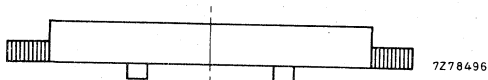


Fig. 3 End-piece for mounting at the right.



Terminals

The switches are supplied with holes or with pins (Fig. 4) for connection.

They can be connected:

- a. by soldering to the holes in the printed-wiring board.
- b. by wire-wrapping the pins (AWG26).
- c. by reflow soldering the pins to a perpendicular external printed-wiring board ($250 \pm 2 \text{ }^\circ\text{C}$, max. 6 s).

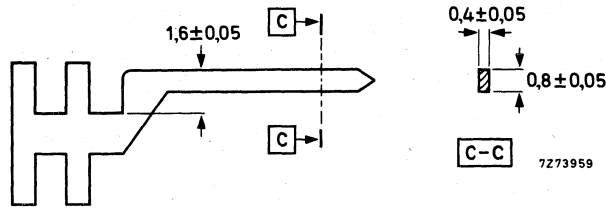


Fig. 4 Outlines of the pins.

The pitch of the holes on the p.w. board depends on the number of connections.

- for 8 connections or less (in general switches presenting only binary or only complementary output) the pitch is 2,54 mm.

If these switches are provided with pins, these pins are in line in position B as indicated in Fig. 5.

- for 9 or more connections the pitch is 2 mm.

If the switches are provided with pins, these pins are staggered according to Figs 5 and 6, to allow enough room for wire-wrapping tools.

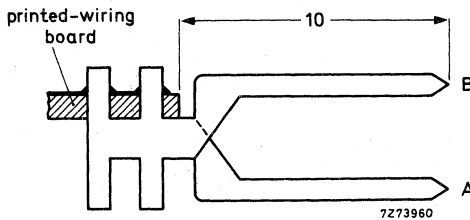


Fig. 5.

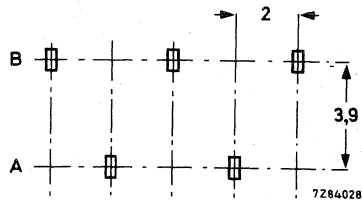


Fig. 6.

Mass 4 to 6 g.

Mounting

The switches are block mounted to a panel with a thickness of 1 to 3,5 mm by means of the spring locking end-pieces.

For panel cut-out see Fig. 7. N = number of switches.

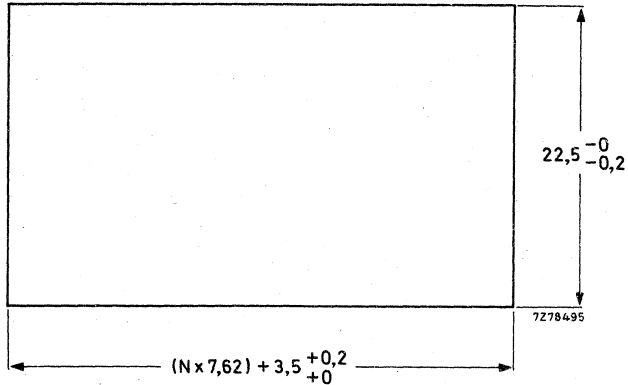


Fig. 7.

SURVEY OF TYPES

description	engraving	type	catalogue number
10-position/1 common	0 to 9	F10P1C	4311 027 94000
binary output	0 to 9	F1248	94010
binary + complementary output	0 to 9	F1248C	94020
complementary output	0 to 9	F1248CS	94030
binary + complementary output positive logic	0 to 9	F1248PC	94040
binary output (16-position)	0 to 9	F1248-16P	94050
complementary output (16-position)	A to F	F1248CS-16P	94060
	0 to 9		
binary + complementary output (16-position)	A to F	F1248C-16P	94070
	0 to 9		
set of end-pieces	A to F		94080

Note: Many types with additional properties mentioned under "Special versions" on next page, are included in our programme and are in current production or available from stock. Please contact the supplier if a version is required which is not present in the "Survey of types".

Special versions

Limit stops	Rotation of the rotor can be limited to any position by means of stop pins which can be installed by factory
Colour of housing	Other colours for housing can be considered, but only for order quantities in one batch and one colour of 10 000 pieces or more.
Special engraving	Special engraving requirements can be undertaken. Due to cost of specific tooling, a minimum quantity of 5000 is recommended.
Pins for wire-wrapping	All switches can be equipped with these pins (see under "Terminals"). Type number prefix is extended with a "W", for example FW1248C-16P.

TECHNICAL PERFORMANCE

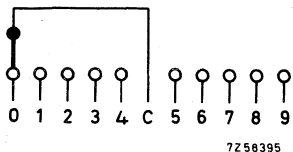
D.C. working voltage	100 V
D.C. test voltage	500 V
Insulation resistance, measured at 100 V (d.c.) * after humidity test	10 ⁵ MΩ 10 ³ MΩ
Power switching capability at resistive load	5 VA per output
Current switching capacity (d.c.) in purely resistive circuits	0,5 A
Maximum current carrying capacity (d.c.) at 25 °C	1,5 A
Contact resistance measured at 10 mA, 50 mV	< 100 mΩ
Operating temperature range	-25 to +70 °C
Storage temperature range	-25 to +85 °C
Life	in excess of 10 ⁶ commutations at a rate of 1 step/s
Operating force	6 N
Quality control tests, IEC 68-2: test C, damp heat	56 days

* Between any pair of terminals and between any terminal and all others connected together.

DIAGRAMS AND TERMINAL LOCATION

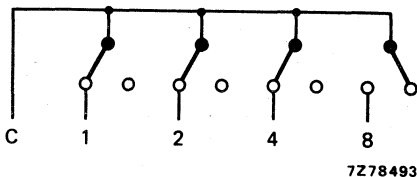
The terminals in the circuit diagrams have, from left to right, the same order as on the printed-wiring board when viewed from the solder side.

NF10P1C



Pitch between holes 2 mm (10 x)

NF1248

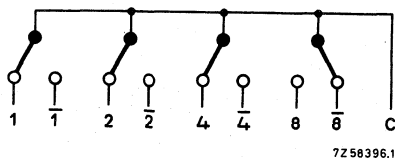


Pitch between holes 2,54 mm (4 x)

Truth table *

Index	1 2 4 8
0	0000
1	1000
2	0100
3	1100
4	0010
5	1010
6	0110
7	1110
8	0001
9	1001

F1248C



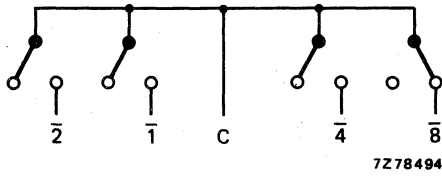
Pitch between holes 2 mm (8 x)

Truth table *

Index	1 2 4 8	1 2 4 8
0	0000	1111
1	1000	0111
2	0100	1011
3	1100	0011
4	0010	1101
5	1010	0101
6	0110	1001
7	1110	0001
8	0001	1110
9	1001	0110

* "1" means switch closed

NF1248CS

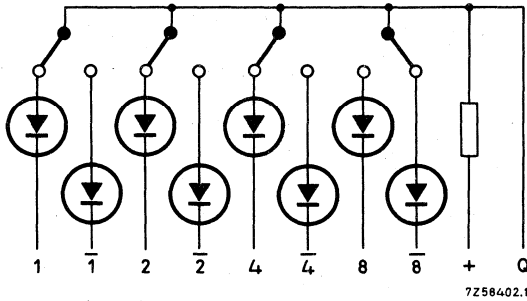


Pitch between holes 2,54 mm (4 x)

Truth table *

Index	1 2 4 8
0	1 1 1 1
1	0 1 1 1
2	1 0 1 1
3	0 0 1 1
4	1 1 0 1
5	0 1 0 1
6	1 0 0 1
7	0 0 0 1
8	1 1 1 0
9	0 1 1 0

F1248PC



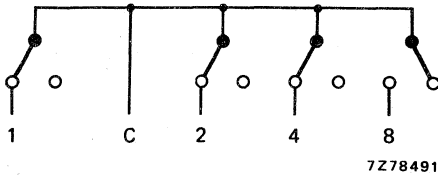
Pitch between holes 2 mm (9 x)

Truth table *

Index	1 2 4 8	1 2 4 8
0	0 0 0 0	1 1 1 1
1	1 0 0 0	0 1 1 1
2	0 1 0 0	1 0 1 1
3	1 1 0 0	0 0 1 1
4	0 0 1 0	1 1 0 1
5	1 0 1 0	0 1 0 1
6	0 1 1 0	1 0 0 1
7	1 1 1 0	0 0 0 1
8	0 0 0 1	1 1 1 0
9	1 0 0 1	0 1 1 0

* "1" means switch closed.

NF1248-16P

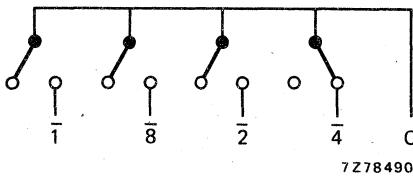


Pitch between holes 2,54 mm (4 x)

Truth table *

Index	1 2 4 8
0	0000
1	1000
2	0100
3	1100
4	0010
5	1010
6	0110
7	1110
8	0001
9	1001
A	0101
B	1101
C	0011
D	1011
E	0111
F	1111

NF1248CS-16P



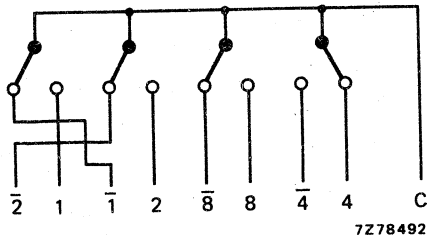
Pitch between holes 2,54 mm (4 x)

Truth table *

Index	1 2 4 8
0	1111
1	0111
2	1011
3	0011
4	1101
5	0101
6	1001
7	0001
8	1110
9	0110
A	1010
B	0010
C	1100
D	0100
E	1000
F	0000

* "1" means switch closed.

F1248C-16P



Pitch between holes 2,0 mm (8 x)

Truth table *

Index	1 2 4 8	1-bar 2-bar 4-bar 8-bar
0	0000	1111
1	1000	0111
2	0100	1011
3	1100	0011
4	0010	1101
5	1010	0101
6	0110	1001
7	1110	0001
8	0001	1110
9	1001	0110
A	0101	1010
B	1101	0010
C	0011	1100
D	1011	0100
E	0111	1000
F	1111	0000

* "1" means switch closed.

DEVELOPMENT SAMPLE DATA

This information is derived from development samples made available for evaluation. It does not necessarily imply that the device will go into regular production.

4311 027 955..

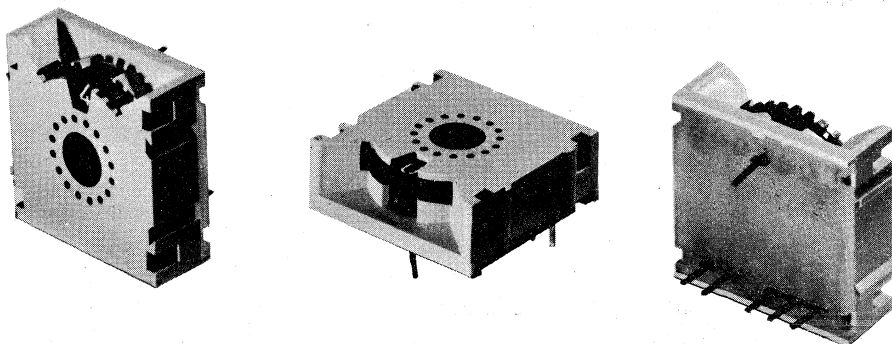
THUMBWHEEL SWITCHES

E- version

QUICK REFERENCE DATA

Contact resistance	< 100 m Ω
Temperature range	
Operating	-20 to + 85 °C
Storage	-40 to + 100 °C
Current switching capability	0,15 A

790816-01-02



APPLICATION

These thumbwheel switches are for use as preset devices in digital systems which have to handle numerical data, or as positioning switches. They are mounted directly onto a printed-wiring board. Assembling of the switches side by side is very simple due to a dovetail construction in the housing. This system permits extension of a circuit with one or more switches without demounting of already soldered items.

The switch is adjusted with finger or screwdriver.

CONSTRUCTION

Housing	grey plastic
Thumbwheel	red plastic, provided with 2 series of figures (and letters), one on cylinder and one on side of screwdriver adjustment, see Fig. 1
Contact springs	phosphor bronze with gold alloy (721)
Terminals	tin-plated pins, one part with contact springs
Thumbwheel detent	formed by the contact springs
Printed-wiring	on rotor, gold-plated tracks
Stacking	dovetail system
Limit stops	provision is made to insert stop pins
Type identification	catalogue number suffix (last 5 digits)
Marking	
10-position switch	0 to 9
16-position switch	0 to 9, and A to F*

Outlines

Dimensions in mm

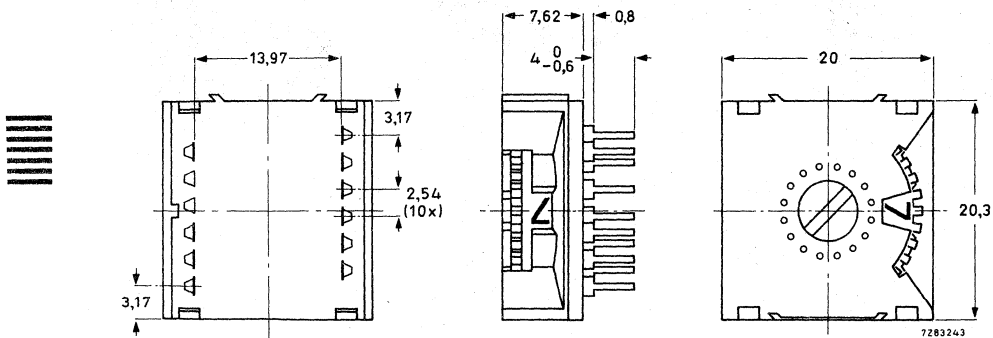


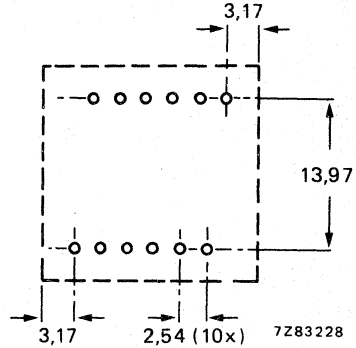
Fig. 1.

* Other engravings on request.

Terminals

The switches are supplied with pins for mounting onto a printed-wiring board. The hole pattern is given in Fig. 2. The items are suitable for wave soldering. (All types can be supplied without openings in the bottom where the pins pass, on request.) Switches with only one row of terminals have an extra C terminal for better mechanical stability.

Fig. 2 Hole pattern viewed from component side, hole diameter 0,8 mm.



DEVELOPMENT SAMPLE DATA

Mass 2 g approximately

Numerals

10-position and 16-position switches, both scales.

Size (height x width)

2,4 x 1,6 mm

Line thickness

0,3 mm

TECHNICAL PERFORMANCE

Working voltage

d.c.

36 V

r.m.s.

150 V

Test voltage (d.c. or r.m.s.)

500 V

Insulation resistance (initial)

min. 1000 M Ω

Power switching capability at resistive load

4 W

Current switching capacity in resistive load

0,15 A

Maximum current carrying capacity

1 A

Contact resistance

max. 100 m Ω

Life, at 5 V, 10 mA

min. 250 000 commutations

Operating torque

5 to 15 mNm

Temperature range

Operating

-20 to + 85 $^{\circ}$ C

Storage

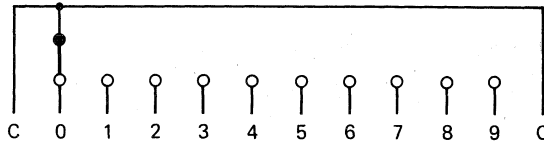
-40 to + 100 $^{\circ}$ C

SURVEY OF TYPES

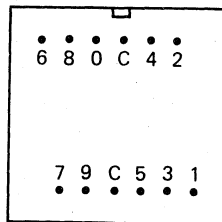
description	engraving	type	catalogue number
Decimal switch			
10-position/1 common	0 to 9	E10P1C/1	4311 027 95531
Coding switches 1.2.4.8			
<i>10-positions</i>			
binary output	0 to 9	E1248/1	4311 027 95541
complimentary output	0 to 9	E1248CS/1	4311 027 95551
binary + compl. output	0 to 9	E1248C/1	4311 027 95561
<i>16-positions</i>			
binary output	0 to 9, A to F	E1248-16P/1	4311 027 95501
complimentary output	0 to 9, A to F	E1248CS-16P/1	4311 027 95511
binary + compl. output	0 to 9, A to F	E1248C-16P/1	4311 027 95521

DIAGRAMS AND TERMINAL LOCATION

E10P1C/1



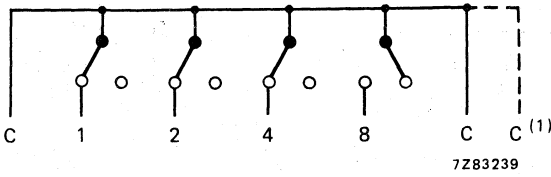
7Z83237



7Z83238

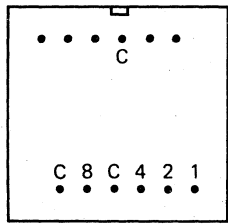


E1248/1



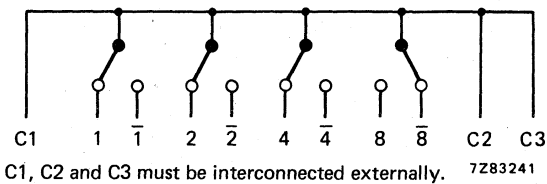
Truth table**

Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1



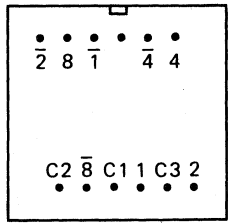
DEVELOPMENT SAMPLE DATA

E1248C/1



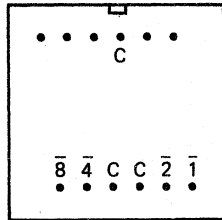
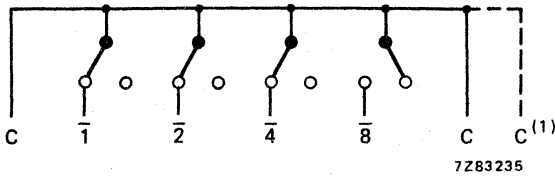
Truth table**

Index	1	2	4	8	$\bar{1}$	$\bar{2}$	$\bar{4}$	$\bar{8}$
0	0	0	0	0	1	1	1	1
1	1	0	0	0	0	1	1	1
2	0	1	0	0	1	0	1	1
3	1	1	0	0	0	0	1	1
4	0	0	1	0	1	1	0	1
5	1	0	1	0	0	1	0	1
6	0	1	1	0	1	0	0	1
7	1	1	1	0	0	0	0	1
8	0	0	0	1	1	1	1	0
9	1	0	0	1	0	1	1	0



(1) For better mechanical stability.
 ** "1" means switch closed.

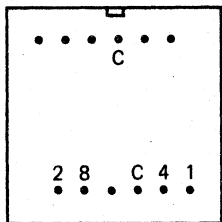
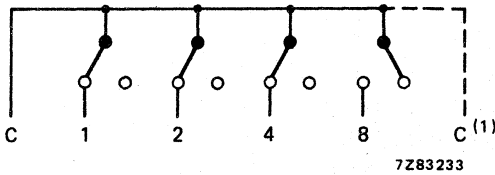
E1248CS/1



Truth table**

Index	$\bar{1}$	$\bar{2}$	$\bar{4}$	$\bar{8}$
0	1	1	1	1
1	0	1	1	1
2	1	0	1	1
3	0	0	1	1
4	1	1	0	1
5	0	1	0	1
6	1	0	0	1
7	0	0	0	1
8	1	1	1	0
9	0	1	1	0

E1248-16P/1

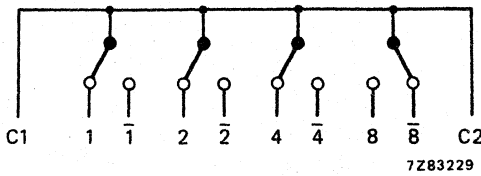


Truth table**

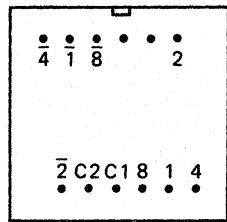
Index	1	2	4	8
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
A	0	1	0	1
B	1	1	0	1
C	0	0	1	1
D	1	0	1	1
E	0	1	1	1
F	1	1	1	1

(1) For better mechanical stability.
 ** "1" means switch closed.

E1248C-16P/1



C1 and C2 must be interconnected externally.

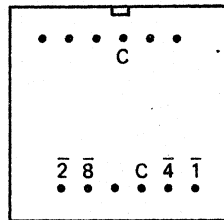
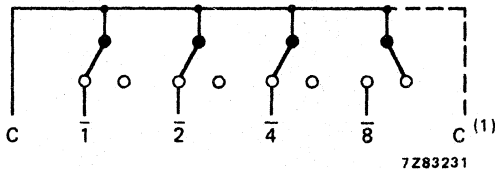


Truth table**

Index	1 2 4 8	$\bar{1}$ $\bar{2}$ $\bar{4}$ $\bar{8}$
0	0000	1111
1	1000	0111
2	0100	1011
3	1100	0011
4	0010	1101
5	1010	0101
6	0110	1001
7	1110	0001
8	0001	1110
9	1001	0110
A	0101	1010
B	1101	0010
C	0011	1100
D	1011	0100
E	0111	1000
F	1111	0000

DEVELOPMENT SAMPLE DATA

E1248CS-16P/1



Truth table**

Index	1 2 4 8
0	1111
1	0111
2	1011
3	0011
4	1101
5	0101
6	1001
7	0001
8	1110
9	0110
A	1010
B	0010
C	1100
D	0100
E	1000
F	0000

(1) For better mechanical stability.

** "1" means switch closed.

|||||

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